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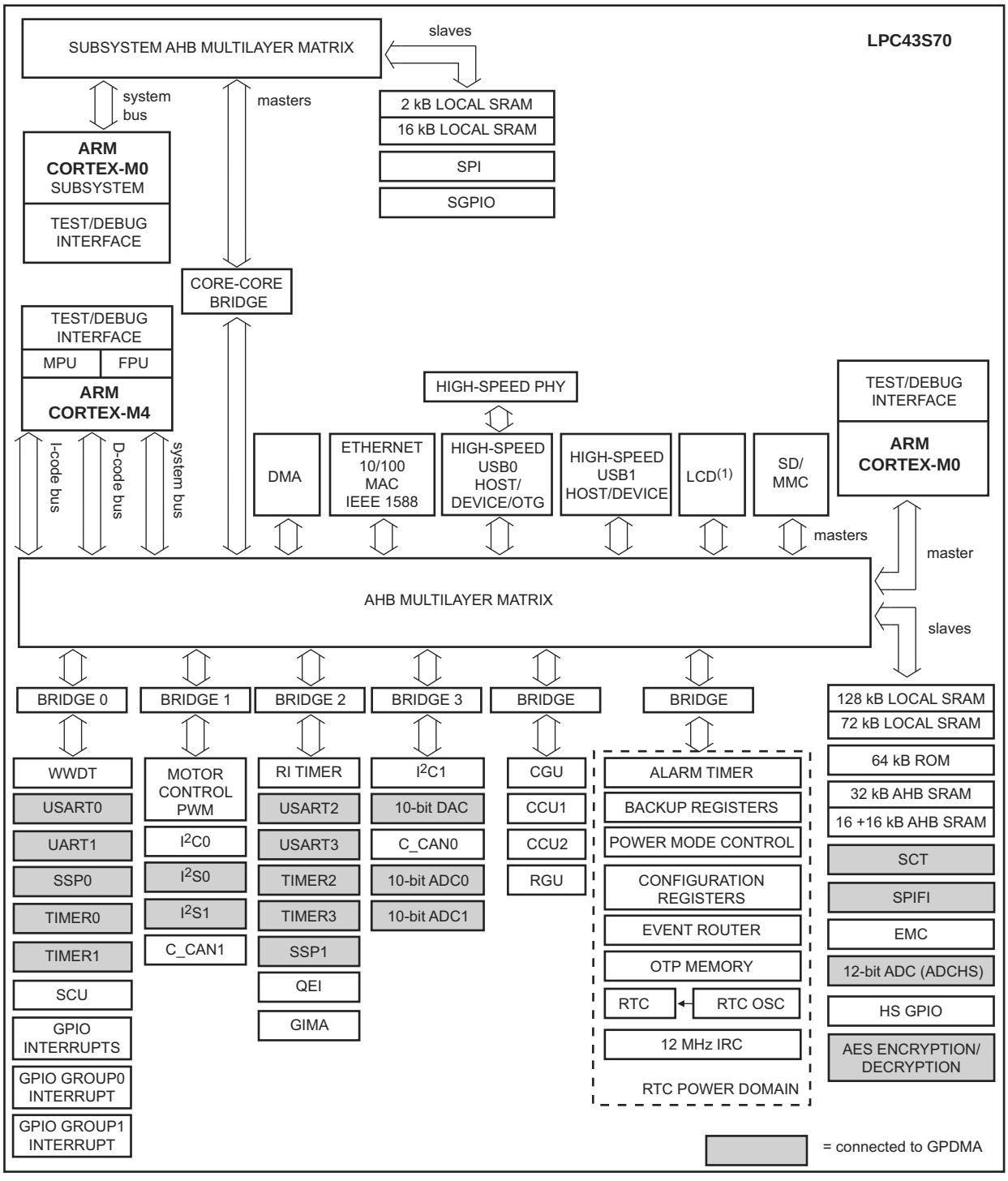
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	49
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	282K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x10b, 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc43s70fet100e

5. Block diagram



(1) Not available on all parts (see Table 2).

Fig 1. LPC43S70 Block diagram

Table 3. Pin description

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
Multiplexed digital pins						
P0_0	L3	G2	[3]	I; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
					I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
					I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
					I/O	**SGPIO0 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
					I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
P0_1	M2	G1	[3]	I; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
					I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
					I	**ENET_COL —** Ethernet Collision detect (MII interface).
					I/O	**SGPIO1 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
						ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
					I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
P1_0	P2	H1	[3]	I; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
					I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
					I/O	**EMC_A5 —** External memory address line 5.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SSP0_SSEL —** Slave Select for SSP0.
					I/O	**SGPIO7 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
P1_1	R2	K2	[3]	I; PU	I/O	**GPIO0[8] —** General purpose digital input/output pin. Boot pin (see Table 5).
					O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
					I/O	**EMC_A6 —** External memory address line 6.
					I/O	**SGPIO8 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
					-	**R —** Function reserved.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P5_7	R12	-	[3]	I; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
					O	**MCOA2 —** Motor control PWM channel 2, output A.
					I/O	**EMC_D11 —** External memory data line 11.
					-	**R —** Function reserved.
					I	**U1_RXD —** Receiver input for UART 1.
					O	**T1_MAT3 —** Match output 3 of timer 1.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_0	M12	H7	[3]	I; PU	-	**R —** Function reserved.
					O	**I2S0_RX_MCLK —** I2S receive master clock.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_1	R15	G5	[3]	I; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
					O	**EMC_DYCS1 —** SDRAM chip select 1.
					I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
					I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
					-	**R —** Function reserved.
					I	**T2_CAP0 —** Capture input 2 of timer 2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_2	L13	J9	[3]	I; PU	I/O	**GPIO3[1] —** General purpose digital input/output pin.
					O	**EMC_CKEOUT1 —** SDRAM clock enable 1.
					I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
					I/O	**I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
					-	**R —** Function reserved.
					I	**T2_CAP1 —** Capture input 1 of timer 2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P7_6	C7	-	[3]	I; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
					O	**CTOUT_11 —** SCT output 1. Match output 3 of timer 2.
					-	**R —** Function reserved.
					O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
					-	**R —** Function reserved.
					O	**TRACEDATA[2] —** Trace data, bit 2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P7_7	B6	-	[6] [13]	I; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
					O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
					-	**R —** Function reserved.
					O	**LCD_PWR —** LCD panel power enable.
					-	**R —** Function reserved.
					O	**TRACEDATA[3] —** Trace data, bit 3.
					O	**ENET_MDC —** Ethernet MIIM clock.
					I/O	**SGPIO7 —** General purpose digital input/output pin.
					AI	**ADC1_6 —** ADC1, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P8_0	E5	-	[4] [13]	I; PU	I/O	**GPIO4[0] —** General purpose digital input/output pin.
					I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					-	**R —** Function reserved.
					I	**MCI2 —** Motor control PWM channel 2, input.
					I/O	**SGPIO8 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**T0_MAT0 —** Match output 0 of timer 0.
P8_1	H5	-	[4]	I; PU	I/O	**GPIO4[1] —** General purpose digital input/output pin.
					O	**USB0_IND1 —** USB0 port indicator LED control output 1.
					-	**R —** Function reserved.
					I	**MCI1 —** Motor control PWM channel 1, input.
					I/O	**SGPIO9 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**T0_MAT1 —** Match output 1 of timer 0.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P8_2	K4	-	[4]	I; PU	I/O	**GPIO4[2] —** General purpose digital input/output pin.
					O	**USB0_IND0 —** USB0 port indicator LED control output 0.
					-	**R —** Function reserved.
					I	**MCI0 —** Motor control PWM channel 0, input.
					I/O	**SGPIO10 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**T0_MAT2 —** Match output 2 of timer 0.
P8_3	J3	-	[3]	I; PU	I/O	**GPIO4[3] —** General purpose digital input/output pin.
					I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
					-	**R —** Function reserved.
					O	**LCD_VD12 —** LCD data.
					O	**LCD_VD19 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**T0_MAT3 —** Match output 3 of timer 0.
P8_4	J2	-	[3]	I; PU	I/O	**GPIO4[4] —** General purpose digital input/output pin.
					I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
					-	**R —** Function reserved.
					O	**LCD_VD7 —** LCD data.
					O	**LCD_VD16 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I	**T0_CAP0 —** Capture input 0 of timer 0.
P8_5	J1	-	[3]	I; PU	I/O	**GPIO4[5] —** General purpose digital input/output pin.
					I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
					-	**R —** Function reserved.
					O	**LCD_VD6 —** LCD data.
					O	**LCD_VD8 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I	**T0_CAP1 —** Capture input 1 of timer 0.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PE_14	C15	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**EMC_DYCS3 —** SDRAM chip select 3.
					I/O	**GPIO7[14] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
PE_15	E13	-	[3]	I; PU	-	**R —** Function reserved.
					O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
					I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I^2C pad).
					O	**EMC_CKEOUT3 —** SDRAM clock enable 3.
					I/O	**GPIO7[15] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
PF_0	D12	-	[3]	O; PU	I/O	**SSP0_SCK —** Serial clock for SSP0.
					I	**GP_CLKIN —** General purpose clock input to the CGU.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**I2S1_TX_MCLK —** I2S1 transmit master clock.
PF_1	E11	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SSP0_SSEL —** Slave Select for SSP0.
					-	**R —** Function reserved.
					I/O	**GPIO7[16] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I/O	**SGPIO0 —** General purpose digital input/output pin.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PF_2	D11	-	[3]	I; PU	-	**R —** Function reserved.
					O	**U3_TXD —** Transmitter output for USART3.
					I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
					-	**R —** Function reserved.
					I/O	**GPIO7[17] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I/O	**SGPIO1 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
PF_3	E10	-	[3]	I; PU	-	**R —** Function reserved.
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
					-	**R —** Function reserved.
					I/O	**GPIO7[18] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I/O	**SGPIO2 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
PF_4	D10	H4	[3]	O; PU	I/O	**SSP1_SCK —** Serial clock for SSP1.
					I	**GP_CLKIN —** General purpose clock input to the CGU.
					O	**TRACECLK —** Trace clock.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**I2S0_TX_MCLK —** I2S transmit master clock.
					I/O	**I2S0_RX_SCK —** I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
PF_5	E9	-	[6]	I; PU	-	**R —** Function reserved.
					I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
					I/O	**SSP1_SSEL —** Slave Select for SSP1.
					O	**TRACEDATA[0] —** Trace data, bit 0.
					I/O	**GPIO7[19] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I/O	**SGPIO4 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					AI	**ADC1_4 —** ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
Clock pins						
CLK0	N5	K3	[5]	O; PU	O	**EMC_CLK0 —** SDRAM clock 0.
					O	**CLKOUT —** Clock output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SD_CLK —** SD/MMC card clock.
					O	**EMC_CLK01 —** SDRAM clock 0 and clock 1 combined.
					I/O	**SSP1_SCK —** Serial clock for SSP1.
					I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
CLK1	T10	-	[5]	O; PU	O	**EMC_CLK1 —** SDRAM clock 1.
					O	**CLKOUT —** Clock output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**CGU_OUT0 —** CGU spare clock output 0.
					-	**R —** Function reserved.
					O	**I2S1_TX_MCLK —** I2S1 transmit master clock.
CLK2	D14	K6	[5]	O; PU	O	**EMC_CLK3 —** SDRAM clock 3.
					O	**CLKOUT —** Clock output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SD_CLK —** SD/MMC card clock.
					O	**EMC_CLK23 —** SDRAM clock 2 and clock 3 combined.
					O	**I2S0_TX_MCLK —** I2S transmit master clock.
					I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
CLK3	P12	-	[5]	O; PU	O	**EMC_CLK2 —** SDRAM clock 2.
					O	**CLKOUT —** Clock output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**CGU_OUT1 —** CGU spare clock output 1.
					-	**R —** Function reserved.
					I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
Debug pins						

In the two-counter case, the following operational elements are global to the SCT, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.16.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs and interrupts.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs (one input connected internally)
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states

7.16.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

7.16.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.
- Each slice has a 32-bit pattern match filter.

7.17 AHB peripherals

7.17.1 AES decryption/encryption

The hardware AES engine can decode and encode data using the AES algorithm in conjunction with a 128-bit key.

The AES encryption and decryption features are accessible through the ROM-based AES API.

7.17.1.1 Features

- On-chip API support for AES encryption and decryption.
- Two 128-bit OTP memories for AES key storage and customer use.One OTP memory bank is encrypted.
- Random number generator (RNG) accessible through AES API.
- Unique ID for each device.
- Decoding of external flash data connected to the quad SPI Flash Interface (SPIFI).
- Secure storage of encryption and decryption keys.
- Support for CMAC hash calculation to authenticate encrypted data.
- AES engine supports the following modes:
  - Electronic Code Block (ECB) mode (encryption and decryption) with 128-bit key.
  - Cypher Block Chaining (CBC) mode (encryption and decryption) with 128-bit key.
- The AES engine is compliant with the FIPS (Federal Information Processing Standard) Publication 197, Advanced Encryption Standard (AES).
- Random Number Generator (RNG) is supported by the AES API and passes the following tests:
  - diehard
  - FIPS_140-1
  - NIST
- Data is processed in little endian mode. This means that the first byte read from flash is integrated into the AES codeword as least significant byte. The 16th byte read from flash is the most significant byte of the first AES codeword.
- AES peak engine performance of 0.5 byte/clock cycle.
- DMA transfers supported through the GPDMA.

7.17.2 General Purpose DMA (GPDMA)

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

7.17.2.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.

7.17.4 SD/MMC card interface

The SD/MMC card interface supports the following modes to control:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)
- MultiMedia Cards (MMC version 4.4)

7.17.5 External Memory Controller (EMC)

The LPC43S70 EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

7.17.5.1 Features

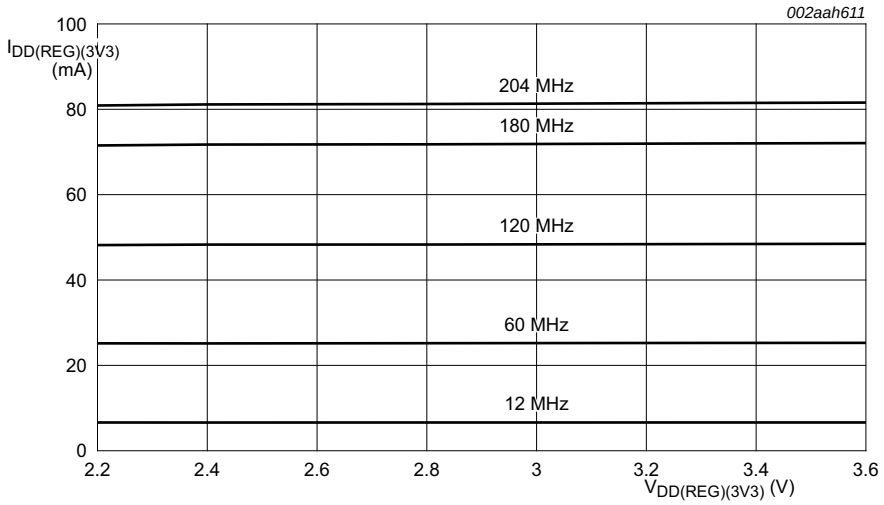
- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.17.6 High-speed USB Host/Device/OTG interface (USB0)

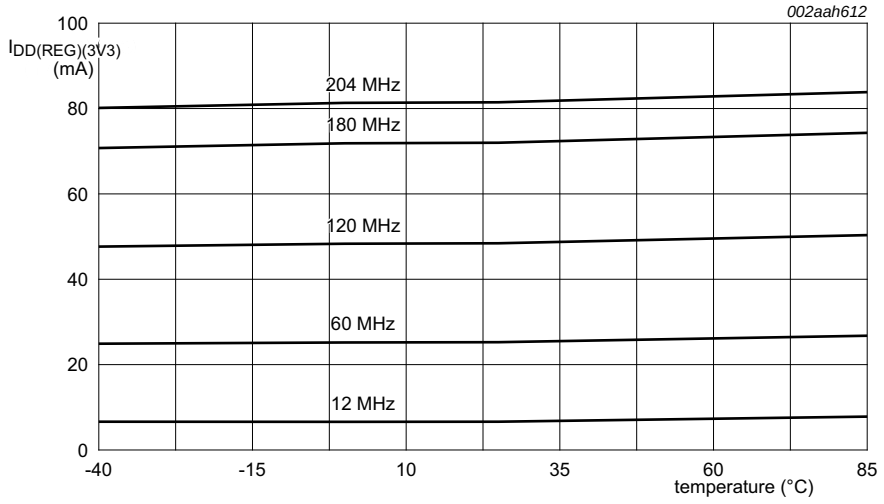
The USB OTG module allows the LPC43S70 to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

10.1 Power consumption



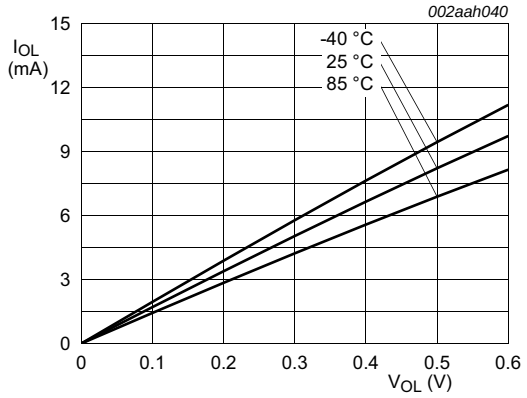
Conditions: T_{amb} = 25 °C; active mode entered executing code while(1){} from SRAM; M0 cores in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 8. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode

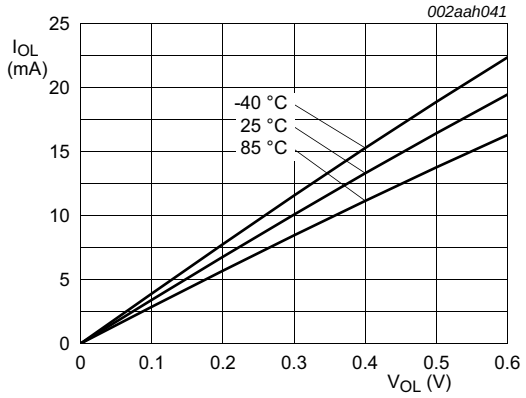


Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V, Active mode entered executing code while(1){} from SRAM;M0 cores in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

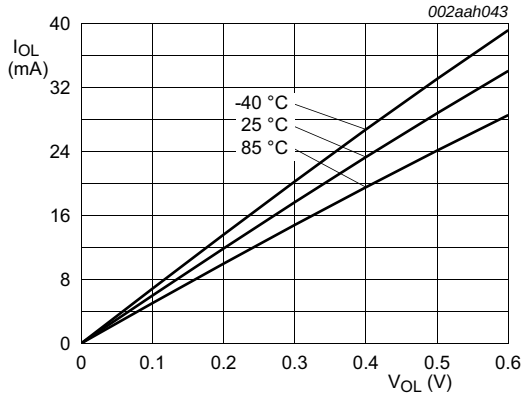
Fig 9. Typical supply current versus temperature in Active mode



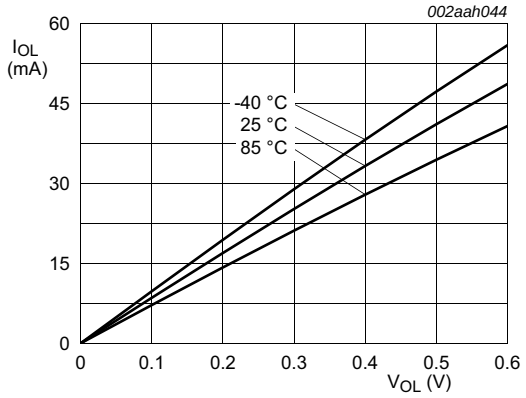
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 19. High-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}

11.3 Crystal oscillator

Table 17. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1 MHz - 20 MHz)[5]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 MHz - 25 MHz)[6]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.4 IRC oscillator

Table 18. Dynamic characteristic: IRC oscillator

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.82	12.0	12.18	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 GPCLKIN

Table 19. Dynamic characteristic: GPCLKIN

T_{amb} = 25 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Min	Typ	Max	Unit
GP_CLKIN	input frequency	-	-	25	MHz

11.6 I/O pins

Table 20. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	1.0	-	2.5	ns
t_f	fall time	pin configured as output; EHS = 1	[2][3]	0.9	-	2.5	ns
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.3	ns

allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

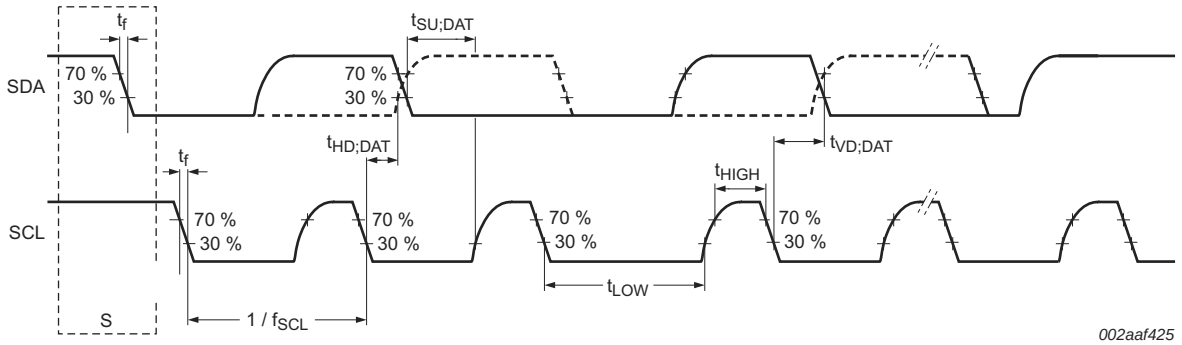


Fig 24. I²C-bus pins clock timing

11.9 I²S-bus interface

Table 23. Dynamic characteristics: I²S-bus interface pins

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

11.12 SPI interface

Table 26. Dynamic characteristics: SPI

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time			5			ns
$T_{cy(clk)}$	clock cycle time		[1]	40	-	-	ns
Master							
t_{DS}	data set-up time			7.2	-	-	ns
t_{DH}	data hold time			0	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	3.7	ns
$t_{h(Q)}$	data output hold time			-	-	1.2	ns
Slave							
t_{DS}	data set-up time			1.2	-	-	ns
t_{DH}	data hold time			3 x $T_{cy(PCLK)}$ + 0.54	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	3 x $T_{cy(PCLK)}$ + 9.7	ns
$t_{h(Q)}$	data output hold time			-	-	2 x $T_{cy(PCLK)}$ + 7.1	ns

[1] $T_{cy(clk)}$ = 8/BASE_SPI_CLK. Tcy(PCLK) = 1/BASE_SPI_CLK.

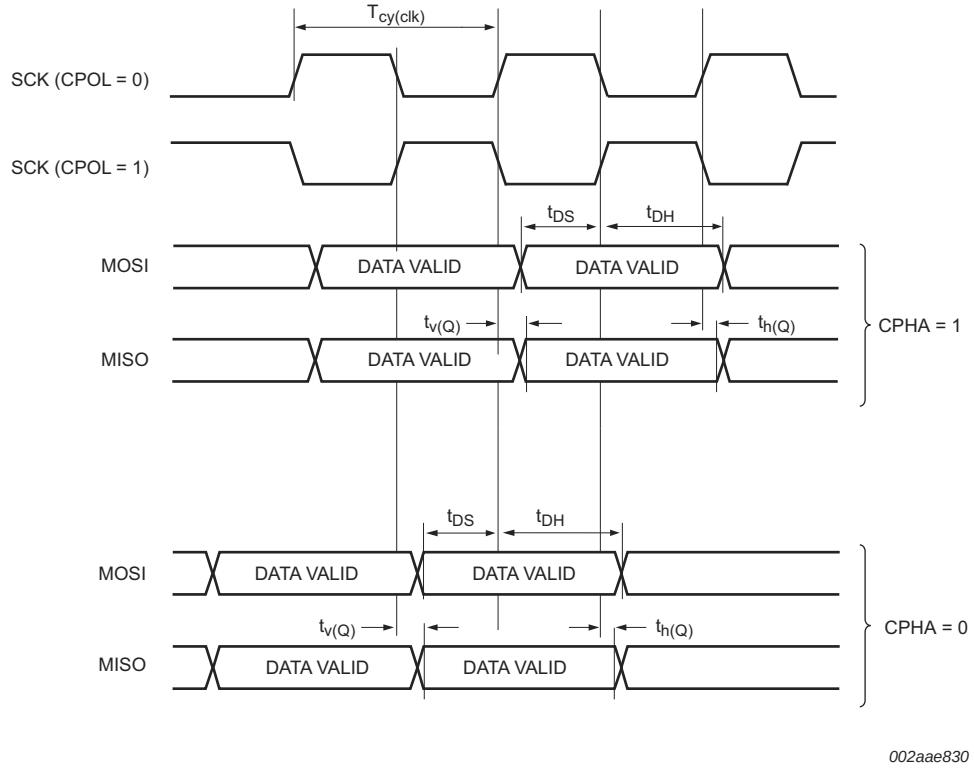


Fig 29. SSP slave timing in SPI mode

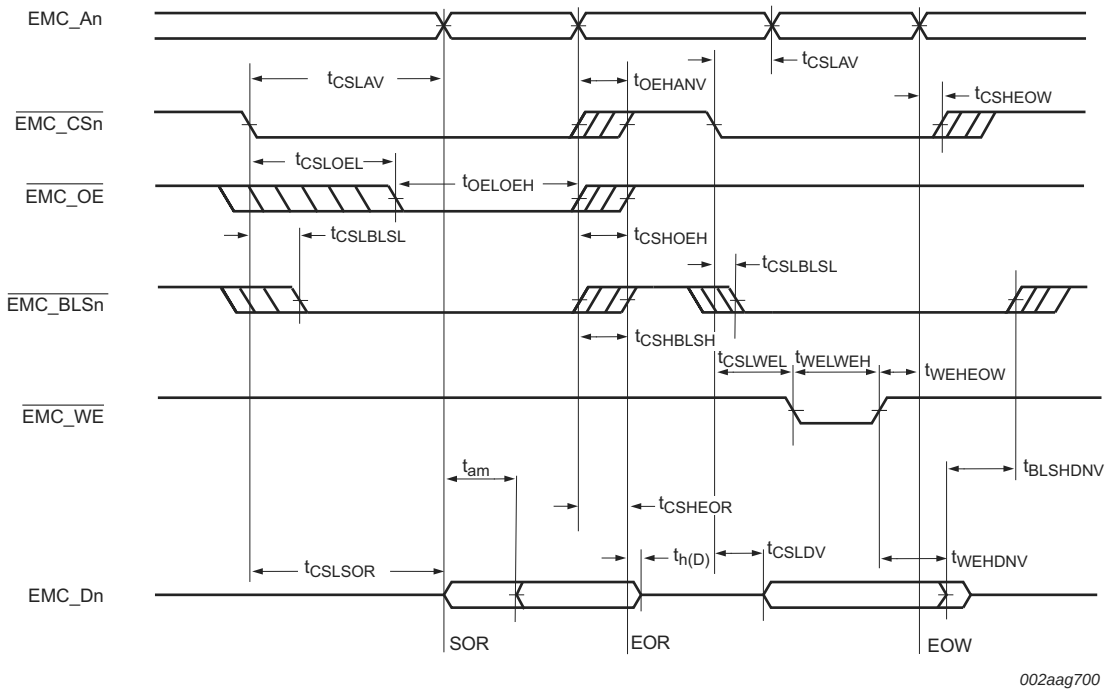


Fig 33. External static memory read/write access (PB = 1)

11.17 USB interface

Table 32. Dynamic characteristics: USB0 and USB1 pins (full-speed)
C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(IO)}$; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4	-	20	ns
t_f	fall time	10 % to 90 %		4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90	-	111.11	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 35		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 35		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 35	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 35	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

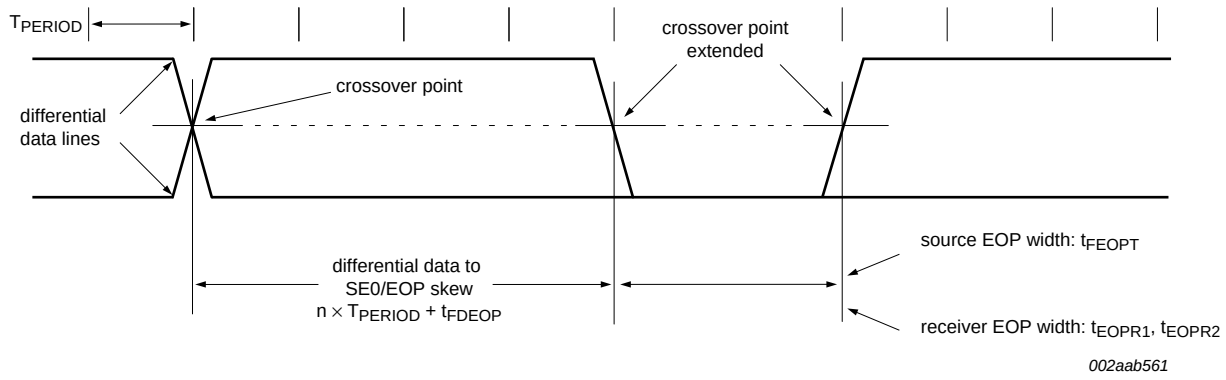


Fig 35. Differential data-to-EOP transition skew and EOP width

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