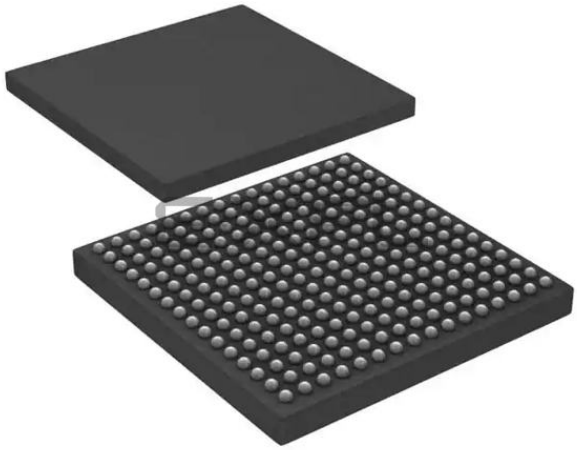


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, QEI, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	164
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	282K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 3x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc43s70fet256e

6. Pinning information

6.1 Pinning

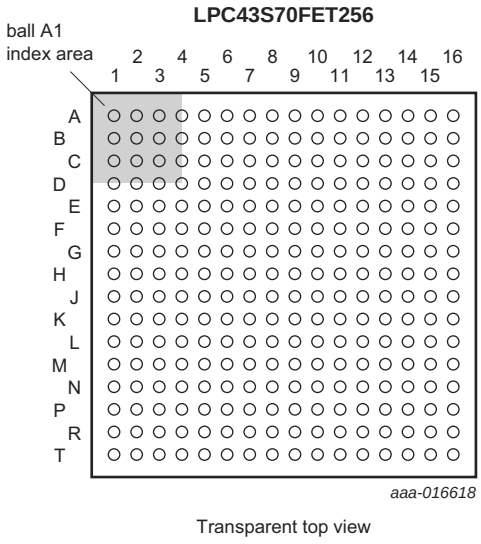


Fig 2. Pin configuration LBGA256 package

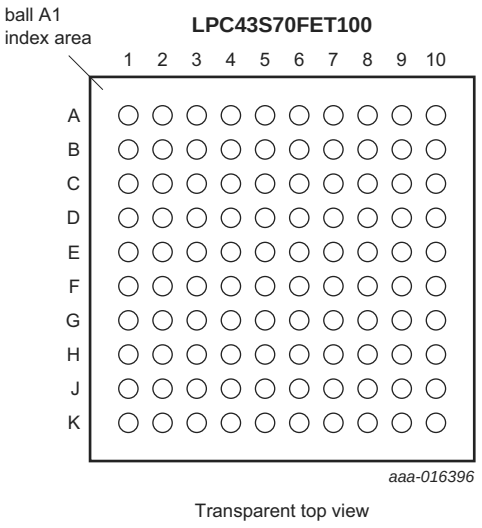


Fig 3. Pin configuration TFBGA100 package

6.2 Pin description

On the LPC43S70, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100	Reset state [2]	Type	Description
P4_2	D3	-	[3] I; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
				O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
				O	**LCD_VD3 —** LCD data.
				-	**R —** Function reserved.
				-	**R —** Function reserved.
				O	**LCD_VD12 —** LCD data.
				I	**U3_RXD —** Receiver input for USART3.
				I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	-	[6] [13] I; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
				O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
				O	**LCD_VD2 —** LCD data.
				-	**R —** Function reserved.
				-	**R —** Function reserved.
				O	**LCD_VD21 —** LCD data.
				I/O	**U3_BAUD —** Baud pin for USART3.
				I/O	**SGPIO9 —** General purpose digital input/output pin.
				AI	**ADC0_0 —** ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	-	[6] I; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
				O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
				O	**LCD_VD1 —** LCD data.
				-	**R —** Function reserved.
				-	**R —** Function reserved.
				O	**LCD_VD20 —** LCD data.
				I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
				I/O	**SGPIO10 —** General purpose digital input/output pin.
				O	**DAC —** DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	-	[3] I; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
				O	**CTOUT_5 —** SCT output 5. Match output 1 of timer 1.
				O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
				-	**R —** Function reserved.
				-	**R —** Function reserved.
				-	**R —** Function reserved.
				-	**R —** Function reserved.
				I/O	**SGPIO11 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P6_3	P15	-	[3]	I; PU	I/O	**GPIO3[2] —** General purpose digital input/output pin.
					I	**USB0_PWR_EN —** VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH).
					I/O	**SGPIO4 —** General purpose digital input/output pin.
					O	**EMC_CS1 —** LOW active Chip Select 1 signal.
					-	**R —** Function reserved.
					I	**T2_CAP2 —** Capture input 2 of timer 2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_4	R16	F6	[3]	I; PU	I/O	**GPIO3[3] —** General purpose digital input/output pin.
					I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
					O	**U0_TXD —** Transmitter output for USART0.
					O	**EMC_CAS —** LOW active SDRAM Column Address Strobe.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_5	P16	F9	[3]	I; PU	I/O	**GPIO3[4] —** General purpose digital input/output pin.
					O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
					I	**U0_RXD —** Receiver input for USART0.
					O	**EMC_RAS —** LOW active SDRAM Row Address Strobe.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_6	L14	-	[3]	I; PU	I/O	**GPIO0[5] —** General purpose digital input/output pin.
					O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.
					I/O	**SGPIO5 —** General purpose digital input/output pin.
					I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					-	**R —** Function reserved.
					I	**T2_CAP3 —** Capture input 3 of timer 2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PA_2	K15	-	[4]	I; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
					I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
					-	**R —** Function reserved.
					I	**U2_RXD —** Receiver input for USART2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
PA_3	H11	-	[4]	I; PU	I/O	**GPIO4[10] —** General purpose digital input/output pin.
					I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
PA_4	G13	-	[3]	I; PU	-	**R —** Function reserved.
					O	**CTOUT_9 —** SCT output 9. Match output 1 of timer 2.
					-	**R —** Function reserved.
					I/O	**EMC_A23 —** External memory address line 23.
					I/O	**GPIO5[19] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
PB_0	B15	-	[3]	I; PU	-	**R —** Function reserved.
					O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
					O	**LCD_VD23 —** LCD data.
					-	**R —** Function reserved.
					I/O	**GPIO5[20] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PC_10	M5	-	[3]	I; PU	-	**R —** Function reserved.
					O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
					I	**U1_DSR —** Data Set Ready input for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[9] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					O	**T3_MAT3 —** Match output 3 of timer 3.
					I/O	**SD_CMD —** SD/MMC command signal.
PC_11	L5	-	[3]	I; PU	-	**R —** Function reserved.
					I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction.
					I	**U1_DCD —** Data Carrier Detect input for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[10] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[11] —** General purpose digital input/output pin.
					I/O	**SGPIO11 —** General purpose digital input/output pin.
					I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
					I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**U1_TXD —** Transmitter output for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[12] —** General purpose digital input/output pin.
					I/O	**SGPIO12 —** General purpose digital input/output pin.
					I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
					I/O	**SD_DAT6 —** SD/MMC data bus line 6.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100	Reset state [2]	Type	Description
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	F10, K5	-	-	I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VDD	-	-			Power supply for main regulator, I/O, and OTP.
VSS	G9, H7, J10, J11, K8	-	-	-	Ground.
VSSIO	C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13	C8, D4, D5, G8, J3, J6	-	-	Ground.
VSSA	B2	C2	-	-	Analog ground.
Not connected					
-	B9	-	-	-	n.c.

[1] - = not pinned out.

[2] I = input, O = output, AI/O analog input/output, IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to $V_{DD(IO)}$); F = floating. Reset state reflects the pin state at reset without boot code operation.

[3] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[4] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V) providing digital I/O functions with TTL levels, and hysteresis; high drive strength.

[5] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V) providing high-speed digital I/O functions with TTL levels and hysteresis.

[6] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input or output (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V). When configured as a ADC input or DAC output, the pin is not 5 V tolerant and the digital section of the pad must be disabled by setting the pin to an input function and disabling the pull-up resistor through the pin's SFSP register.

[7] 5 V tolerant transparent analog pad.

[8] For maximum load C_L = 6.5 μF and maximum resistance R_{pd} = 80 kΩ, the VBUS signal takes about 2 s to fall from VBUS = 5 V to VBUS = 0.2 V when it is no longer driven.

[9] Transparent analog pad. Not 5 V tolerant.

[10] Pad provides USB functions (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V). It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only).

[11] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus Fast Mode Plus specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines.

[12] 5 V tolerant pad with 20 ns glitch filter; provides digital I/O functions with open-drain output with weak pull-up resistor and hysteresis.

[13] To minimize interference on the 12-bit ADC signal lines, do not configure the digital signal as output when using the 12-bit ADC. See Table 45.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC43S70 use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

An ARM Cortex-M0 coprocessor is included in the LPC43S70, capable of off-loading the main ARM Cortex-M4 application processor. Most peripheral interrupts are connected to both processors. The processors communicate with each other via an interprocessor communication protocol.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core. The processor includes a NVIC with up to 53 interrupts.

7.3 ARM Cortex-M0 processors

The ARM Cortex-M0 processors are general purpose, 32-bit microprocessors, which offer high performance and very low power consumption. The ARM Cortex-M0 processor uses a 3-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The processors each incorporate an NVIC with 32 interrupts.

7.3.1 ARM Cortex-M0 coprocessor

The M0 coprocessor resides on the same AHB multi-layer matrix as the main Cortex-M0 core. The coprocessor can be used to off-load multiple tasks from the main Cortex-M4 processor.

7.3.2 ARM Cortex-M0 subsytem

The Cortex-M0 subsystem can be used to manage the SGPIO and SPI peripherals on the M0 subsystem multilayer matrix but any other peripheral as well. The M0 subsystem is separated by a bridge from the main AHB matrix. The M0 subsystem AHB matrix has two SRAM blocks which allows to run the Cortex-M0 subsytem at full speed independently from the main matrix.

One application of using the subsystem is to reduce power, for example when the main matrix runs at a very low speed and the M0 subsystem monitors activity and increases the main matrix speed when needed.

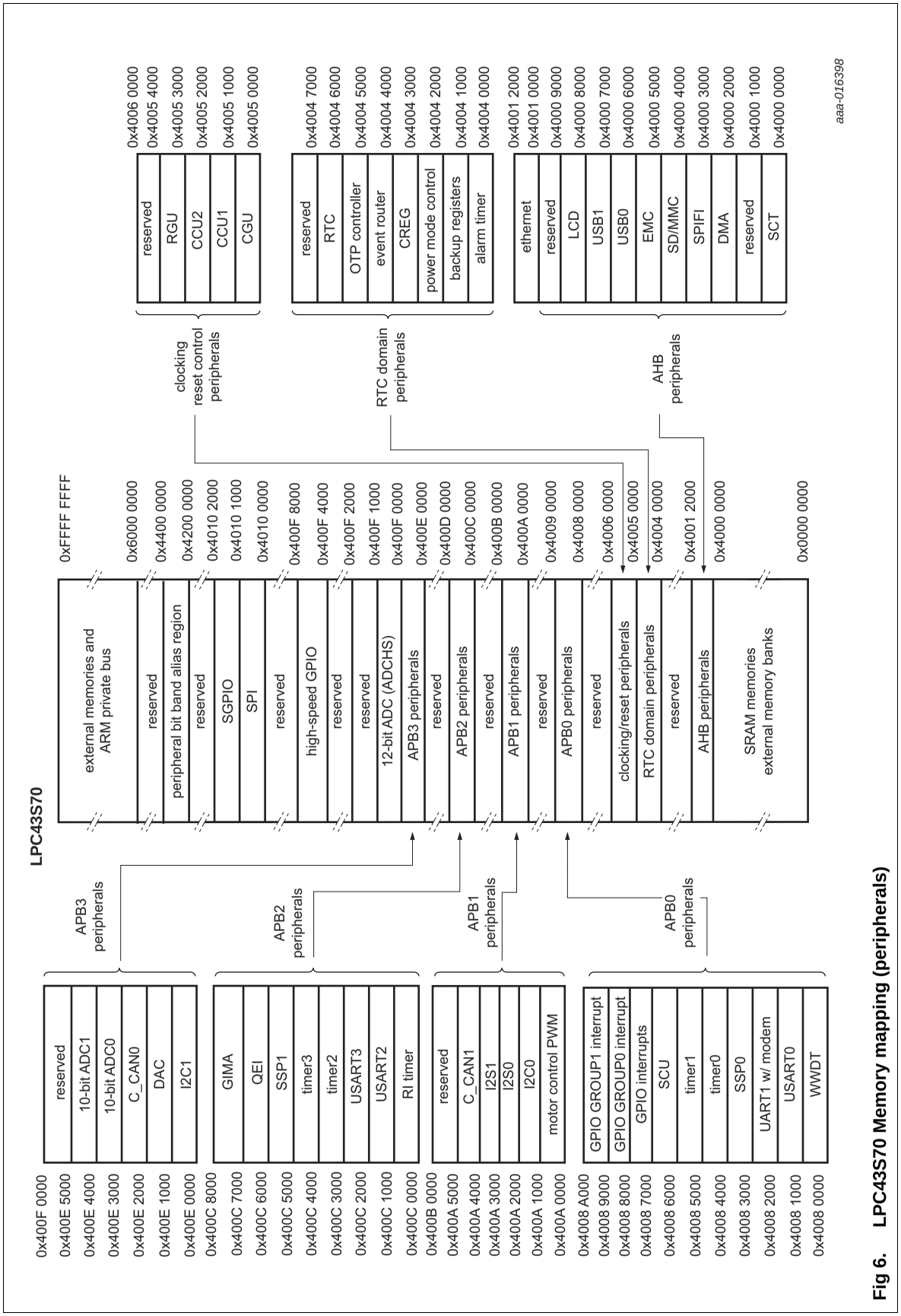


Fig 6. LPC43S70 Memory mapping (peripherals)

- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.19.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.19.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.19.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

- Measurement range of 0 V to 1.2 V.
- 12-bit conversion rate of 80 MSamples/s.
- Conversion on transition on input pin or various internal signals.
- Output FIFO with DMA support.

7.20.2 10-bit Analog-to-Digital Converter (ADC0/1)

7.20.2.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins per ADC for a total of 16 individual channels.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.20.3 Digital-to-Analog Converter (DAC)

7.20.3.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

7.21 Peripherals in the RTC power domain

7.21.1 RTC

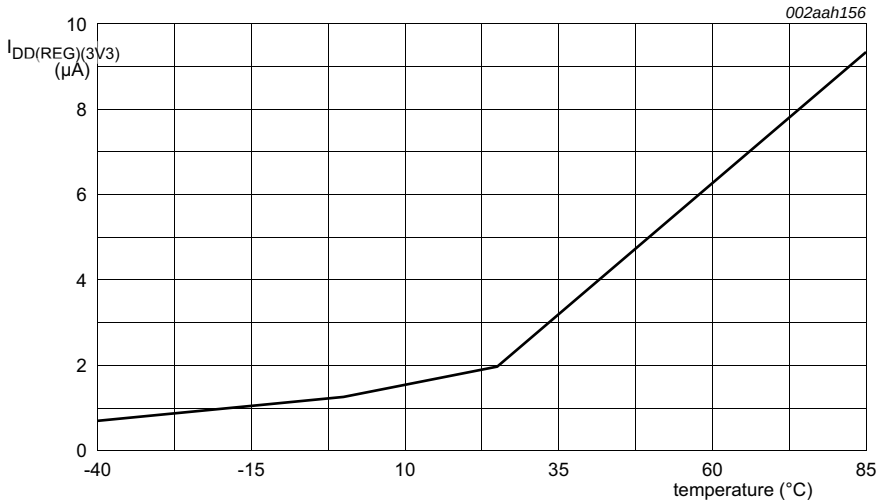
The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses very little power when its registers are not being accessed by the CPU, especially reduced power modes. The RTC is clocked by a separate 32 kHz oscillator that produces a 1 Hz internal time reference. The RTC is powered by its own power supply pin, VBAT.

7.21.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.

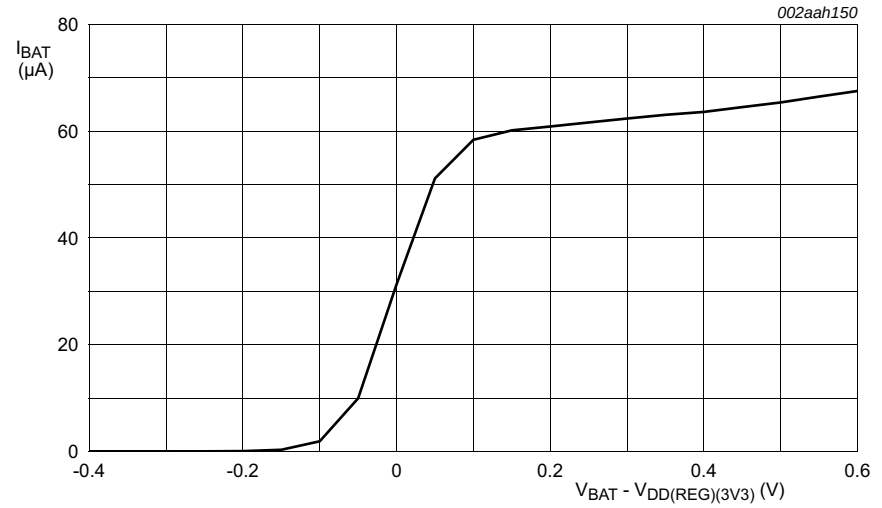
Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{BAT}	battery supply current	$V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} = 3.6 V	[8]				
		deep-sleep mode		-	2	-	µA
		power-down mode	[8]	-	2	-	µA
		deep power-down mode	[8]	-	2	-	µA
$I_{DD(IO)}$	I/O supply current	deep sleep mode		-	1	-	µA
		power-down mode		-	1	-	µA
		deep power-down mode	[9]	-	0.05	-	µA
I_{DDA}	Analog supply current	on pin VDDA;	[11]	-	0.4	-	
		deep sleep mode					µA
		power-down mode	[11]	-	0.4	-	µA
		deep power-down mode	[11]	-	0.007	-	µA
$\overline{\text{RESET}}$,RTC_ALARM, WAKEUPn pins							
V_{IH}	HIGH-level input voltage		[10]	$0.8 \times (V_{ps} - 0.35)$	-	5.5	V
V_{IL}	LOW-level input voltage		[10]	0	-	$0.3 \times (V_{ps} - 0.1)$	V
V_{hys}	hysteresis voltage		[10]	$0.05 \times (V_{ps} - 0.35)$	-	-	V
Vo	output voltage		[10]	-	V_{ps} - 0.2	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	5.2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V		-	-	20	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function;		0	-	5.5	V
		$V_{DD(IO)} \geq$ 2.2 V					
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(IO)}$	-	-	V



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} floating; $V_{DD(IO)}$ = 3.3 V.

Fig 14. Typical supply current versus temperature in Deep power-down mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; CCLK = 12 MHz.

Fig 15. Typical battery supply current in Active mode

[1] Clock to the I²S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I²S-bus interface PCLK = BASE_APB1_CLK / 12. I²S clock cycle time $T_{cy(clk)}$ = 79.2 ns; corresponds to the SCK signal in the *I²S-bus specification*.

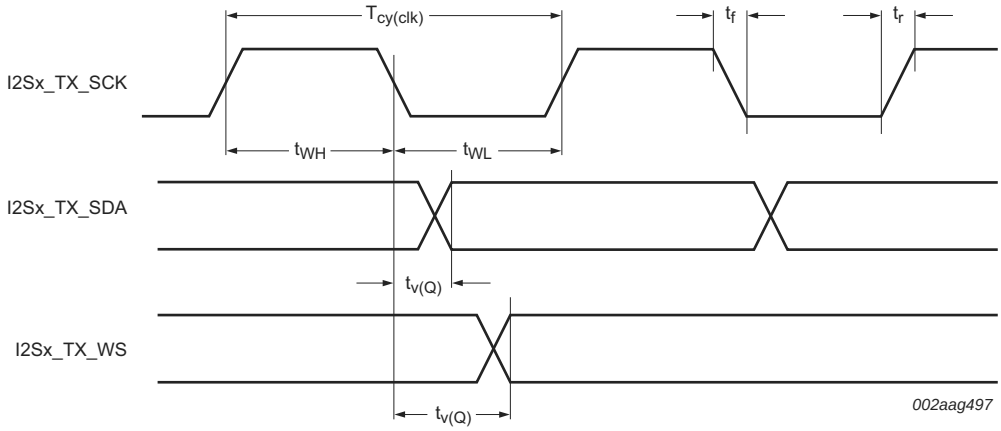


Fig 25. I²S-bus timing (transmit)

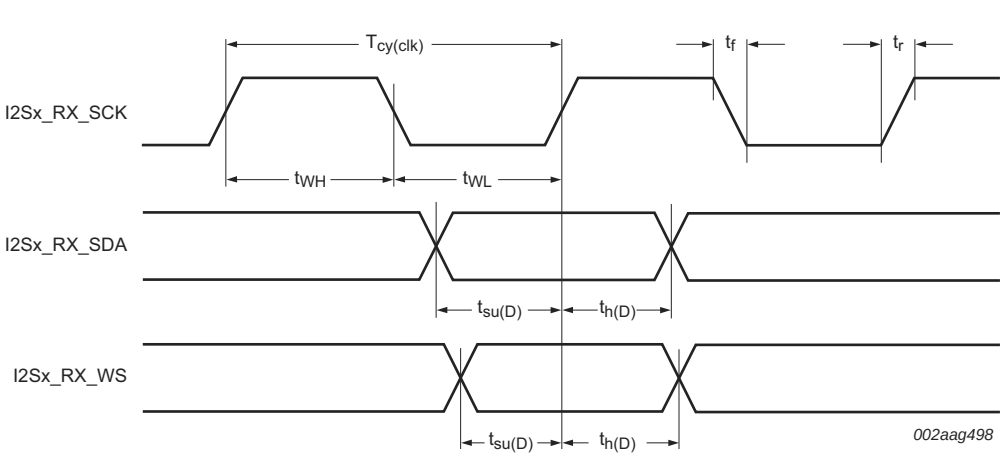


Fig 26. I²S-bus timing (receive)

11.10 USART interface

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	26.6	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	0	8.8	ns

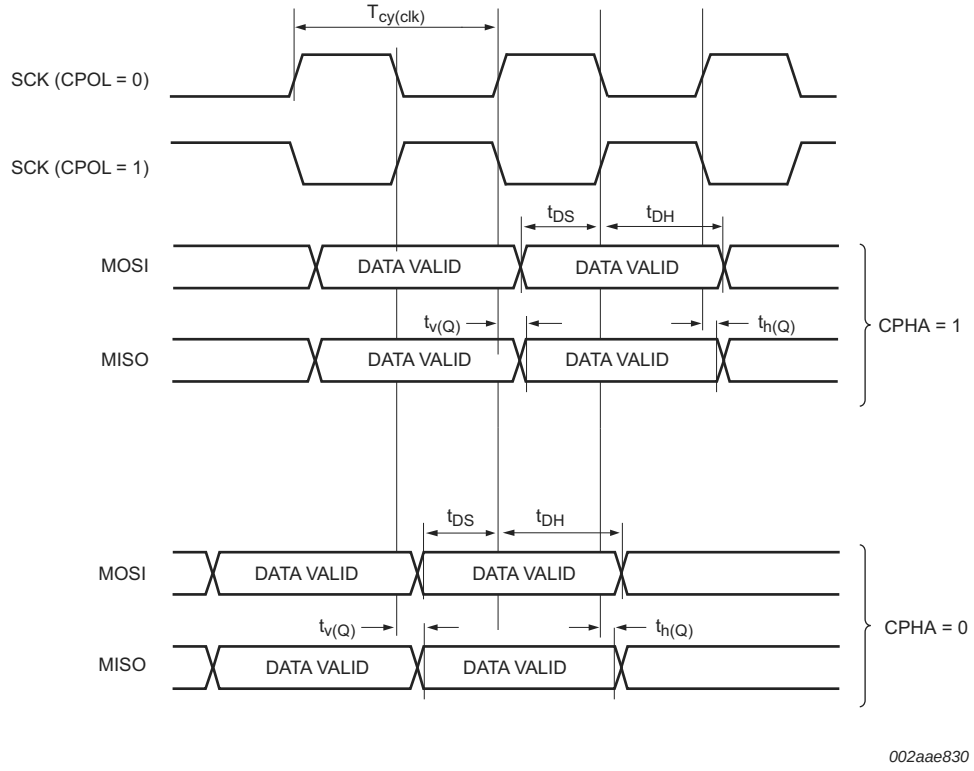


Fig 29. SSP slave timing in SPI mode

Table 28. Dynamic characteristics: SGPIO

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(D)}$	data input set-up time			2	-	-	ns
$t_{h(D)}$	data input hold time		[1]	T_{SGPIO} + 2	-	-	ns
$t_{su(D)}$	data input set-up time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{h(D)}$	data input hold time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{v(Q)}$	data output valid time		[1]	-	-	2 x T_{SGPIO}	ns
$t_{h(Q)}$	data output hold time		[1]	T_{SGPIO}	-		ns
$t_{v(Q)}$	data output valid time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns
$t_{h(Q)}$	data output hold time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns

[1] SGPIO_CLOCK is the internally generated SGPIO clock. $T_{SGPIO} = 1/f_{SGPIO\_CLOCK}$.

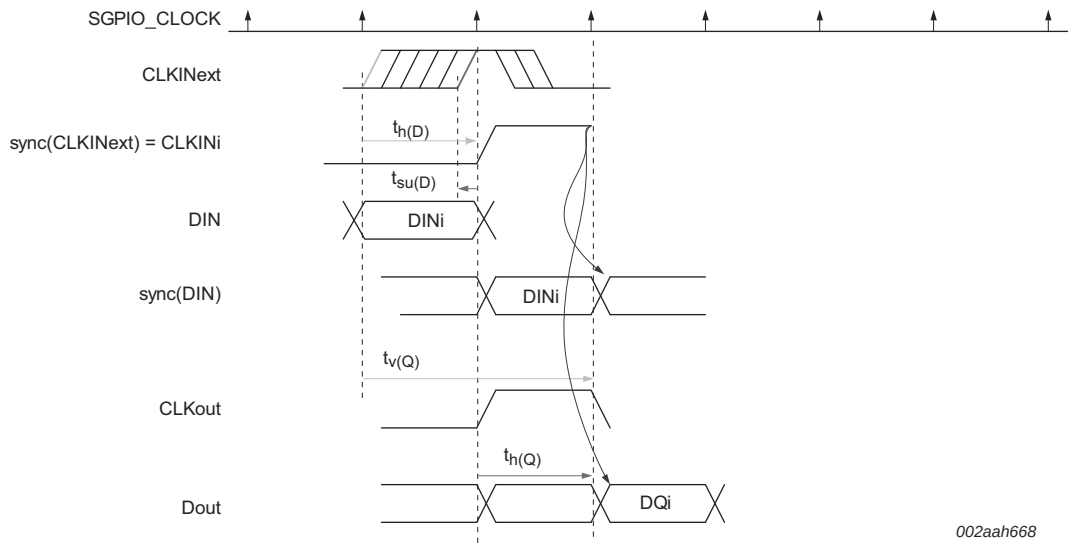


Fig 31. SGPIO timing

11.19 SD/MMC

Table 35. Dynamic characteristics: SD/MMC

T_{amb} = −40 °C to 85 °C, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, C_L = 20 pF. SAMPLE_DELAY = 0x9, DRV_DELAY = 0xD in the SDDELAY register sampled at 90 % and 10 % of the signal level, EHS = 1 for SD_CLK pin, EHS = 1 for SD_DATn and SD_CMD pins. Simulated values.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode		52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	3.9	-	ns
		on pins SD_CMD as inputs	5.2	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0.4	-	ns
		on pins SD_CMD as inputs	0		ns
$t_{d(QV)}$	data output valid delay time	on pins SD_DATn as outputs	-	15.3	ns
		on pins SD_CMD as outputs	-	16	ns
$t_{h(Q)}$	data output hold time	on pins SD_DATn as outputs	4	-	ns
		on pins SD_CMD as outputs	4	-	ns

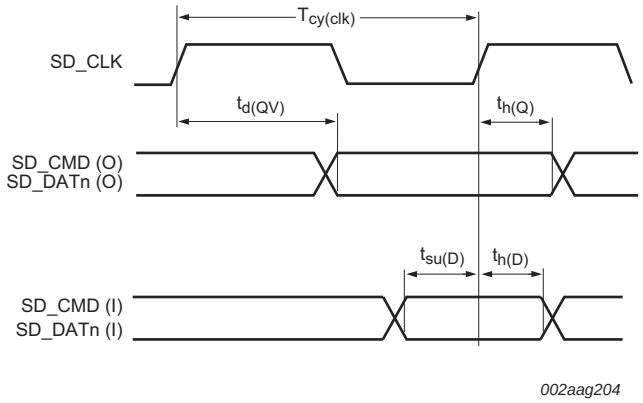


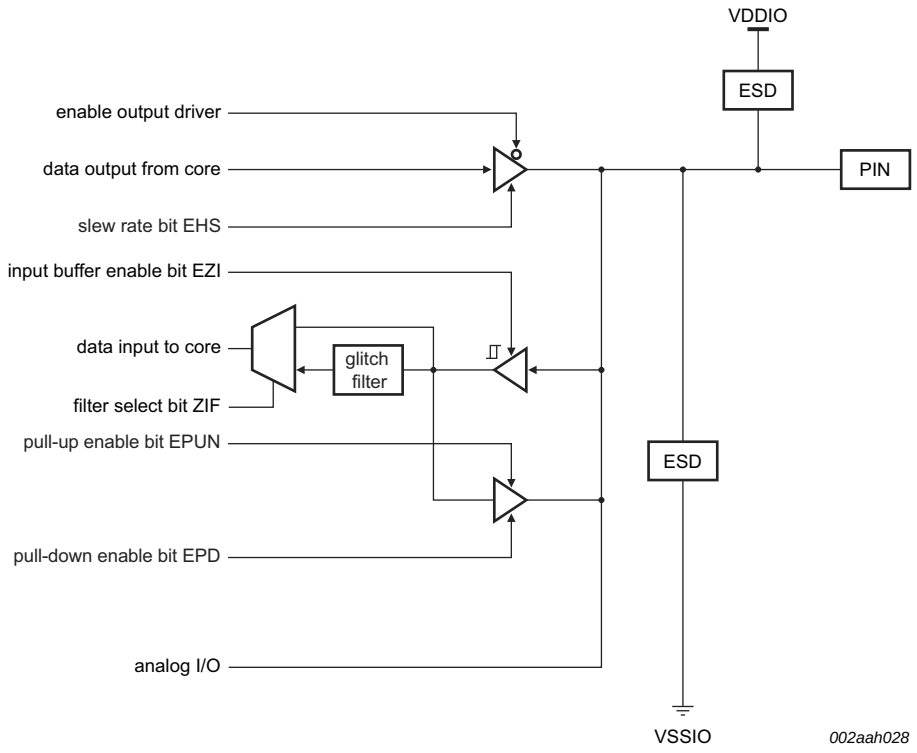
Fig 37. SD/MMC timing

11.20 LCD

Table 36. Dynamic characteristics: LCD

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	-	MHz
$t_{d(QV)}$	data output valid delay time			-	17	ns
$t_{h(Q)}$	data output hold time		8.5	-		ns



The glitch filter rejects pulses of typical 12 ns width.

Fig 43. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

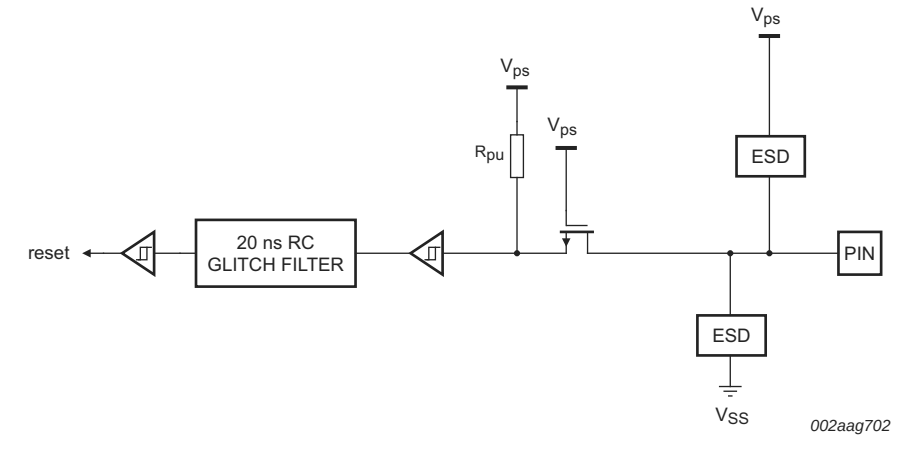


Fig 44. Reset pin configuration

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 45) or bus-powered device (see Figure 46).

On the LPC43S70, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

VDDIO = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See Figure 46.

Remark: Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.

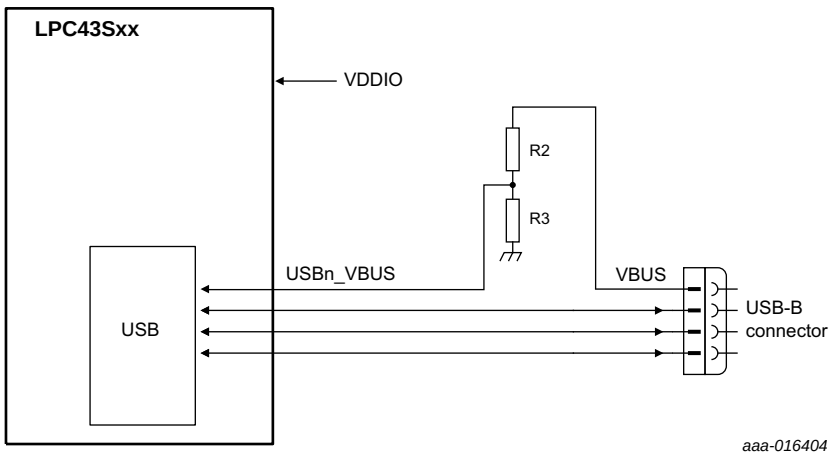


Fig 45. USB interface on a self-powered device where USBn_VBUS = 5 V

16. Abbreviations

Table 46. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DC-DC	Direct Current-to-Direct Current
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PMC	Power Mode Control
PWM	Pulse Width Modulator
RIT	Repetitive Interrupt Timer
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SIMD	Single Instruction Multiple Data
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB2.0 Transceiver Macrocell Interface