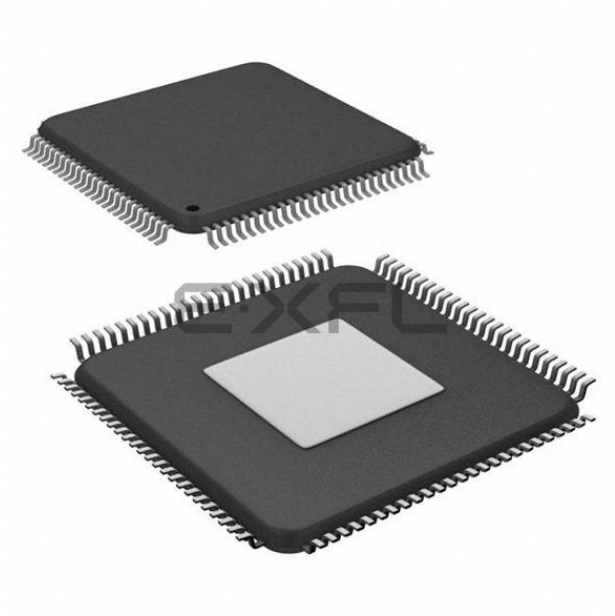
# Infineon Technologies - XC2764X40F80LRABKXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | C166SV2 |
| Core Size | 16/32-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 76 |
| Program Memory Size | 320KB (320K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 34K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-100-8 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xc2764x40f80lrabkxuma1 |

- On-Chip Peripheral Modules
  - Two synchronizable A/D Converters with up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - 4 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with 64 message objects (Full CAN/Basic CAN) on up to 2 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes
- Programmable watchdog timer and oscillator watchdog
- Up to 76 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

**Ordering Information**

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the temperature range:
  - SAF-…: -40°C to 85°C
  - SAH-…: -40°C to 110°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC2764X please contact your sales representative or local distributor.

# 2 General Device Information

The XC2764X series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

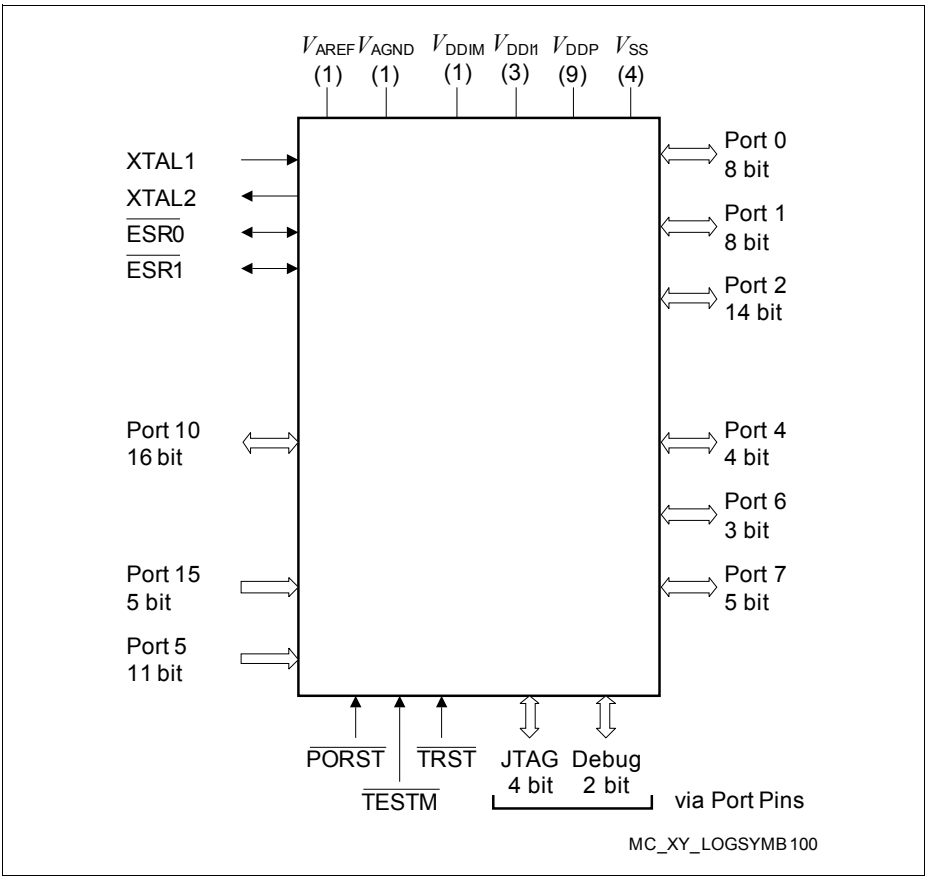


**Figure 2 XC2764X Logic Symbol**

## 2.1 Pin Configuration and Definition

The pins of the XC2764X are described in detail in **Table 5**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

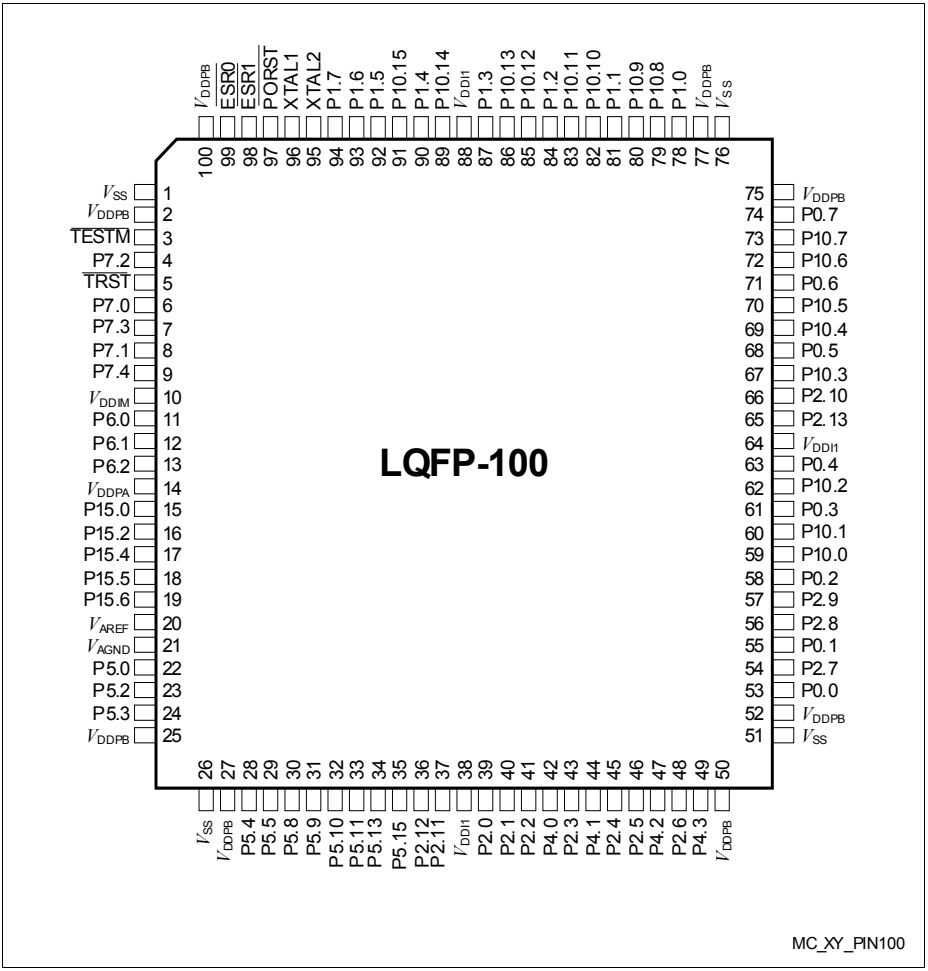


**Figure 3 XC2764X Pin Configuration (top view)**

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 31 | P5.9 | I | In/A | **Bit 9 of Port 5, General Purpose Input** |
| | ADC0_CH9 | I | In/A | **Analog Input Channel 9 for ADC0** |
| | ADC1_CH9 | I | In/A | **Analog Input Channel 9 for ADC1** |
| | CC2_T7IN | I | In/A | **CAPCOM2 Timer T7 Count Input** |
| 32 | P5.10 | I | In/A | **Bit 10 of Port 5, General Purpose Input** |
| | ADC0_CH10 | I | In/A | **Analog Input Channel 10 for ADC0** |
| | ADC1_CH10 | I | In/A | **Analog Input Channel 10 for ADC1** |
| | $\overline{\text{BRKIN\_A}}$ | I | In/A | **OCDS Break Signal Input** |
| | CCU61_T13HRA | I | In/A | **External Run Control Input for T13 of CCU61** |
| 33 | P5.11 | I | In/A | **Bit 11 of Port 5, General Purpose Input** |
| | ADC0_CH11 | I | In/A | **Analog Input Channel 11 for ADC0** |
| | ADC1_CH11 | I | In/A | **Analog Input Channel 11 for ADC1** |
| 34 | P5.13 | I | In/A | **Bit 13 of Port 5, General Purpose Input** |
| | ADC0_CH13 | I | In/A | **Analog Input Channel 13 for ADC0** |
| 35 | P5.15 | I | In/A | **Bit 15 of Port 5, General Purpose Input** |
| | ADC0_CH15 | I | In/A | **Analog Input Channel 15 for ADC0** |
| 36 | P2.12 | O0 / I | St/B | **Bit 12 of Port 2, General Purpose Input/Output** |
| | U0C0_SELO4 | O1 | St/B | **USIC0 Channel 0 Select/Control 4 Output** |
| | U0C1_SELO3 | O2 | St/B | **USIC0 Channel 1 Select/Control 3 Output** |
| | READY | IH | St/B | **External Bus Interface READY Input** |
| 37 | P2.11 | O0 / I | St/B | **Bit 11 of Port 2, General Purpose Input/Output** |
| | U0C0_SELO2 | O1 | St/B | **USIC0 Channel 0 Select/Control 2 Output** |
| | U0C1_SELO2 | O2 | St/B | **USIC0 Channel 1 Select/Control 2 Output** |
| | $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ | OH | St/B | **External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{\text{BHE}}$) or as Write strobe for High Byte ($\overline{\text{WRH}}$). |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 39 | P2.0 | O0 / I | St/B | **Bit 0 of Port 2, General Purpose Input/Output** |
| | AD13 | OH / IH | St/B | **External Bus Interface Address/Data Line 13** |
| | RxDC0C | I | St/B | **CAN Node 0 Receive Data Input** |
| | T5INB | I | St/B | **GPT12E Timer T5 Count/Gate Input** |
| 40 | P2.1 | O0 / I | St/B | **Bit 1 of Port 2, General Purpose Input/Output** |
| | TxDC0 | O1 | St/B | **CAN Node 0 Transmit Data Output** |
| | AD14 | OH / IH | St/B | **External Bus Interface Address/Data Line 14** |
| | T5EUDB | I | St/B | **GPT12E Timer T5 External Up/Down Control Input** |
| | ESR1_5 | I | St/B | **ESR1 Trigger Input 5** |
| 41 | P2.2 | O0 / I | St/B | **Bit 2 of Port 2, General Purpose Input/Output** |
| | TxDC1 | O1 | St/B | **CAN Node 1 Transmit Data Output** |
| | AD15 | OH / IH | St/B | **External Bus Interface Address/Data Line 15** |
| | ESR2_5 | I | St/B | **ESR2 Trigger Input 5** |
| 42 | P4.0 | O0 / I | St/B | **Bit 0 of Port 4, General Purpose Input/Output** |
| | CC2_CC24 | O3 / I | St/B | **CAPCOM2 CC24IO Capture Inp./ Compare Out.** |
| | $\overline{CS0}$ | OH | St/B | **External Bus Interface Chip Select 0 Output** |
| 43 | P2.3 | O0 / I | St/B | **Bit 3 of Port 2, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CC2_CC16 | O3 / I | St/B | **CAPCOM2 CC16IO Capture Inp./ Compare Out.** |
| | A16 | OH | St/B | **External Bus Interface Address Line 16** |
| | ESR2_0 | I | St/B | **ESR2 Trigger Input 0** |
| | U0C0_DX0E | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX0D | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | RxDC0A | I | St/B | **CAN Node 0 Receive Data Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 57 | P2.9 | O0 / I | St/B | **Bit 9 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | CC2_CC22 | O3 / I | St/B | **CAPCOM2 CC22IO Capture Inp./ Compare Out.** |
| | A22 | OH | St/B | **External Bus Interface Address Line 22** |
| | CLKIN1 | I | St/B | **Clock Signal Input 1** |
| | TCK_A | IH | St/B | **DAP0/JTAG Clock Input**<br>If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.<br>If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| 58 | P0.2 | O0 / I | St/B | **Bit 2 of Port 0, General Purpose Input/Output** |
| | U1C0_SCLKOUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CCU61_CC62 | O3 | St/B | **CCU61 Channel 2 Output** |
| | A2 | OH | St/B | **External Bus Interface Address Line 2** |
| | U1C0_DX1B | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | CCU61_CC62INA | I | St/B | **CCU61 Channel 2 Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 62 | P10.2 | O0 / I | St/B | **Bit 2 of Port 10, General Purpose Input/Output** |
| | U0C0_SCLKOUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | CCU60_CC62 | O2 | St/B | **CCU60 Channel 2 Output** |
| | AD2 | OH / IH | St/B | **External Bus Interface Address/Data Line 2** |
| | CCU60_CC62INA | I | St/B | **CCU60 Channel 2 Input** |
| | U0C0_DX1B | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| 63 | P0.4 | O0 / I | St/B | **Bit 4 of Port 0, General Purpose Input/Output** |
| | U1C1_SELO0 | O1 | St/B | **USIC1 Channel 1 Select/Control 0 Output** |
| | U1C0_SELO1 | O2 | St/B | **USIC1 Channel 0 Select/Control 1 Output** |
| | CCU61_COUT61 | O3 | St/B | **CCU61 Channel 1 Output** |
| | A4 | OH | St/B | **External Bus Interface Address Line 4** |
| | U1C1_DX2A | I | St/B | **USIC1 Channel 1 Shift Control Input** |
| | RxDC1B | I | St/B | **CAN Node 1 Receive Data Input** |
| | ESR2_8 | I | St/B | **ESR2 Trigger Input 8** |
| 65 | P2.13 | O0 / I | St/B | **Bit 13 of Port 2, General Purpose Input/Output** |
| 66 | P2.10 | O0 / I | St/B | **Bit 10 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_SELO3 | O2 | St/B | **USIC0 Channel 0 Select/Control 3 Output** |
| | CC2_CC23 | O3 / I | St/B | **CAPCOM2 CC23IO Capture Inp./ Compare Out.** |
| | A23 | OH | St/B | **External Bus Interface Address Line 23** |
| | U0C1_DX0E | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | CAPINA | I | St/B | **GPT12E Register CAPREL Capture Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 70 | P10.5 | O0 / I | St/B | **Bit 5 of Port 10, General Purpose Input/Output** |
| | U0C1_SCLKOUT | O1 | St/B | **USIC0 Channel 1 Shift Clock Output** |
| | CCU60_COUT62 | O2 | St/B | **CCU60 Channel 2 Output** |
| | AD5 | OH / IH | St/B | **External Bus Interface Address/Data Line 5** |
| | U0C1_DX1B | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| 71 | P0.6 | O0 / I | St/B | **Bit 6 of Port 0, General Purpose Input/Output** |
| | U1C1_DOUT | O1 | St/B | **USIC1 Channel 1 Shift Data Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | CCU61_COUT63 | O3 | St/B | **CCU61 Channel 3 Output** |
| | A6 | OH | St/B | **External Bus Interface Address Line 6** |
| | U1C1_DX0A | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | CCU61_CTRAPA | I | St/B | **CCU61 Emergency Trap Input** |
| | U1C1_DX1B | I | St/B | **USIC1 Channel 1 Shift Clock Input** |
| 72 | P10.6 | O0 / I | St/B | **Bit 6 of Port 10, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | U1C0_SELO0 | O3 | St/B | **USIC1 Channel 0 Select/Control 0 Output** |
| | AD6 | OH / IH | St/B | **External Bus Interface Address/Data Line 6** |
| | U0C0_DX0C | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U1C0_DX2D | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | CCU60_CTRAPA | I | St/B | **CCU60 Emergency Trap Input** |

With this hardware most XC2764X instructions are executed in a single machine cycle of 12.5 ns @ 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XC2764X instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

## 3.6 Interrupt System

The architecture of the XC2764X supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC2764X has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XC2764X can react quickly to the occurrence of non-deterministic events.

### Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

### External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

### Trap Processing

The XC2764X provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

## 3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

*Note: The number of CAN nodes and message objects depends on the selected device type.*

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

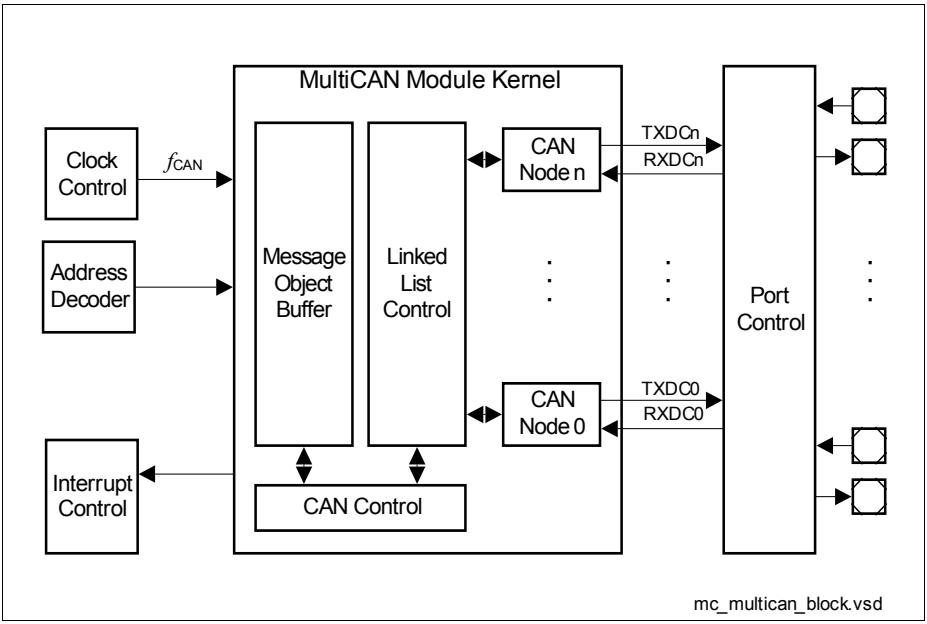


**Figure 12 Block Diagram of MultiCAN Module**

**MultiCAN Features**

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

## 3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

## 3.16 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 µs and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

## 3.18 Parallel Ports

The XC2764X provides up to 76 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 9**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

**Table 9 Summary of the XC2764X's Ports**

| Port | Width | I/O | Connected Modules |
|---|---|---|---|
| P0 | 8 | I/O | EBC (A7...A0), CCU6, USIC, CAN |
| P1 | 8 | I/O | EBC (A15...A8), CCU6, USIC |
| P2 | 14 | I/O | EBC (READY, $\overline{\text{BHE}}$, A23...A16, AD15...AD13, D15...D13), CAN, CC2, GPT12E, USIC, DAP/JTAG |
| P4 | 4 | I/O | EBC ($\overline{\text{CS3}}$...$\overline{\text{CS0}}$), CC2, CAN, GPT12E, USIC |
| P5 | 11 | I | Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN |
| P6 | 3 | I/O | ADC, CAN, GPT12E |
| P7 | 5 | I/O | CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC |
| P10 | 16 | I/O | EBC (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD12...AD0, D12...D0), CCU6, USIC, DAP/JTAG, CAN |
| P15 | 5 | I | Analog Inputs, GPT12E |

### 4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC2764X. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

*Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.*

**Table 12 Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Voltage Regulator Buffer Capacitance for DMP_M | $C_{EVRM}$ SR | 1.0 | – | 4.7 | µF | [1] |
| Voltage Regulator Buffer Capacitance for DMP_1 | $C_{EVR1}$ SR | 0.47 | – | 2.2 | µF | [2][1] |
| External Load Capacitance | $C_L$ SR | – | 20[3] | – | pF | pin out driver= default [4] |
| System frequency | $f_{SYS}$ SR | – | – | 80 | MHz | [5] |
| Overload current for analog inputs[6] | $I_{OVA}$ SR | -2 | – | 5 | mA | not subject to production test |
| Overload current for digital inputs[6] | $I_{OVD}$ SR | -5 | – | 5 | mA | not subject to production test |
| Overload current coupling factor for analog inputs[7] | $K_{OVA}$ CC | – | $2.5 \times 10^{-4}$ | $1.5 \times 10^{-3}$ | - | $I_{OV}$< 0 mA; not subject to production test |
| | | – | $1.0 \times 10^{-6}$ | $1.0 \times 10^{-4}$ | - | $I_{OV}$> 0 mA; not subject to production test |

**Table 16 DC Characteristics for Lower Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output High voltage[7] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \geq I_{OHmax}$ |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq I_{OHnom}$ [8] |
| Output Low Voltage[7] | $V_{OL}$ CC | – | – | 0.4 | V | $I_{OL} \leq I_{OLnom}$ [8] |
| | | – | – | 1.0 | V | $I_{OL} \leq I_{OLmax}$ |

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature ($T_J$ = junction temperature [°C]): $I_{OZ}$ = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = $V_{DDP}$ - $V_{PIN}$ [V]): $I_{OZ}$ = $I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} <= V_{IL}$ for a pullup; $V_{PIN} >= V_{IH}$ for a pulldown.

6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} >= V_{IH}$ for a pullup; $V_{PIN} <= V_{IL}$ for a pulldown.

7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

8) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL}$->$V_{SS}$, $V_{OH}$->$V_{DDP}$). However, only the levels for nominal output currents are verified.

**Table 31 External Bus Timing for Upper Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Address output valid delay for AD15 ... AD0 (MUX mode) | $t_{13}$ CC | – | 8 | 15 | ns | |
| Output valid delay for $\overline{CS}$ | $t_{14}$ CC | – | 7 | 13 | ns | |
| Data output valid delay for AD15 ... AD0 (write data, MUX mode) | $t_{15}$ CC | – | 8 | 15 | ns | |
| Data output valid delay for D15 ... D0 (write data, DEMUX mode) | $t_{16}$ CC | – | 8 | 15 | ns | |
| Output hold time for $\overline{RD}$, $\overline{WR}$($\overline{L}$/$\overline{H}$) | $t_{20}$ CC | -2 | 6 | 8 | ns | |
| Output hold time for $\overline{BHE}$, ALE | $t_{21}$ CC | -2 | 6 | 10 | ns | |
| Address output hold time for AD15 ... AD0 | $t_{23}$ CC | -3 | 6 | 8 | ns | |
| Output hold time for $\overline{CS}$ | $t_{24}$ CC | -3 | 6 | 11 | ns | |
| Data output hold time for D15 ... D0 and AD15 ... AD0 | $t_{25}$ CC | -3 | 6 | 8 | ns | |
| Input setup time for READY, D15 ... D0, AD15 ... AD0 | $t_{30}$ SR | 25 | 15 | – | ns | |
| Input hold time READY, D15 ... D0, AD15 ... AD0[1)] | $t_{31}$ SR | 0 | -7 | – | ns | |

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

**Table 32** is valid under the following conditions: $C_L$= 20 pF; voltage_range= lower ; voltage_range= lower

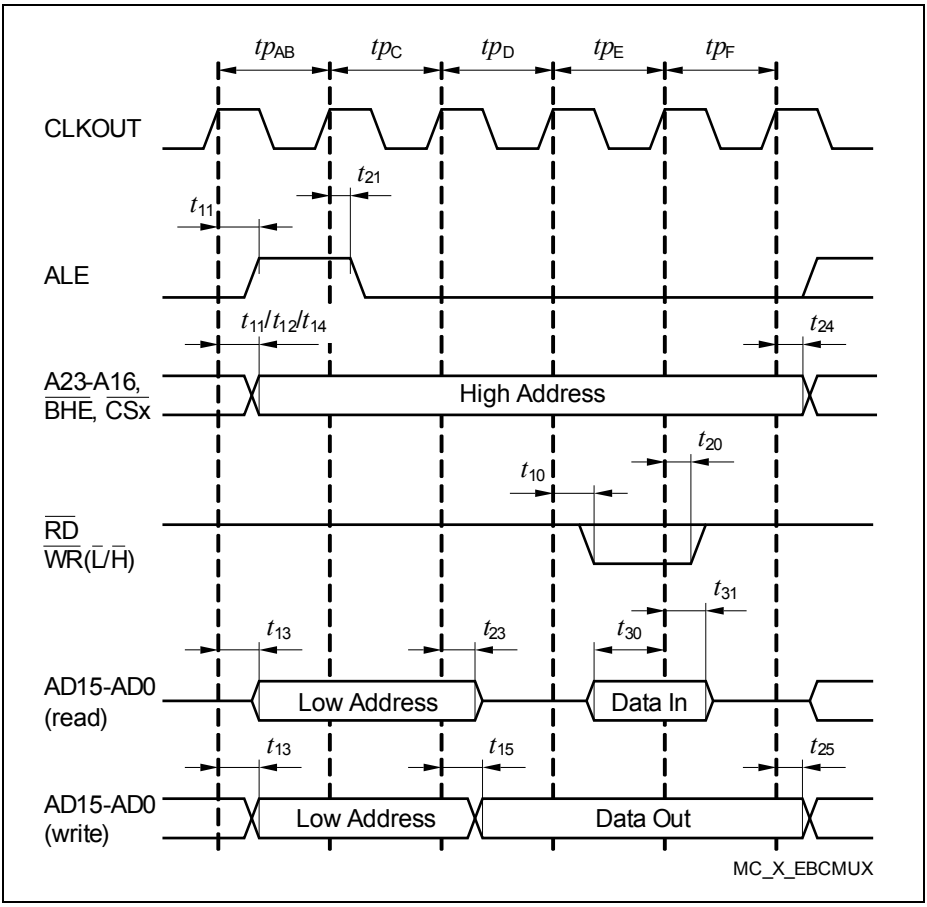


**Figure 23 Multiplexed Bus Cycle**

**Table 35 USIC SSC Slave Mode Timing for Upper Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Data input DX0 hold time from clock input DX1 receive edge[1)] | $t_{13}$ SR | 5 | – | – | ns | |
| Data output DOUT valid time | $t_{14}$ CC | 7 | – | 33 | ns | |

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

**Table 36** is valid under the following conditions: $C_L$= 20 pF; $SSC$= slave ; voltage_range= lower

**Table 36 USIC SSC Slave Mode Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Select input DX2 setup to first clock input DX1 transmit edge[1)] | $t_{10}$ SR | 7 | – | – | ns | |
| Select input DX2 hold after last clock input DX1 receive edge[1)] | $t_{11}$ SR | 7 | – | – | ns | |
| Receive data input setup time to shift clock receive edge[1)] | $t_{12}$ SR | 7 | – | – | ns | |
| Data input DX0 hold time from clock input DX1 receive edge[1)] | $t_{13}$ SR | 5 | – | – | ns | |
| Data output DOUT valid time | $t_{14}$ CC | 8 | – | 41 | ns | |

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

# 5 Package and Reliability

The XC2000 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XC2764X in its target environment.

## 5.1 Packaging

These parameters specify the packaging rather than the silicon.

**Table 41 Package Parameters (PG-LQFP-100-8)**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Exposed Pad Dimension | Ex × Ey | – | 5.2 × 5.2 | mm | – |
| Power Dissipation | $P_{DISS}$ | – | 0.8 | W | – |
| Thermal resistance Junction-Ambient | $R_{\Theta JA}$ | – | 54 | K/W | No thermal via[1)] |
| | | | 49 | K/W | 4-layer, no pad[2)] |
| | | | 27 | K/W | 4-layer, pad[3)] |

1) Device mounted on a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

*Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.*
*Board layout examples are given in an application note.*

### Package Compatibility Considerations

The XC2764X is a member of the XC2000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

## 5.3 Quality Declarations

The operation lifetime of the XC2764X depends on the applied temperature profile in the application. For a typical example, please refer to **Table 43**; for other profiles, please contact your Infineon counterpart to calculate the specific lifetime within your application.

**Table 42 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation lifetime | $t_{OP}$ CC | – | – | 20 | a | See **Table 43** and **Table 44** |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | – | – | 2 000 | V | EIA/JESD22-A114-B |
| Moisture sensitivity level | MSL CC | – | – | 3 | – | JEDEC J-STD-020C |

**Table 43 Typical Usage Temperature Profile**

| Operating Time (Sum = 20 years) | Operating Temperat. | Notes |
|---|---|---|
| 1 200 h | $T_J$ = 150°C | Normal operation |
| 3 600 h | $T_J$ = 125°C | Normal operation |
| 7 200 h | $T_J$ = 110°C | Normal operation |
| 12 000 h | $T_J$ = 100°C | Normal operation |
| 7 × 21 600 h | $T_J$ = 0…10°C, …, 60…70°C | Power reduction |

**Table 44 Long Time Storage Temperature Profile**

| Operating Time (Sum = 20 years) | Operating Temperat. | Notes |
|---|---|---|
| 2 000 h | $T_J$ = 150°C | Normal operation |
| 16 000 h | $T_J$ = 125°C | Normal operation |
| 6 000 h | $T_J$ = 110°C | Normal operation |
| 151 200 h | $T_J \leq$ 150°C | No operation |