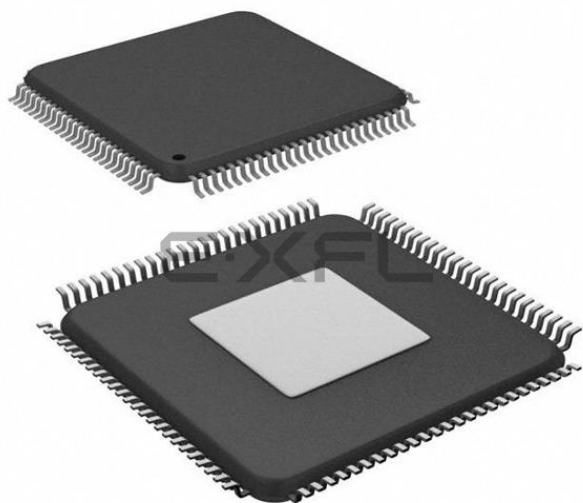




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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	26K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc2265n-24f40l-aa

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	TXDC4	O2	St/B	CAN Node 4 Transmit Data Output
	BRKIN_C	I	St/B	OCDS Break Signal Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
9	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_SCLK OUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	TCK_C	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input
11	P6.0	O0 / I	DA/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	DA/A	External Analog MUX Control Output 0 (ADC0)
	TxDC2	O2	DA/A	CAN Node 2 Transmit Data Output
	BRKOUT	O3	DA/A	OCDS Break Signal Output
	ADCx_REQG TyG	I	DA/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	DA/A	USIC1 Channel 1 Shift Data Input
12	P6.1	O0 / I	DA/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	DA/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	DA/A	USIC1 Channel 1 Shift Data Output
	ADCx_REQT RyE	I	DA/A	External Request Trigger Input for ADC0/1
	RxDC2E	I	DA/A	CAN Node 2 Receive Data Input
	ESR1_6	I	DA/A	ESR1 Trigger Input 6

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
24	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3INA	I	In/A	GPT12E Timer T3 Count/Gate Input
28	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
29	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12 HRB	I	In/A	External Run Control Input for T12 of CCU60
30	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	ADC1_CH8	I	In/A	Analog Input Channel 8 for ADC1
	CCU6x_T12H RC	I	In/A	External Run Control Input for T12 of CCU60/1
	CCU6x_T13H RC	I	In/A	External Run Control Input for T13 of CCU60/1
	U2C0_DX0F	I	In/A	USIC2 Channel 0 Shift Data Input
31	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	ADC1_CH9	I	In/A	Analog Input Channel 9 for ADC1
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input
32	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	ADC1_CH10	I	In/A	Analog Input Channel 10 for ADC1
	BRKIN_A	I	In/A	OCDS Break Signal Input
	U2C1_DX0F	I	In/A	USIC2 Channel 1 Shift Data Input
	CCU61_T13 HRA	I	In/A	External Run Control Input for T13 of CCU61

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
33	P5.11	I	In/A	Bit 11 of Port 5, General Purpose Input
	ADC0_CH11	I	In/A	Analog Input Channel 11 for ADC0
	ADC1_CH11	I	In/A	Analog Input Channel 11 for ADC1
34	P5.13	I	In/A	Bit 13 of Port 5, General Purpose Input
	ADC0_CH13	I	In/A	Analog Input Channel 13 for ADC0
35	P5.15	I	In/A	Bit 15 of Port 5, General Purpose Input
	ADC0_CH15	I	In/A	Analog Input Channel 15 for ADC0
	RxDC2F	I	In/A	CAN Node 2 Receive Data Input
36	P2.12	O0 / I	St/B	Bit 12 of Port 2, General Purpose Input/Output
	U0C0_SELO 4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_SELO 3	O2	St/B	USIC0 Channel 1 Select/Control 3 Output
	TXDC2	O3	St/B	CAN Node 2 Transmit Data Output
	READY	IH	St/B	External Bus Interface READY Input
37	P2.11	O0 / I	St/B	Bit 11 of Port 2, General Purpose Input/Output
	U0C0_SELO 2	O1	St/B	USIC0 Channel 0 Select/Control 2 Output
	U0C1_SELO 2	O2	St/B	USIC0 Channel 1 Select/Control 2 Output
	BHE/WRH	OH	St/B	External Bus Interf. High-Byte Control Output Can operate either as Byte High Enable (BHE) or as Write strobe for High Byte (WRH).
39	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output
	TxDC5	O1	St/B	CAN Node 5 Transmit Data Output
	AD13	OH / IH	St/B	External Bus Interface Address/Data Line 13
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input
	T5INB	I	St/B	GPT12E Timer T5 Count/Gate Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
55	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC61	O3	St/B	CCU61 Channel 1 Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC61INA	I	St/B	CCU61 Channel 1 Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input
56	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output 1)
	CC2_CC21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input
57	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_CC22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input 1
	TCK_A	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
58	P0.2	O0 / I	St/B	Bit 2 of Port 0, General Purpose Input/Output
	U1C0_SCLK OUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC6 2	O3	St/B	CCU61 Channel 2 Output
	A2	OH	St/B	External Bus Interface Address Line 2
	U1C0_DX1B	I	St/B	USIC1 Channel 0 Shift Clock Input
	CCU61_CC6 2INA	I	St/B	CCU61 Channel 2 Input
59	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_CC6 0	O2	St/B	CCU60 Channel 0 Output
	AD0	OH / IH	St/B	External Bus Interface Address/Data Line 0
	CCU60_CC6 0INA	I	St/B	CCU60 Channel 0 Input
	ESR1_2	I	St/B	ESR1 Trigger Input 2
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input
60	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU60_CC6 1	O2	St/B	CCU60 Channel 1 Output
	AD1	OH / IH	St/B	External Bus Interface Address/Data Line 1
	CCU60_CC6 1INA	I	St/B	CCU60 Channel 1 Input
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P1.3	O0 / I	St/B	Bit 3 of Port 1, General Purpose Input/Output
	U1C0_SELO 7	O2	St/B	USIC1 Channel 0 Select/Control 7 Output
	U2C0_SELO 4	O3	St/B	USIC2 Channel 0 Select/Control 4 Output
	A11	OH	St/B	External Bus Interface Address Line 11
	ESR2_4	I	St/B	ESR2 Trigger Input 4
89	P10.14	O0 / I	St/B	Bit 14 of Port 10, General Purpose Input/Output
	U1C0_SELO 1	O1	St/B	USIC1 Channel 0 Select/Control 1 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	RD	OH	St/B	External Bus Interface Read Strobe Output
	ESR2_2	I	St/B	ESR2 Trigger Input 2
	U0C1_DX0C	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC3C	I	St/B	CAN Node 3 Receive Data Input
90	P1.4	O0 / I	St/B	Bit 4 of Port 1, General Purpose Input/Output
	U1C1_SELO 4	O2	St/B	USIC1 Channel 1 Select/Control 4 Output
	U2C0_SELO 5	O3	St/B	USIC2 Channel 0 Select/Control 5 Output
	A12	OH	St/B	External Bus Interface Address Line 12
	U2C0_DX2B	I	St/B	USIC2 Channel 0 Shift Control Input
	RxDC5A	I	St/B	CAN Node 5 Receive Data Input
91	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO 2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input

2.2 Identification Registers

The identification registers describe the current version of the XC226xN and of its modules.

Table 7 XC226xN Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820 _H	00'F07E _H	
SCU_IDCHIP	3001 _H	00'F07C _H	marking EES-AA or ES-AA
	3002 _H	00'F07C _H	marking AA, AB
SCU_IDMEM	304F _H	00'F07A _H	
SCU_IDPROG	1313 _H	00'F078 _H	
JTAG_ID	0018'B083 _H	---	marking EES-AA or ES-AA
	1018'B083 _H	---	marking AA, AB

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).

The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.

The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

3.17 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC226xN from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also [Section 4.7.2](#).

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

Electrical Parameters

4.3.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Note: Operating Conditions apply.

Table 17 is valid under the following conditions: $V_{DDP} \geq 3.0 \text{ V}$; $V_{DDP} \text{ typ. } 3.3 \text{ V}$; $V_{DDP} \leq 4.5 \text{ V}$

Table 17 DC Characteristics for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	$C_{IO} \text{ CC}$	–	–	10	pF	not subject to production test
Input Hysteresis ²⁾	$HYS \text{ CC}$	$0.07 \times V_{DDP}$	–	–	V	$R_S = 0 \text{ Ohm}$
Absolute input leakage current on pins of analog ports ³⁾	$ I_{OZ1} \text{ CC}$	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins. ³⁾¹⁾⁴⁾	$ I_{OZ2} \text{ CC}$	–	0.2	2.5	μA	$T_J \leq 110 \text{ }^\circ\text{C}$; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	8	μA	$T_J \leq 150 \text{ }^\circ\text{C}$; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current ⁵⁾	$ I_{PLF} \text{ SR}$	150	–	–	μA	$V_{IN} \geq V_{IHmin}(\text{pull down})$; $V_{IN} \leq V_{ILmax}(\text{pull up})$
Pull Level Keep Current ⁶⁾	$ I_{PLK} \text{ SR}$	–	–	10	μA	$V_{IN} \geq V_{IHmin}(\text{pull up})$; $V_{IN} \leq V_{ILmax}(\text{pull down})$
Input high voltage (all except XTAL1)	$V_{IH} \text{ SR}$	$0.7 \times V_{DDP}$	–	$V_{DDP} + 0.3$	V	
Input low voltage (all except XTAL1)	$V_{IL} \text{ SR}$	-0.3	–	$0.3 \times V_{DDP}$	V	

Electrical Parameters

Sample time and conversion time of the XC226xN's A/D converters are programmable. The timing above can be calculated using [Table 21](#).

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 21 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time¹⁾ t_s
000000 _B	f_{SYS}	00 _H	$t_{\text{ADCI}} \times 2$
000001 _B	$f_{\text{SYS}} / 2$	01 _H	$t_{\text{ADCI}} \times 3$
000010 _B	$f_{\text{SYS}} / 3$	02 _H	$t_{\text{ADCI}} \times 4$
:	$f_{\text{SYS}} / (\text{DIVA}+1)$	:	$t_{\text{ADCI}} \times (\text{STC}+2)$
111110 _B	$f_{\text{SYS}} / 63$	FE _H	$t_{\text{ADCI}} \times 256$
111111 _B	$f_{\text{SYS}} / 64$	FF _H	$t_{\text{ADCI}} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: $f_{\text{SYS}} = 80 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 12.5 \text{ ns}$), DIVA = 03_H, STC = 00_H

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 4 = 20 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 50 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 2 = 100 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 13 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 13 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.675 \text{ } \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 11 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 11 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.575 \text{ } \mu\text{s}$$

Converter Timing Example B:

Assumptions: $f_{\text{SYS}} = 40 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 25 \text{ ns}$), DIVA = 02_H, STC = 03_H

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 3 = 13.3 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 75 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 5 = 375 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 16 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 16 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.25 \text{ } \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 14 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 14 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.10 \text{ } \mu\text{s}$$

Electrical Parameters

- 2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.
- 3) Value of IMB_IMBCTRL.WSFLASH.
- 4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticeably only at extremely low system clock frequencies.

Access to the XC226xN Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.7.5 External Bus Timing

The following parameters specify the behavior of the XC226xN bus interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 30 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CLKOUT Cycle Time ¹⁾	t_5 CC	–	$1 / f_{SYS}$	–	ns	
CLKOUT high time	t_6 CC	3	–	–		
CLKOUT low time	t_7 CC	3	–	–		
CLKOUT rise time	t_8 CC	–	–	3	ns	
CLKOUT fall time	t_9 CC	–	–	3		

1) The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).

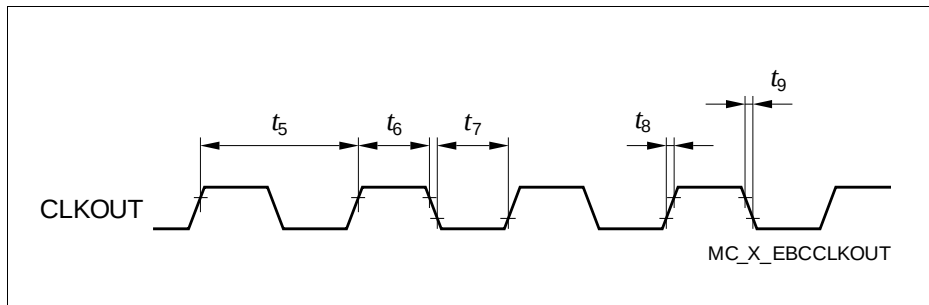


Figure 22 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

Electrical Parameters

Variable Memory Cycles

External bus cycles of the XC226xN are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 31 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 ... 2 TCS) can be extended by 0 ... 3 TCS if the address window is changed	tpAB	1 ... 2 (5)	TCS
Command delay phase	tpC	0 ... 3	TCS
Write Data setup/MUX Tristate phase	tpD	0 ... 1	TCS
Access phase	tpE	1 ... 32	TCS
Address/Write Data hold phase	tpF	0 ... 3	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Note: Operating Conditions apply.

Table 32 is valid under the following conditions: $C_L = 20 \text{ pF}$; voltage_range= upper ; voltage_range= upper

Table 32 External Bus Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{\text{RD}}$, $\overline{\text{WR}}(\text{L/H})$	$t_{10} \text{ CC}$	–	7	13	ns	
Output valid delay for $\overline{\text{BHE}}$, ALE	$t_{11} \text{ CC}$	–	7	14	ns	
Address output valid delay for A23 ... A0	$t_{12} \text{ CC}$	–	8	14	ns	

Table 33 External Bus Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, $\overline{WR(L/H)}$	t_{10} CC	–	11	20	ns	
Output valid delay for BHE, ALE	t_{11} CC	–	10	21	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	11	22	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	10	22	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	10	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	10	22	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	10	22	ns	
Output hold time for $\overline{RD}$, $\overline{WR(L/H)}$	t_{20} CC	-2	8	10	ns	
Output hold time for BHE, ALE	t_{21} CC	-2	8	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	8	10	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	8	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	8	10	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	29	17	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0 ¹⁾	t_{31} SR	0	-9	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

Electrical Parameters

duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command (RD or WR).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

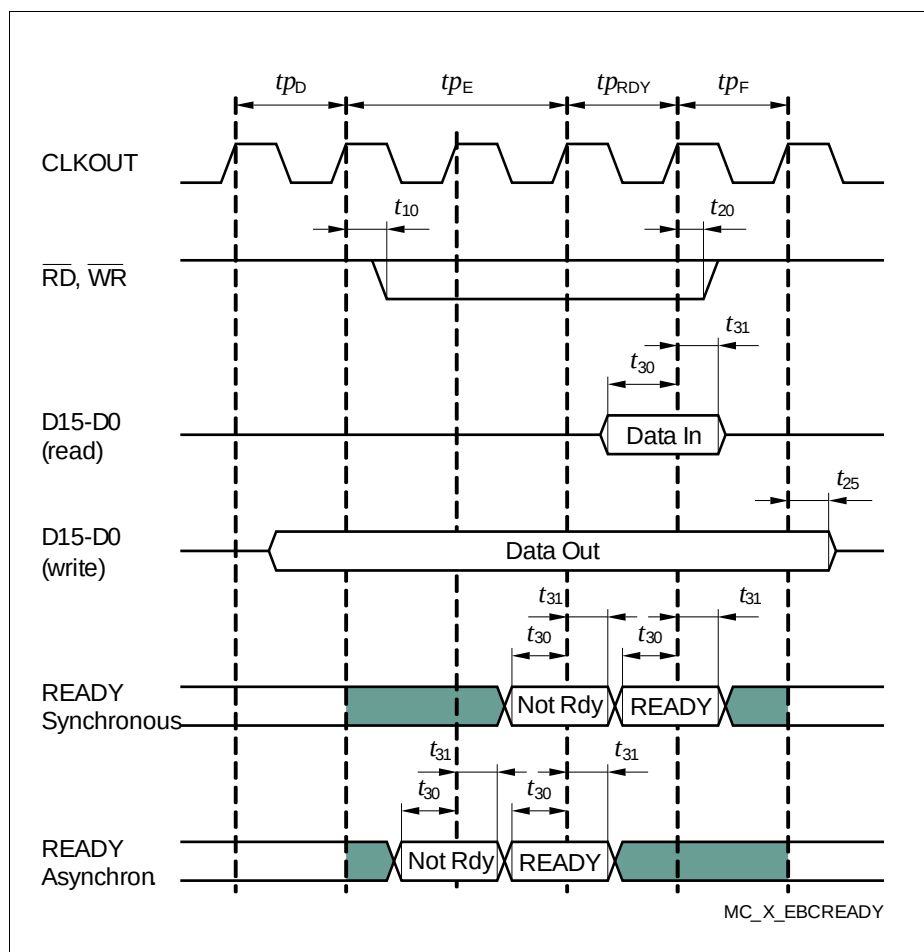


Figure 25 READY Timing

Electrical Parameters

Note: If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (t_{pRDY}), sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle.

*Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see t_{pE}) before the READY input value is used.*

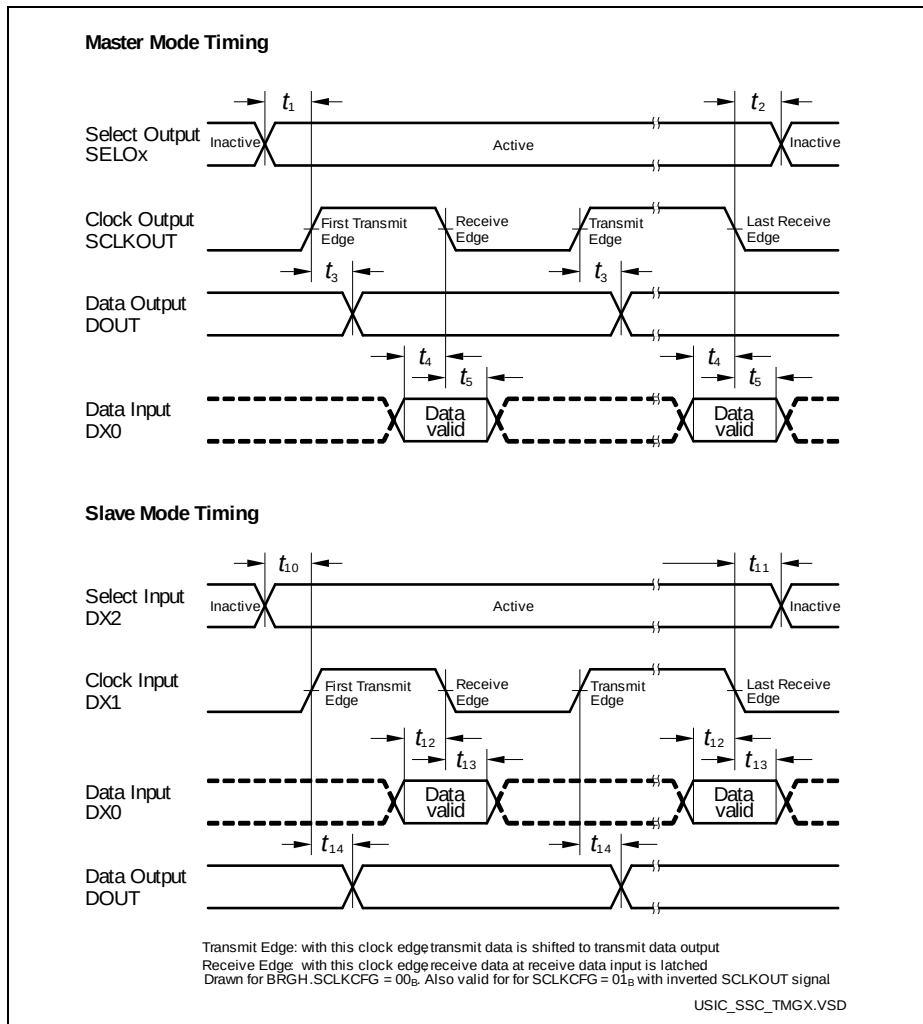


Figure 26 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

Electrical Parameters

Table 41 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	
TDO valid from TCK falling edge (propagation delay) ¹⁾	t_8 CC	—	32	36	ns	
TDO high impedance to valid output from TCK falling edge ²⁾¹⁾	t_9 CC	—	32	36	ns	
TDO valid output to high impedance from TCK falling edge ¹⁾	t_{10} CC	—	32	36	ns	
TDO hold after TCK falling edge ¹⁾	t_{18} CC	5	—	—	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

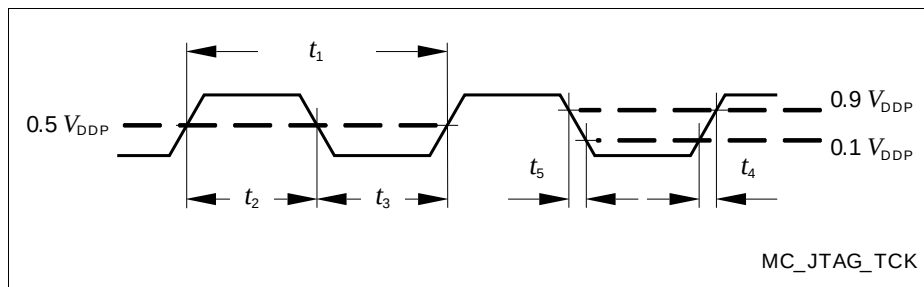


Figure 30 Test Clock Timing (TCK)