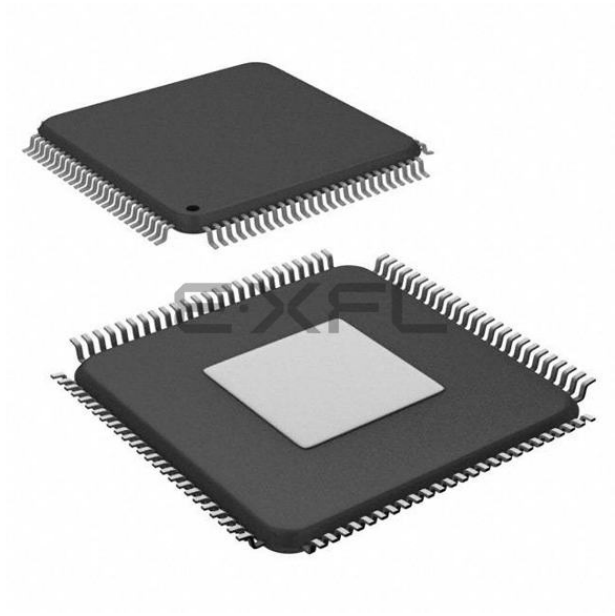
Infineon Technologies - XC2263N40F40LAAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	42K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2263n40f40laakxuma1

- On-Chip Peripheral Modules
  - Two synchronizable A/D Converters with up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 256 message objects (Full CAN/Basic CAN) on up to 6 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable watchdog timer and oscillator watchdog
- Up to 76 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (A, B, M, 1).
  - St: Standard pad
  - Sp: Special pad e.g. XTALx
  - DP: Double pad - can be used as standard or high speed pad
  - In: Input only pad
  - PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	**Bit 2 of Port 7, General Purpose Input/Output**
	EMUX0	O1	St/B	**External Analog MUX Control Output 0 (ADC1)**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	TxDC5	O3	St/B	**CAN Node 5 Transmit Data Output**
	TDI_C	IH	St/B	**JTAG Test Data Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
5	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC226xN's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
49	P4.3	O0 / I	St/B	**Bit 3 of Port 4, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CC2_CC27	O3 / I	St/B	**CAPCOM2 CC27IO Capture Inp./ Compare Out.**
	$\overline{CS3}$	OH	St/B	**External Bus Interface Chip Select 3 Output**
	RxDC2A	I	St/B	**CAN Node 2 Receive Data Input**
	T2EUDA	I	St/B	**GPT12E Timer T2 External Up/Down Control Input**
53	P0.0	O0 / I	St/B	**Bit 0 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	CCU61_CC60	O3	St/B	**CCU61 Channel 0 IOutput**
	A0	OH	St/B	**External Bus Interface Address Line 0**
	U1C0_DX0A	I	St/B	**USIC1 Channel 0 Shift Data Input**
	CCU61_CC60INA	I	St/B	**CCU61 Channel 0 Input**
	ESR1_11	I	St/B	**ESR1 Trigger Input 11**
54	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_SELO0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_SELO1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_CC20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	A20	OH	St/B	**External Bus Interface Address Line 20**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
	ESR2_7	I	St/B	**ESR2 Trigger Input 7**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
61	P0.3	O0 / I	St/B	**Bit 3 of Port 0, General Purpose Input/Output**
	U1C0_SELO 0	O1	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U1C1_SELO 1	O2	St/B	**USIC1 Channel 1 Select/Control 1 Output**
	CCU61_COU T60	O3	St/B	**CCU61 Channel 0 Output**
	A3	OH	St/B	**External Bus Interface Address Line 3**
	U1C0_DX2A	I	St/B	**USIC1 Channel 0 Shift Control Input**
	RxDC0B	I	St/B	**CAN Node 0 Receive Data Input**
62	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLK OUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC6 2	O2	St/B	**CCU60 Channel 2 Output**
	AD2	OH / IH	St/B	**External Bus Interface Address/Data Line 2**
	CCU60_CC6 2INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
63	P0.4	O0 / I	St/B	**Bit 4 of Port 0, General Purpose Input/Output**
	U1C1_SELO 0	O1	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C0_SELO 1	O2	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	CCU61_COU T61	O3	St/B	**CCU61 Channel 1 Output**
	A4	OH	St/B	**External Bus Interface Address Line 4**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**
	ESR2_8	I	St/B	**ESR2 Trigger Input 8**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
80	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_SELO 4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_MCLK OUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	AD9	OH / IH	St/B	**External Bus Interface Address/Data Line 9**
	CCU60_CCP OS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	T3INB	I	St/B	**GPT12E Timer T3 Count/Gate Input**
81	P1.1	O0 / I	St/B	**Bit 1 of Port 1, General Purpose Input/Output**
	U1C0_SELO 5	O2	St/B	**USIC1 Channel 0 Select/Control 5 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	A9	OH	St/B	**External Bus Interface Address Line 9**
	ESR2_3	I	St/B	**ESR2 Trigger Input 3**
	U2C1_DX0C	I	St/B	**USIC2 Channel 1 Shift Data Input**

3 Functional Description

The architecture of the XC226xN combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC226xN.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC226xN.

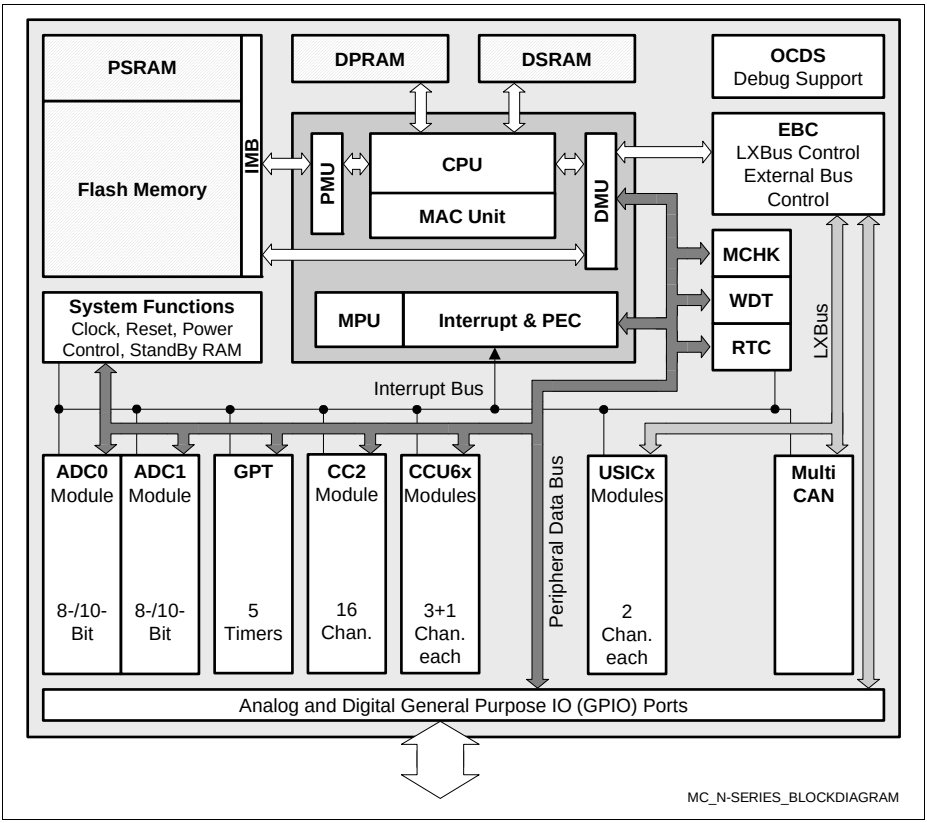

Figure 4 Block Diagram

3.6 Interrupt System

The architecture of the XC226xN supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC226xN has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XC226xN can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XC226xN provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

3.13 Universal Serial Interface Channel Modules (USIC)

The XC226xN features the USIC modules USIC0, USIC1, USIC2. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

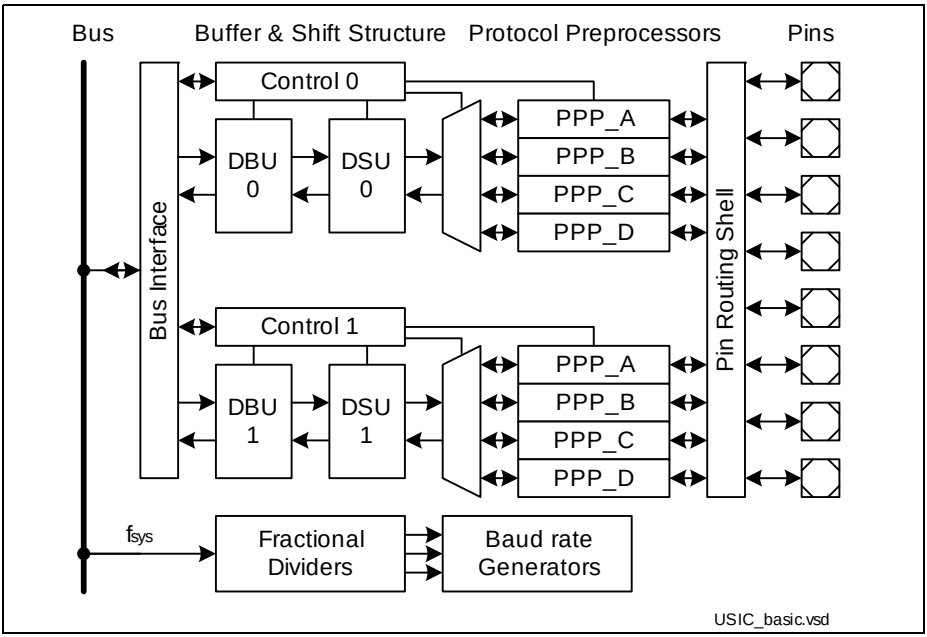

Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

3.17 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC226xN from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

3.19 Power Management

The XC226xN provides the means to control the power it consumes either at a given time or averaged over a certain duration.
Three mechanisms can be used (and partly in parallel):

- **Supply Voltage Management** permits the temporary reduction of the supply voltage of major parts of the logic or even its complete disconnection. This drastically reduces the power consumed because it eliminates leakage current, particularly at high temperature.
  Several power reduction modes provide the best balance of power reduction and wake-up time.
- **Clock Generation Management** controls the frequency of internal and external clock signals. Clock signals for currently inactive parts of logic are disabled automatically. The user can drastically reduce the consumed power by reducing the XC226xN system clock frequency.
  External circuits can be controlled using the programmable frequency output EXTCLK.
- **Peripheral Management** permits temporary disabling of peripheral modules. Each peripheral can be disabled and enabled separately. The CPU can be switched off while the peripherals can continue to operate.

Wake-up from power reduction modes can be triggered either externally with signals generated by the external system, or internally by the on-chip wake-up timer. This supports intermittent operation of the XC226xN by generating cyclic wake-up signals. Full performance is available to quickly react to action requests while the intermittent sleep phases greatly reduce the average system power consumption.

Note: When selecting the supply voltage and the clock source and generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states. Recommended sequences are provided which ensure the intended operation of power supply system and clock system. Please refer to the Programmer's Guide.

3.20 Instruction Set Summary

Table 11 lists the instructions of the XC226xN.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 11 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 20 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND[2]	t_{BWG} CC	–	–	50[3]		
Broken wire detection delay against VAREF[2]	t_{BWR} CC	–	–	50[4]		
Conversion time for 8-bit result[2]	t_{c8} CC	(11+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Conversion time for 10-bit result[2]	t_{c10} CC	(13+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Total Unadjusted Error	|TUE| CC	–	1	2	LSB	[5]
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	4	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	15	µs	
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	–	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	[6]
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used: $C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kOhm, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kOhm.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H)

4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 µs. This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H)

5) TUE is tested at V_{AREF} = V_{DDPA} = 5.0 V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

6) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

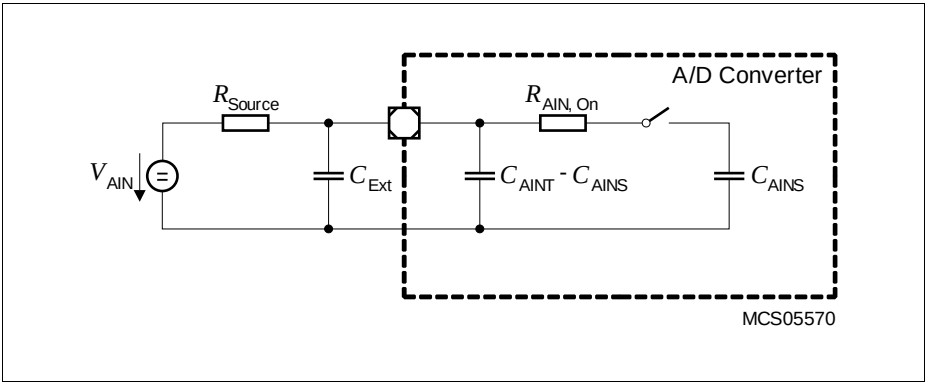

Figure 16 Equivalent Circuitry for Analog Inputs

2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.
3) Value of IMB_IMBCTRL.WSFLASH.
4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC226xN Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

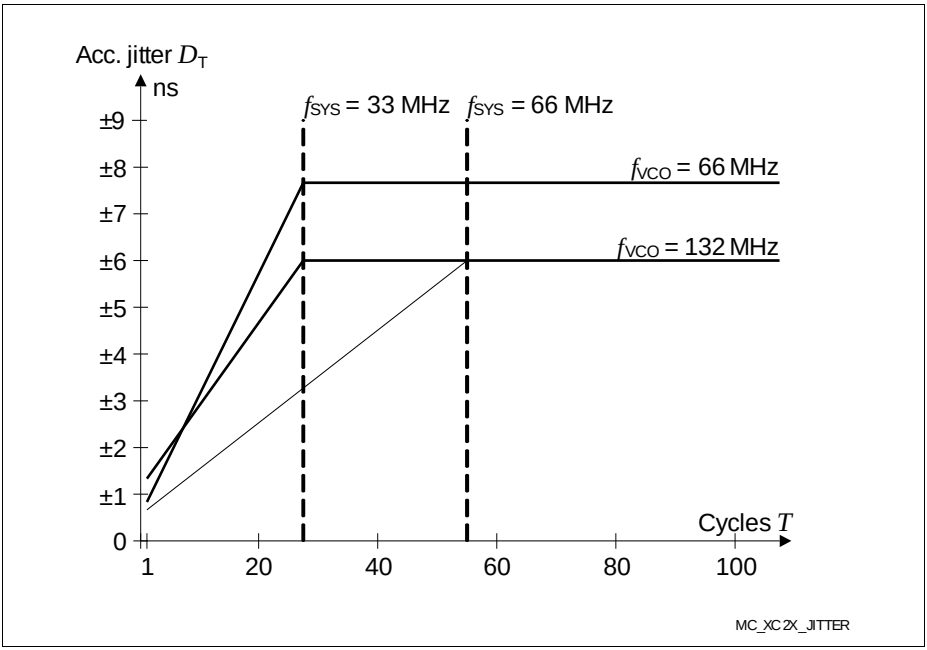

Figure 20 Approximated Accumulated PLL Jitter

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF.
The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

PLL frequency band selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 29 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	37 + 0.65 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	24 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	6.2 + 0.24 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	34 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	500 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

Table 32 External Bus Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	8	15	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	7	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	8	15	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	8	15	ns	
Output hold time for $\overline{RD}$, $\overline{WR}$($\overline{L}$/$\overline{H}$)	t_{20} CC	-2	6	8	ns	
Output hold time for $\overline{BHE}$, ALE	t_{21} CC	-2	6	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	6	8	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	6	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	6	8	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	25	15	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0[1)]	t_{31} SR	0	-7	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

Table 33 is valid under the following conditions: C_L= 20 pF; voltage_range= lower ; voltage_range= lower

4.7.7 Debug Interface Timing

The debugger can communicate with the XC226xN either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 38 is valid under the following conditions: C_L= 20 pF; voltage_range= upper

Table 38 DAP Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1)]	t_{11} SR	25	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time[1)]	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	17	20	–	ns	

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

Table 39 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

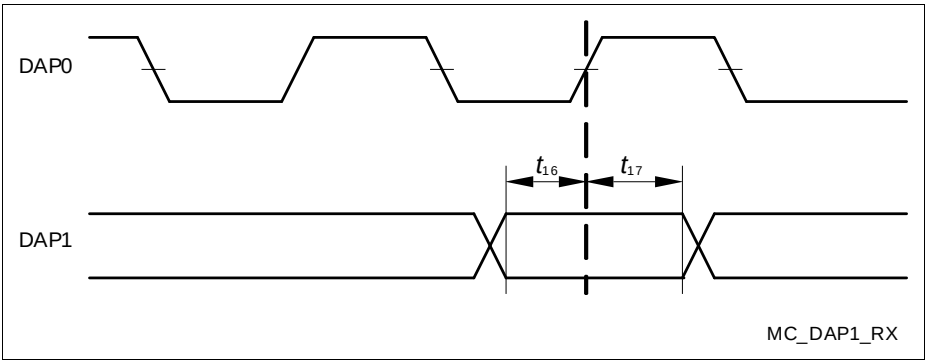

Figure 28 DAP Timing Host to Device

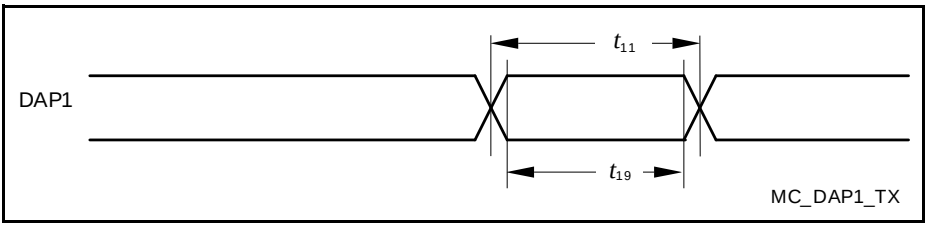

Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.

Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 40 is valid under the following conditions: C_L= 20 pF; voltage_range= upper

Table 40 JTAG Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	–	–	ns	[1]
TCK high time	t_2 SR	16	–	–	ns	