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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	120MHz
Connectivity	EBI/EMI, SCI, SPI, SSI
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	12KB (6K x 16)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.3V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LFBGA
Supplier Device Package	81-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56852vfe

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
E4	A0	Output(Z)	**Address Bus (A0–A16)—**These pins specify a word address for external program or data memory addresses.
F2	A1		
F3	A2		
F4	A3		
F1	A4		
G3	A5		
G2	A6		
J1	A7		
H2	A8		
H3	A9		
J2	A10		
H4	A11		
G4	A12		
J3	A13		
F5	A14		
H5	A15		
E5	A16		
F6	A17	**Output(Z)**	**Address Bus (A17)**
	TIO0	Input/Output	**Timer I/O (0)**—Can be programmed as either a timer input source or as a timer output flag.
G5	A18	**Output(Z)**	**Address Bus (A18)**
	TIO1	Input/Output	**Timer I/O (1)**—Can be programmed as either a timer input source or as a timer output flag.
H6	A19	**Output(Z)**	**Address Bus (A19)**
	$\overline{CS3}$	Output	**External Chip Select 3** —When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range.
J8	CLKO	**Output**	**Output clock (CLKO)**—User programmable clock out reference
	A20	Output	**Address Bus—A20**
D2	$\overline{CS0}$	**Output**	**Chip Select 0 ($\overline{CS0}$)** —When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range.
	GPIOA0	Input/Output	**Port A GPIO (0)** —A general purpose IO pin.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
D3	$\overline{CS1}$ GPIOA1	**Output** Input/Output	**Chip Select 1 ($\overline{CS1}$)** —When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range. **Port A GPIO (1)** —A general purpose IO pin.
C3	$\overline{CS2}$ GPIOA2	**Output** Input/Output	**Chip Select 2 ($\overline{CS2}$)**—When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range. **Port A GPIO (2)** —A general purpose IO pin.
G7	D0	**Input**/Output	**Data Bus (D0–D12)** —specify the data for external program or data memory accesses. D0–D15 are tri-stated when the external bus is inactive.
H7	D1		
H8	D2		
G8	D3		
H9	D4		
F8	D5		
F7	D6		
G6	D7		
E8	D8		
E7	D9		
E6	D10		
D8	D11		
D7	D12		
D9	D13 MODE A	**Input**/Output	**Data Bus (D13–D15)** — specify the data for external program or data memory accesses. D0–D15 are tri-stated when the external bus is inactive. **Mode Select**—During the bootstrap process the MODE A, MODE B, and MODE C pins select one of the eight bootstrap modes. These pins are sampled at the end of reset. **Note:** Any time POR and EXTERNAL resets are active, the state of MODE A, B and C pins get asynchronously transferred to the SIM Control Register [14:12] ($1FFF08) respectively. These bits determine the mode in which the part will boot up. **Note:** Software and COP resets do not update the SIM Control Register.
C8	D14 MODE B		
A9	D15 MODE C		
E2	$\overline{RD}$	Output	**Bus Control– Read Enable ($\overline{RD}$)**—is asserted during external memory read cycles. When $\overline{RD}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the data bus. When $\overline{RD}$ is deasserted high, the external data is latched inside the controller. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a Static RAM or ROM.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
E3	$\overline{WR}$	Output	**Bus Control–Write Enable ($\overline{WR}$)**— is asserted during external memory write cycles. When $\overline{WR}$ is asserted low, pins D0–D15 become outputs and the controller puts data on the bus. When $\overline{WR}$ is deasserted high, the external data is latched inside the external device. When $\overline{WR}$ is asserted, it qualifies the A0–A15 pins. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a Static RAM.
B4	RXD	**Input**	**SCI Receive Data (RXD)—**This input receives byte-oriented serial data and transfers it to the SCI receive shift register.
	GPIOE0	Input/Output	**Port E GPIO (0)**—A general purpose I/O pin.
D4	TXD	**Output(Z)**	**SCI Transmit Data (TXD)—**This signal transmits data from the SCI transmit data register.
	GPIOE1	Input/Output	**Port E GPIO (1)**—A general purpose I/O pin.
B2	GPIOC0	**Input**/Output	**Port C GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when the SSI is not in use.
	STXD	**Output**	**SSI Transmit Data (STXD)—**This output pin transmits serial data from the SSI Transmitter Shift Register.
A2	GPIOC1	**Input**/Output	**Port C GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the SSI is not in use.
	SRXD	**Input**	**SSI Receive Data (SRXD)—**This input pin receives serial data and transfers the data to the SSI Receive Shift Register.
A3	SCLK	**Input**/Output	**SPI Serial Clock (SCLK)**—In Master mode, this pin serves as an output, clocking slaved listeners. In Slave mode, this pin serves as the data clock input.
	GPIOC2	Input/Output	**Port C GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
	STCK	Input/Output	**SSI Serial Transfer Clock (STCK)—**This bidirectional pin provides the serial bit rate clock for the transmit section of the SSI. The clock signal can be continuous or gated.
B3	$\overline{SS}$	**Input**	**SPI Slave Select ($\overline{SS}$)**—In Master mode, this pin is used to arbitrate multiple masters. In Slave mode, this pin is used to select the slave.
	GPIOC3	Input/Output	**Port C GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
	STFS	Input/Output	**SSI Serial Transfer Frame Sync (STFS) —**This bidirectional pin is used to count the number of words in a frame while transmitting. A programmable frame rate divider and a word length divider are used for frame rate sync signal generation.

Part 4 Specifications

4.1 General Characteristics

The 56852 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term “5-volt tolerant” refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V- compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ±10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 4-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56852 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 4-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
V_{DD} supply current (Core logic, memories, peripherals)	I_{DD}[4]				
Run [1]		—	55	70	mA
Deep Stop[2]		—	0.02	2.5	mA
Light Stop[3]		—	3.4	8	mA
V_{DDIO} supply current (I/O circuity)	I_{DDIO}				
Run[5]		—	40	50	mA
Deep Stop[2]		—	0	300	μA
V_{DDA} supply current (analog circuity)	I_{DDA}				
Deep Stop[2]		—	60	120	μA
Low Voltage Interrupt[6]	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[7]	POR	—	1.5	2.0	V

Note: Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out.

1. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active as long as the internal 2.5V is below 1.8V, no matter how long the ramp up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.

Table 4-7 External Memory Interface Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$ V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, P = 8.333ns

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	WWS=0	-0.75	0.50	WWSS	ns
		WWS>0	-1.50	0.69		
$\overline{WR}$ Width Asserted to $\overline{WR}$ Deasserted	t_{WR}	WWS=0	-0.52	0.19	WWS	ns
		WWS>0	-0.13	0.00		
Data Out Valid to $\overline{WR}$ Asserted	t_{DWR}	WWS=0	-1.86	0.00	WWSS	ns
		WWS=0	- 6.03	0.25		
		WWS>0	-1.73	0.19		
		WWS>0	-4.29	0.50		
Valid Data Out Hold Time after $\overline{WR}$ Deasserted	t_{DOH}		-1.71	0.25	WWSH	ns
Valid Data Out Set Up Time to $\overline{WR}$ Deasserted	t_{DOS}		-2.38	0.19	WWS,WWSS	ns
			-4.42	0.50		
Valid Address after $\overline{WR}$ Deasserted	t_{WAC}		-1.44	0.25	WWSH	
$\overline{RD}$ Deasserted to Address Invalid	t_{RDA}		- 0.51	0.00	RWSH	ns
Address Valid to $\overline{RD}$ Deasserted	t_{ARDD}		-2.03	1.00	RWSS,RWS	ns
Valid Input Data Hold after $\overline{RD}$ Deasserted	t_{DRD}		0.00	N/A[1]	—	ns
$\overline{RD}$ Assertion Width	t_{RD}		-0.97	1.00	RWS	ns
Address Valid to Input Data Valid	t_{AD}		-10.13	1.00	RWSS,RWS	ns
			-13.22	1.19		
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}		- 1.06	0.00	RWSS	ns
$\overline{RD}$ Asserted to Input Data Valid	t_{RDD}		-9.06	1.00	RWSS,RWS	ns
			-12.65	1.19		
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}		-0.70	0.25	WWSH,RWSS	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}		-0.17[2]	0.00	RWSS,RWSH	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	WWS=0	-0.47	0.75	WWSS, WWSH	ns
		WWS>0	-0.07	1.00		
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}		0.10	0.50	MDAR, BMDAR, RWSH, WWSS	ns
			-0.31	0.69		

1. N/A since device captures data before it deasserts $\overline{RD}$
2. If RWSS = RWSH = 0, RD does not deassert during back-to-back reads and D = 0.00 should be used.

4.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 4-8 Reset, Stop, Wait, Mode Select, and Interrupt Timing [1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	11	ns	4-11
Minimum $\overline{\text{RESET}}$ Assertion Duration[3]	t_{RA}	30	—	ns	4-11
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	—	120T	ns	4-11
Edge-sensitive Interrupt Request Width	t_{IRW}	1T + 3	—	ns	4-12
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	18T	—	ns	4-13
	$t_{IDM\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	4-13
	$t_{IG\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[4]	t_{IRI}	22T	—	ns	4-14
	$t_{IRI\ -FAST}$	18T	—		
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Stop) to External Data Memory[5]	t_{IW}	1.5T	—	ns	4-15
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Wait) to External Data Memory	t_{IF}				4-15
Fast[6]		18T	—	ns	
Normal[7]		22ET	—	ns	
RSTO pulse width[8]	t_{RSTO}				4-16
normal operation		128ET	—	—	
internal reset mode		8ET	—	—	

1. In the formulas, T = clock cycle. For $f_{op} = 120MHz$ operation and $f_{ipb} = 60MHz$, T = 8.33ns.
2. Parameters listed are guaranteed by design.
3. At reset, the PLL is disabled and bypassed. The part is then put into run mode and t_{clk} assumes the period of the source clock, t_{xtal}, t_{extal} or t_{osc}.
4. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
5. The interrupt instruction fetch is visible on the pins only in Mode 3.
6. Fast stop mode:

   Fast stop recovery applies when external clocking is in use (direct clocking to XTAL) or when fast stop mode recovery is requested (OMR bit 6 is set to 1). In both cases the PLL and the master clock are unaffected by stop mode entry. Recovery takes one less cycle and t_{clk} will continue same value it had before stop mode was entered.
7. Normal stop mode:

   As a power saving feature, normal stop mode disables and bypasses the PLL. Stop mode will then shut down the master clock, recovery will take an extra cycle (to restart the clock), and t_{clk} will resume at the input clock source rate.
8. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125 ns.

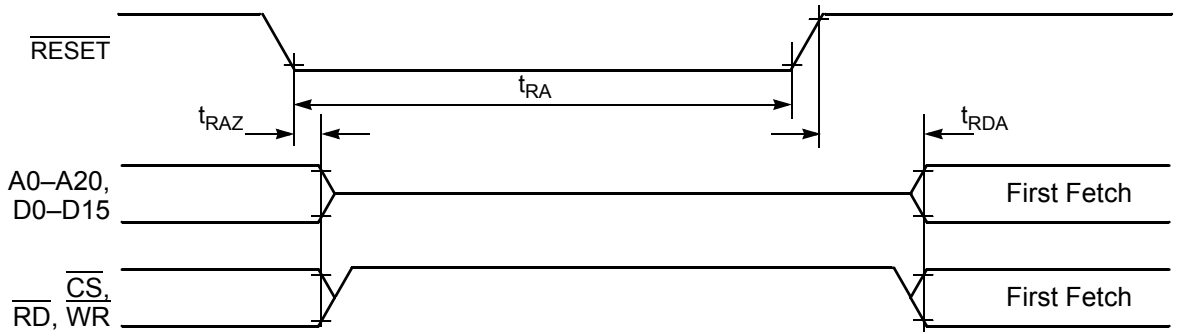


Figure 4-11 Asynchronous Reset Timing

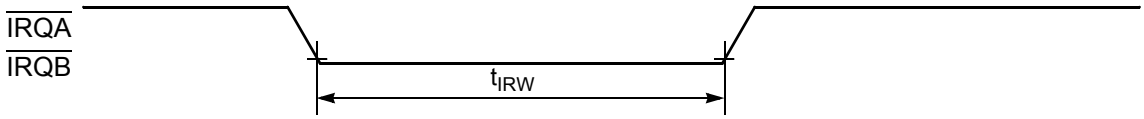
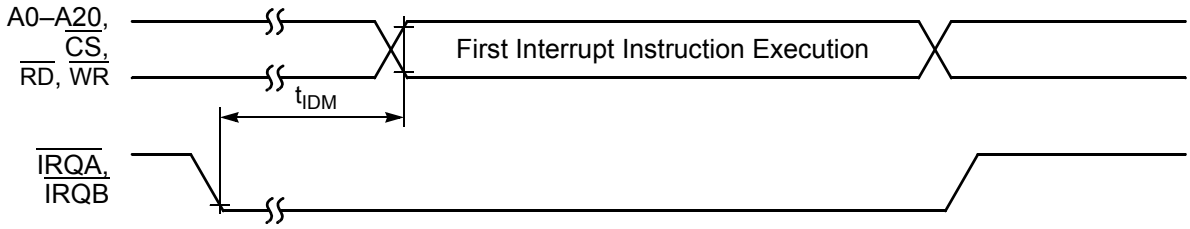
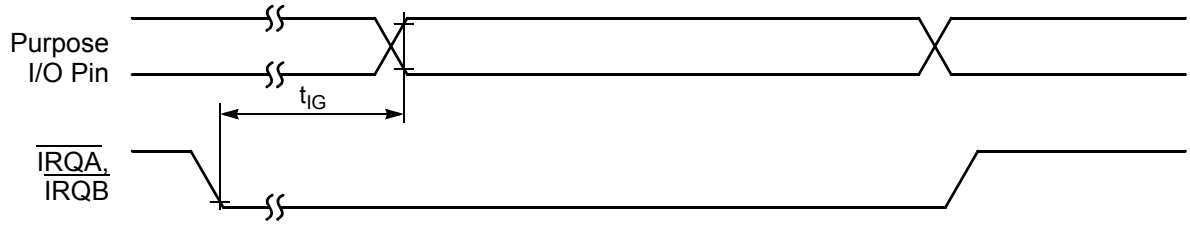


Figure 4-12 External Interrupt Timing (Negative-Edge-Sensitive)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 4-13 External Level-Sensitive Interrupt Timing

Figure 4-14 Interrupt from Wait State Timing

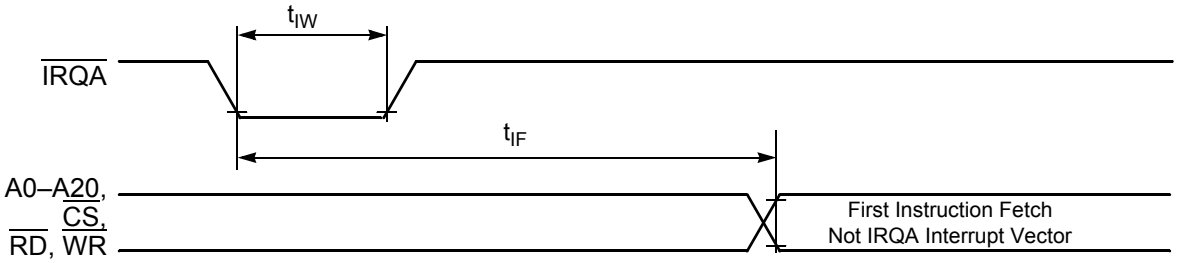


Figure 4-15 Recovery from Stop State Using Asynchronous Interrupt Timing

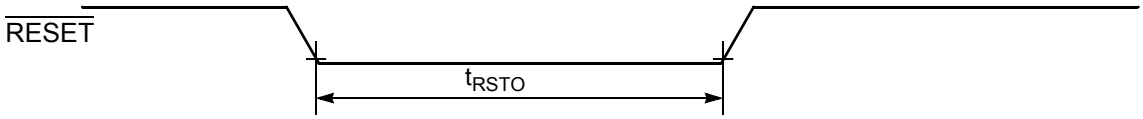


Figure 4-16 Reset Output Timing

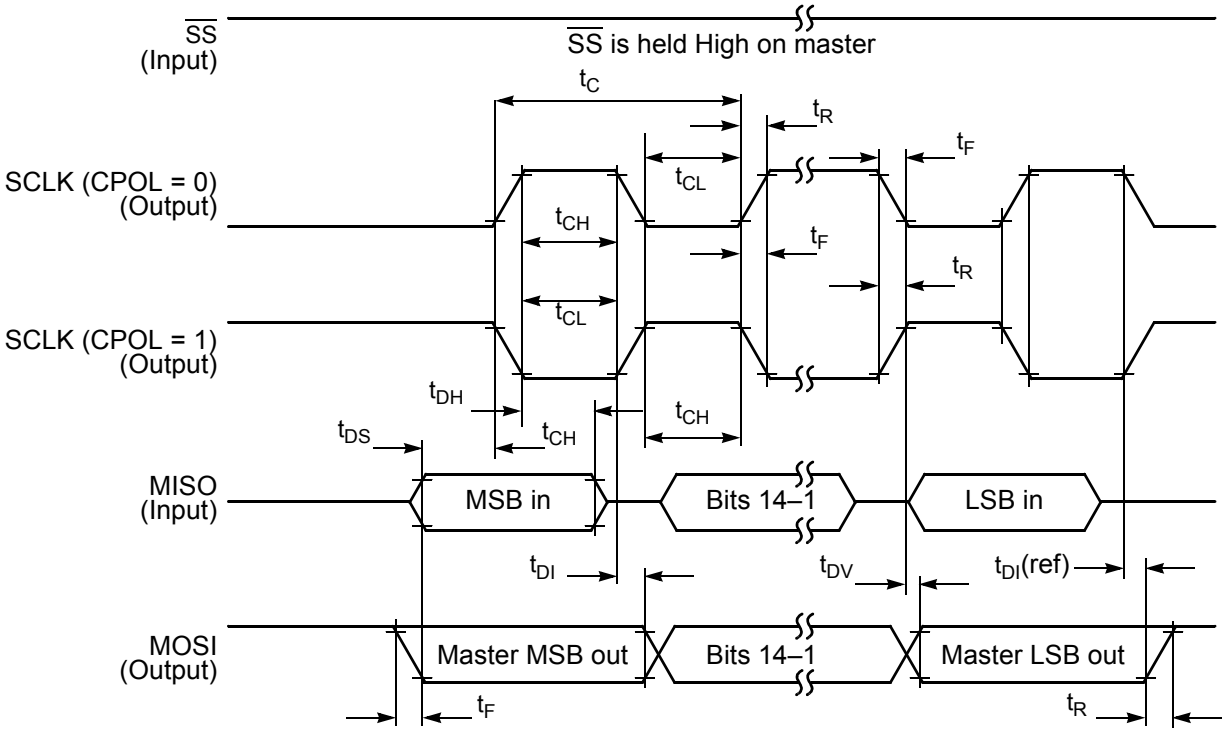


Figure 4-17 SPI Master Timing (CPHA = 0)

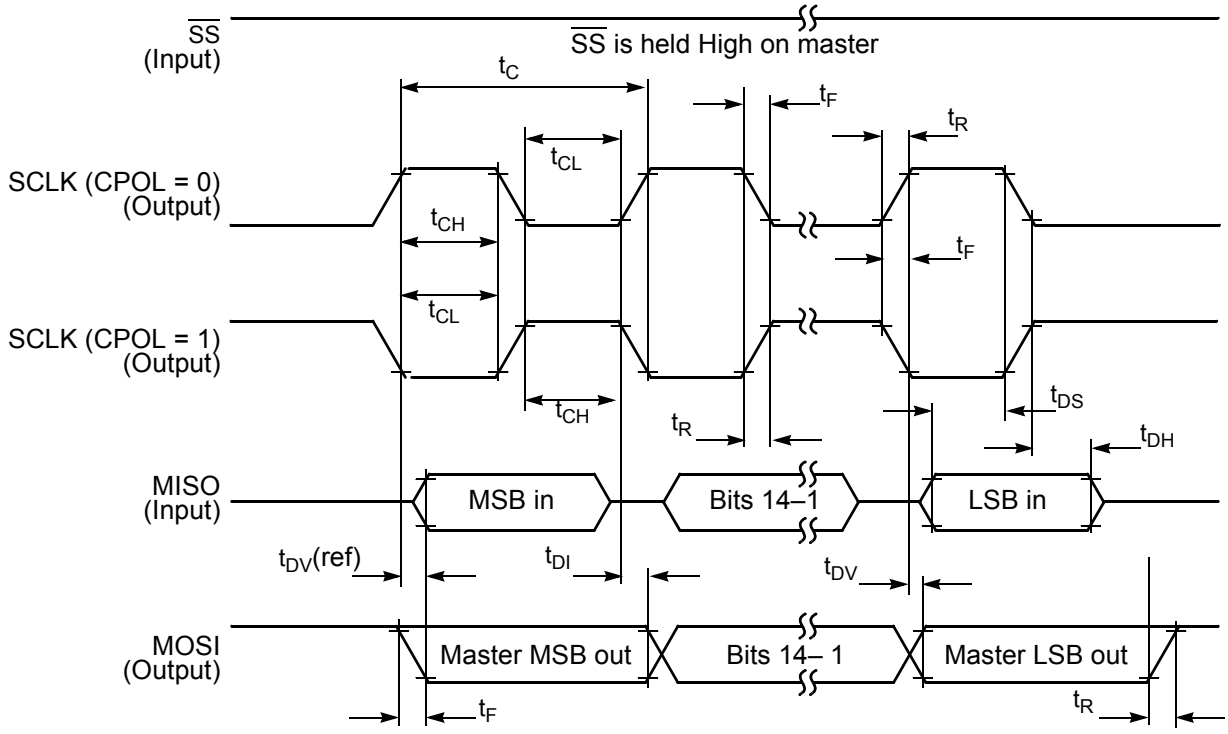


Figure 4-18 SPI Master Timing (CPHA = 1)

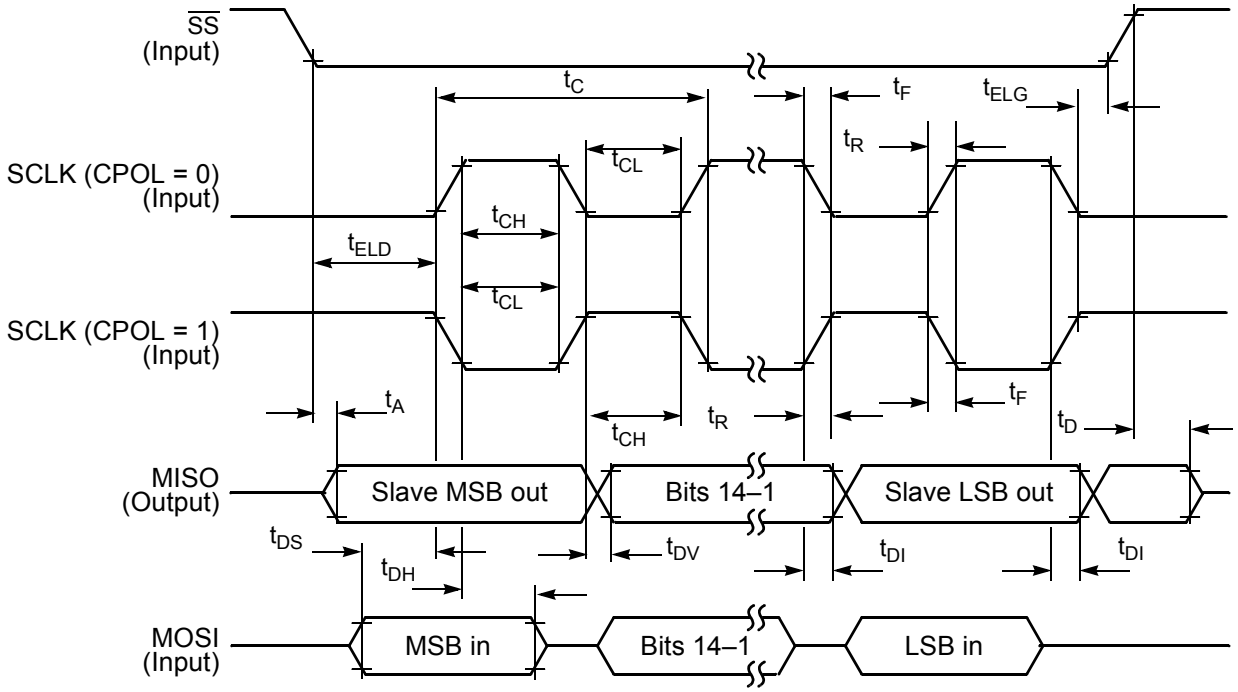


Figure 4-19 SPI Slave Timing (CPHA = 0)

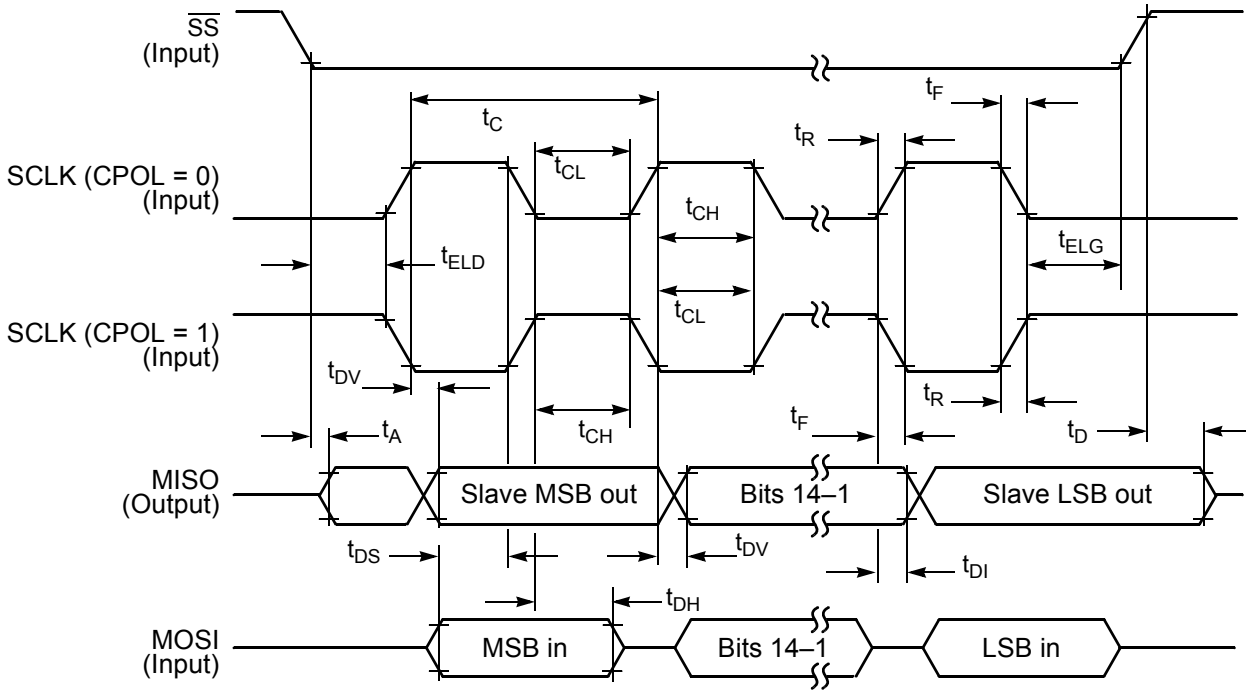


Figure 4-20 SPI Slave Timing (CPHA = 1)

4.9 Quad Timer Timing

Table 4-10 Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0–3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	2T + 3	—	ns
Timer input high/low period	P_{INHL}	1T + 3	—	ns
Timer output period	P_{OUT}	2T - 3	—	ns
Timer output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For f_{op} = 120MHz operation and fipb = 60MHz, T = 8.33ns
2. Parameters listed are guaranteed by design.

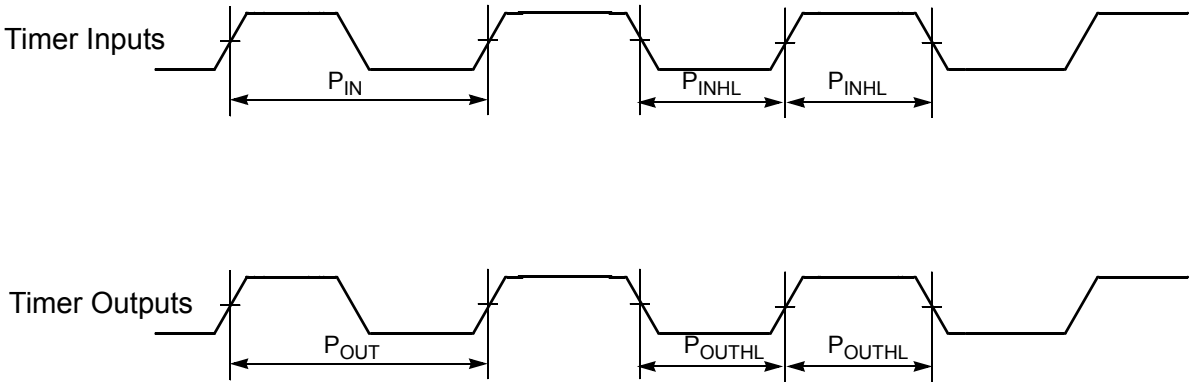


Figure 4-21 Timer Timing

2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for a 120MHz part.

3. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync has been inverted, all the timings remain valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS in the tables and in the figures.

4. bl = bit length; wl = word length

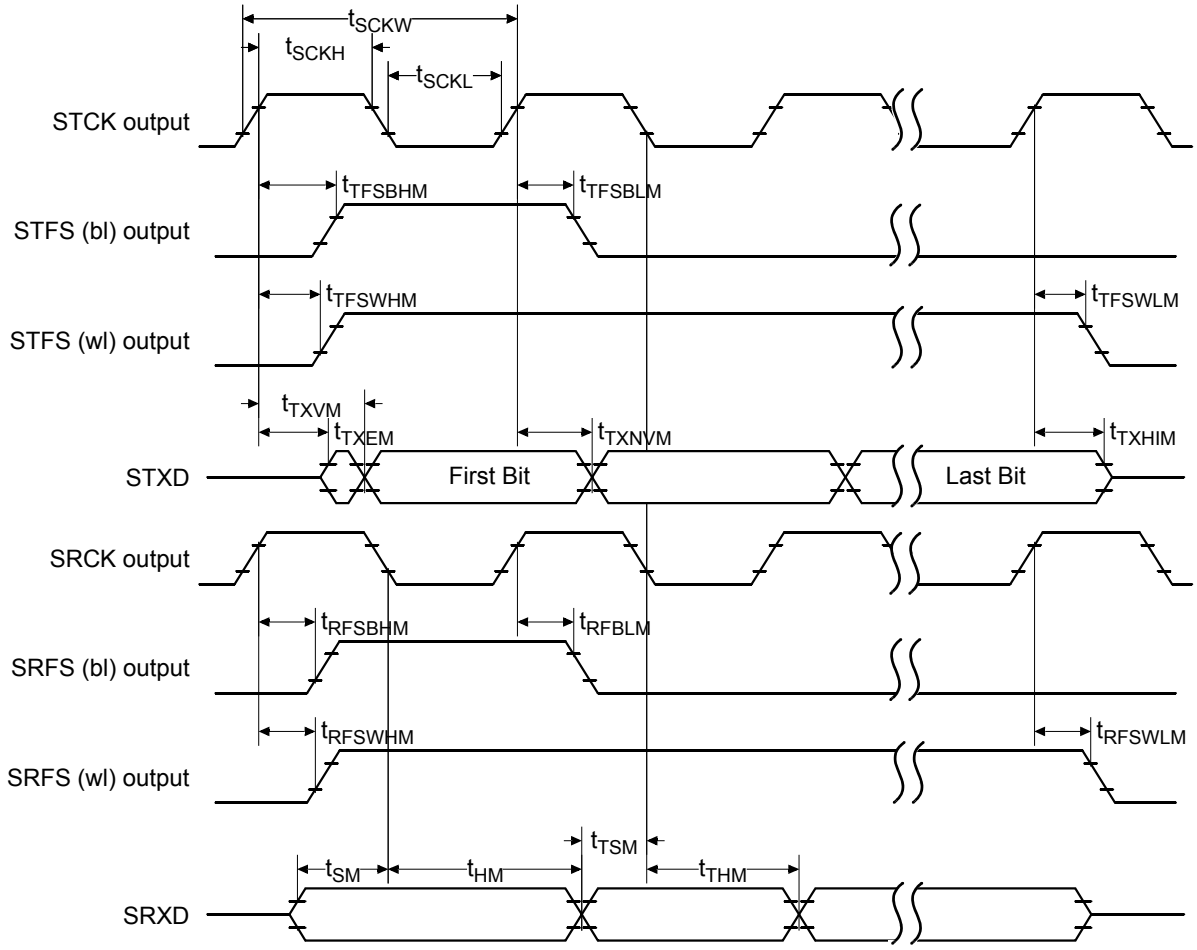


Figure 4-22 Master Mode Timing Diagram

4.13 GPIO Timing

Table 4-15 GPIO Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.7\text{-}1.9V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit
GPIO input period	P_{IN}	2T + 3	—	ns
GPIO input high/low period	P_{INHL}	1T + 3	—	ns
GPIO output period	P_{OUT}	2T - 3	—	ns
GPIO output high/low period	P_{OUTHL}	1T - 3	—	ns

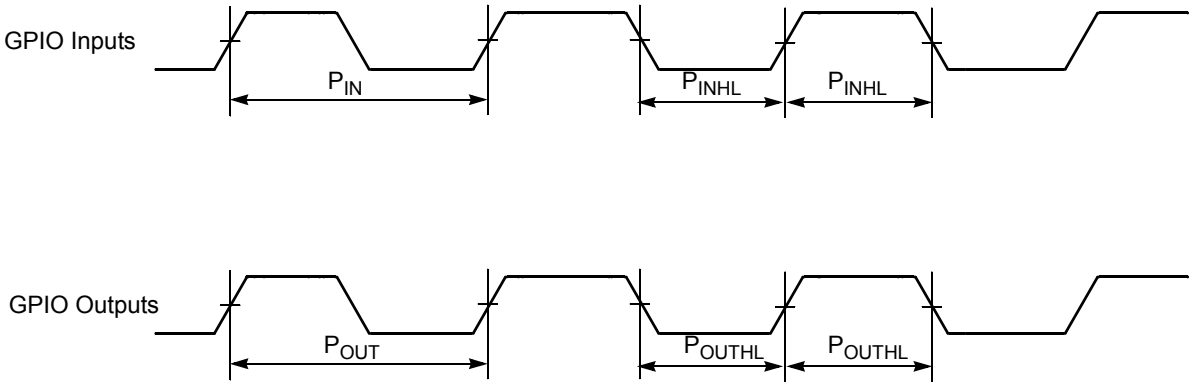


Figure 4-31 GPIO Timing

Part 5 56852 Packaging & Pinout Information

This section contains package and pin-out information for the 81-pin MAPBGA configuration of the 56852.

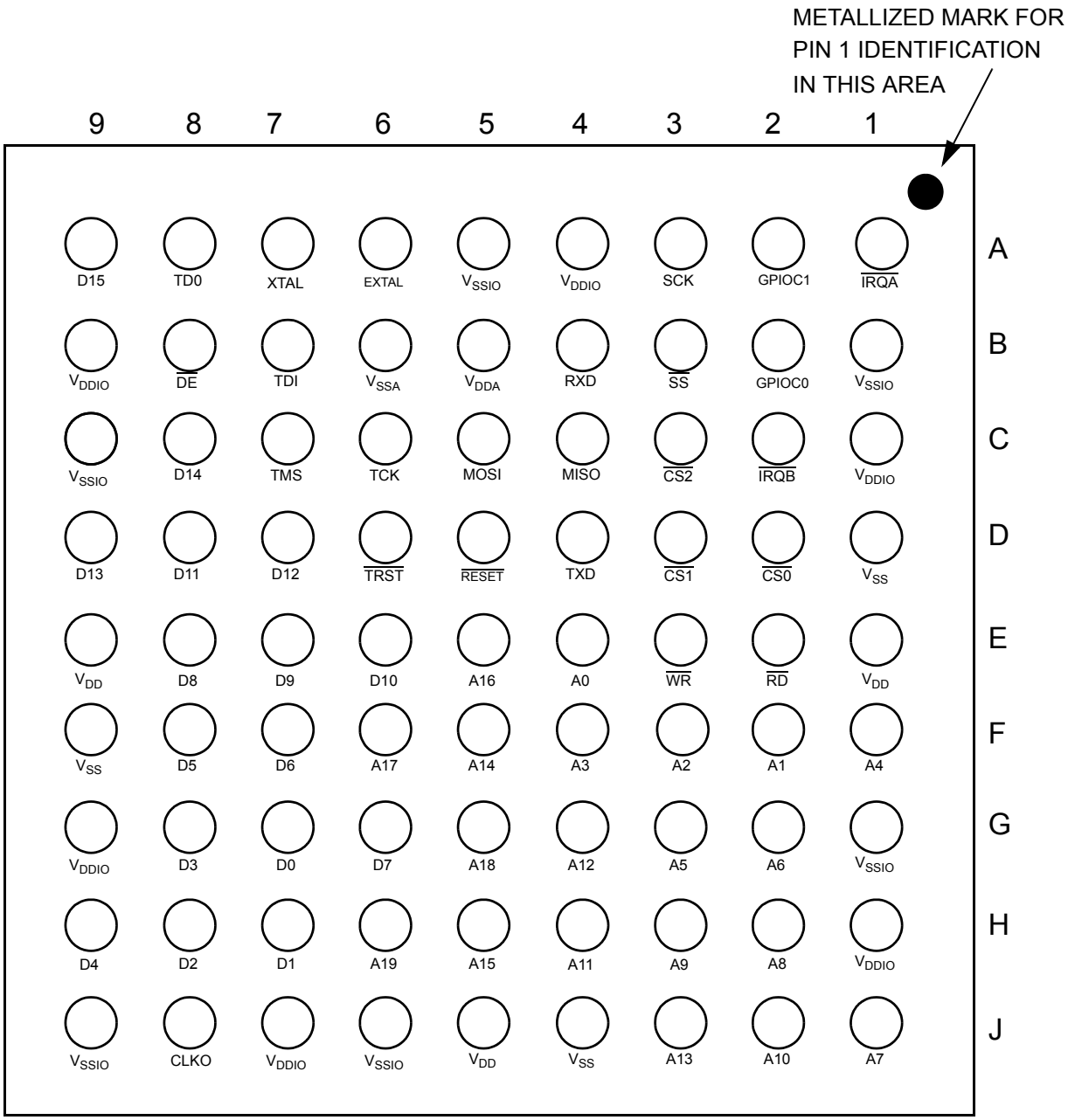


Figure 5-1 Bottom-View, 56852 81-pin MAPBGA Package

Part 6 Design Considerations

6.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

6.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and GND.
- Bypass the V_{DD} and GND layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the device's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.

Part 7 Ordering Information

Table 7-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 7-1 56852 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56852	1.8–3.3 V	Mold Array Process Ball Grid Array (MAPBGA)	81	120	DSP56852VF120
DSP56852	1.8–3.3 V	Mold Array Process Ball Grid Array (MAPBGA)	81	120	DSP56852VFE *

*This package is RoHS compliant.

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