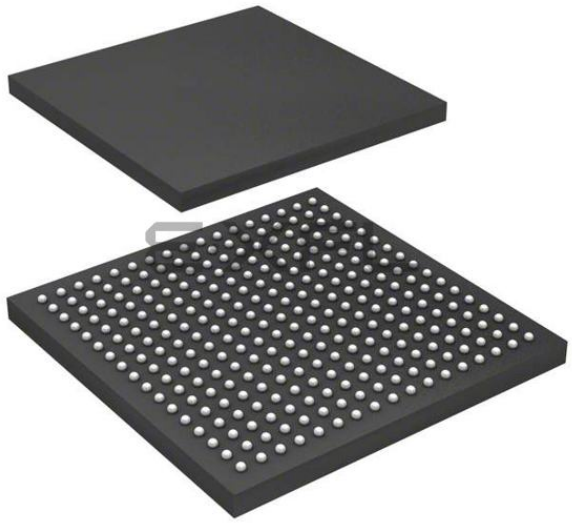

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y2cvm05aa

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y2CVM08AA MCIMX6Y2CVM08AB	Features supports: • 792 MHz, industrial grade for general purpose • Basic security • With LCD/CSI • CAN x2 • Ethernet x2 • USB OTG x2 • ADC x2 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14 mm, 0.8 pitch MAPBGA	-40 to +105
MCIMX6Y2CVK08AB	Features supports: • 792 MHz, industrial grade for general purpose • Basic security • With LCD/CSI • CAN x2 • Ethernet x2 • USB OTG x2 • ADC x2 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	9 x 9 mm, 0.5 pitch MAPBGA	-40 to +105

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number they have (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 6ULL Applications Processors for Industrial Products Data Sheet (IMX6ULLIEC) covers parts listed with a “C (Industrial temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there will be any questions, visit the web page NXP.com/imx6series or contact a NXP representative for details.

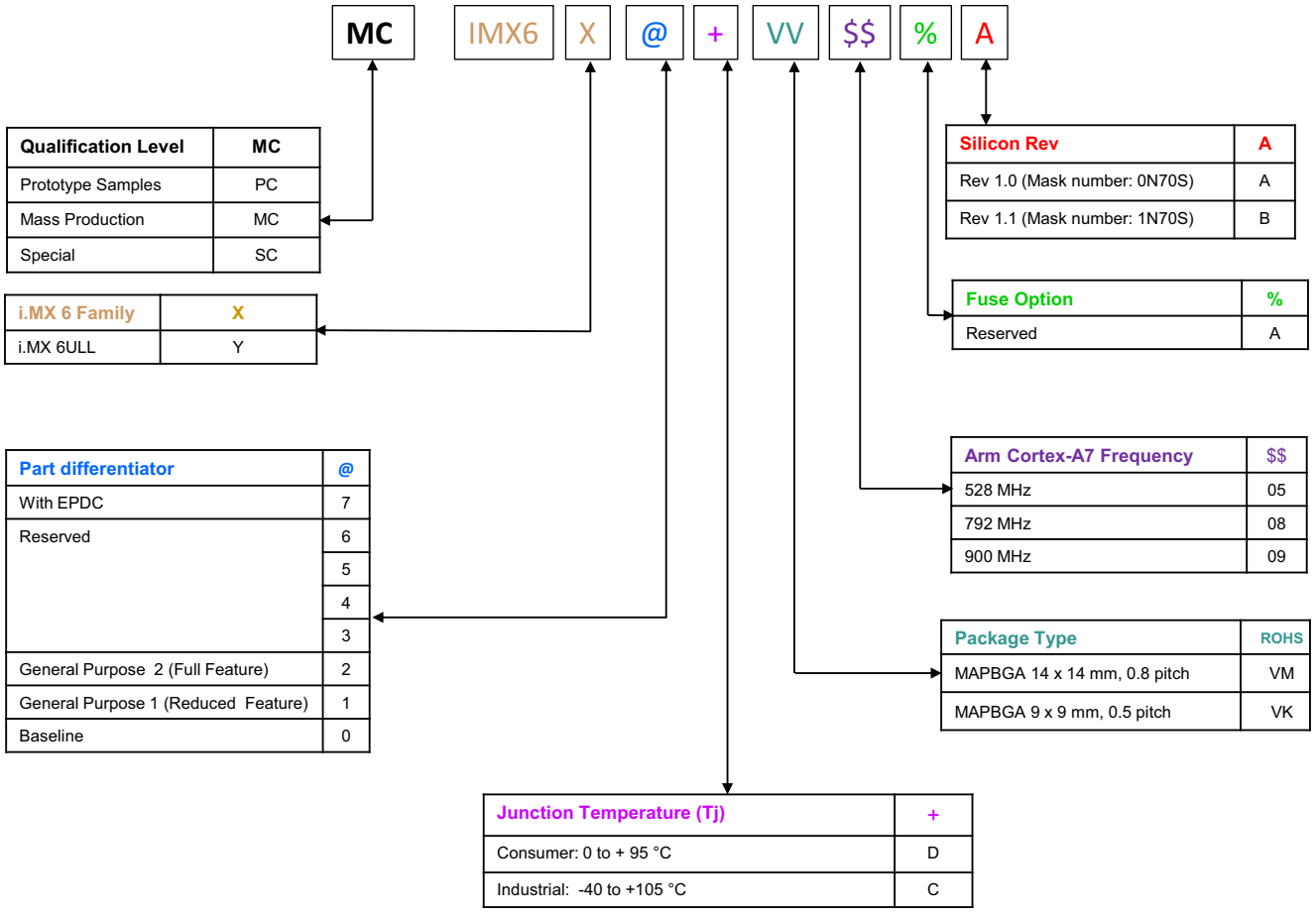

Figure 1. Part Number Nomenclature—i.MX 6ULL

1.2 Features

The i.MX 6ULL processors are based on Arm Cortex-A7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-A7 MPCore (with TrustZone) with:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A7 NEON Media Processing Engine (MPE) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache
- Single Master AXI bus interface output of L2 cache

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6ULL processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6ULL processor system.

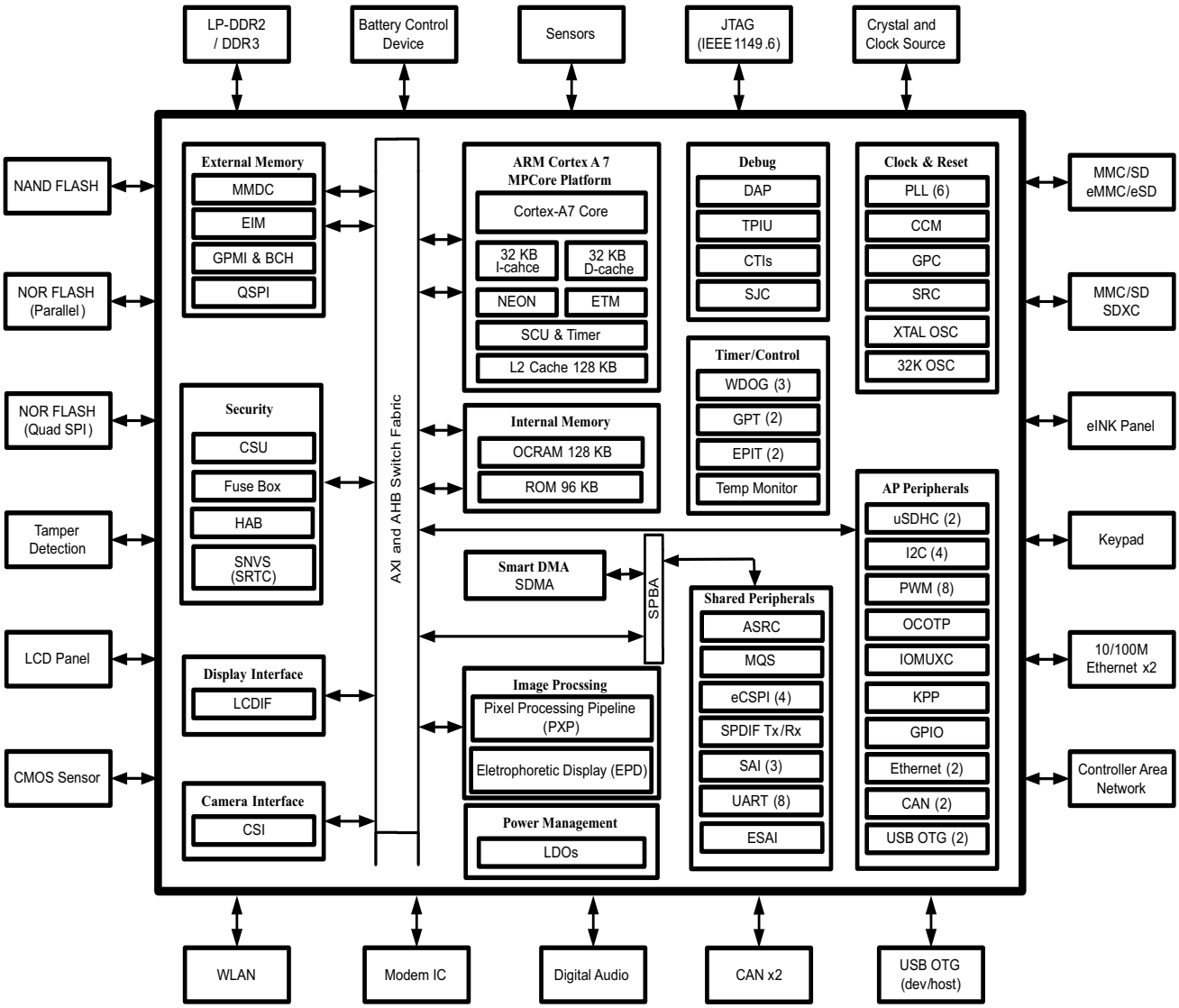

Figure 2. i.MX 6ULL System Block Diagram

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.
RNGB	Random Number Generator	Security	Random number generating module.
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6ULL reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be disconnected by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for NXP factory use. The user must tie this pin directly to GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6ULL processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6ULL Chip-Level Conditions

For these characteristics	Topic appears
Absolute Maximum Ratings	on page 22
Thermal Resistance	on page 22
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximum Supply Currents	on page 27
Power Modes	on page 28
USB PHY Current Consumption	on page 31

Table 22. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

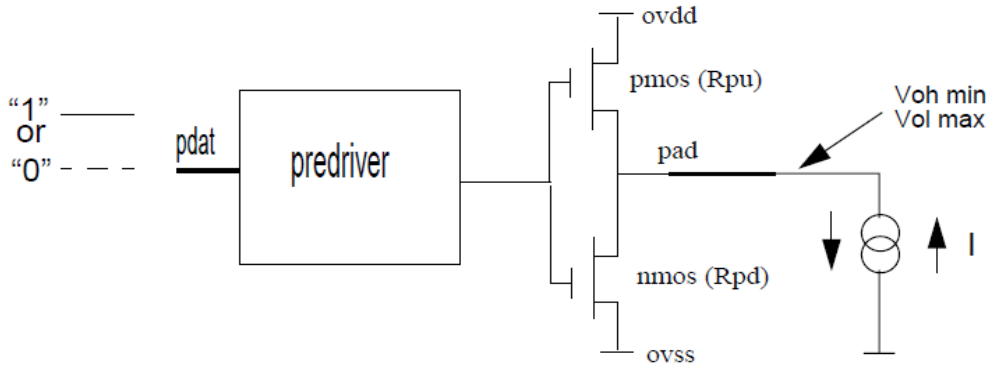

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 23 shows the DC parameters for the clock inputs.

Table 23. XTALI and RTC_XTALI DC Parameters [1]

Parameter	Symbol	Test Conditions	Min	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL	NVCC_PLL	V
XTALI low-level DC input voltage	Vil	—	0	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	1.1	V
RTC_XTALI low-level DC input voltage	Vil	—	0	0.2	V

- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

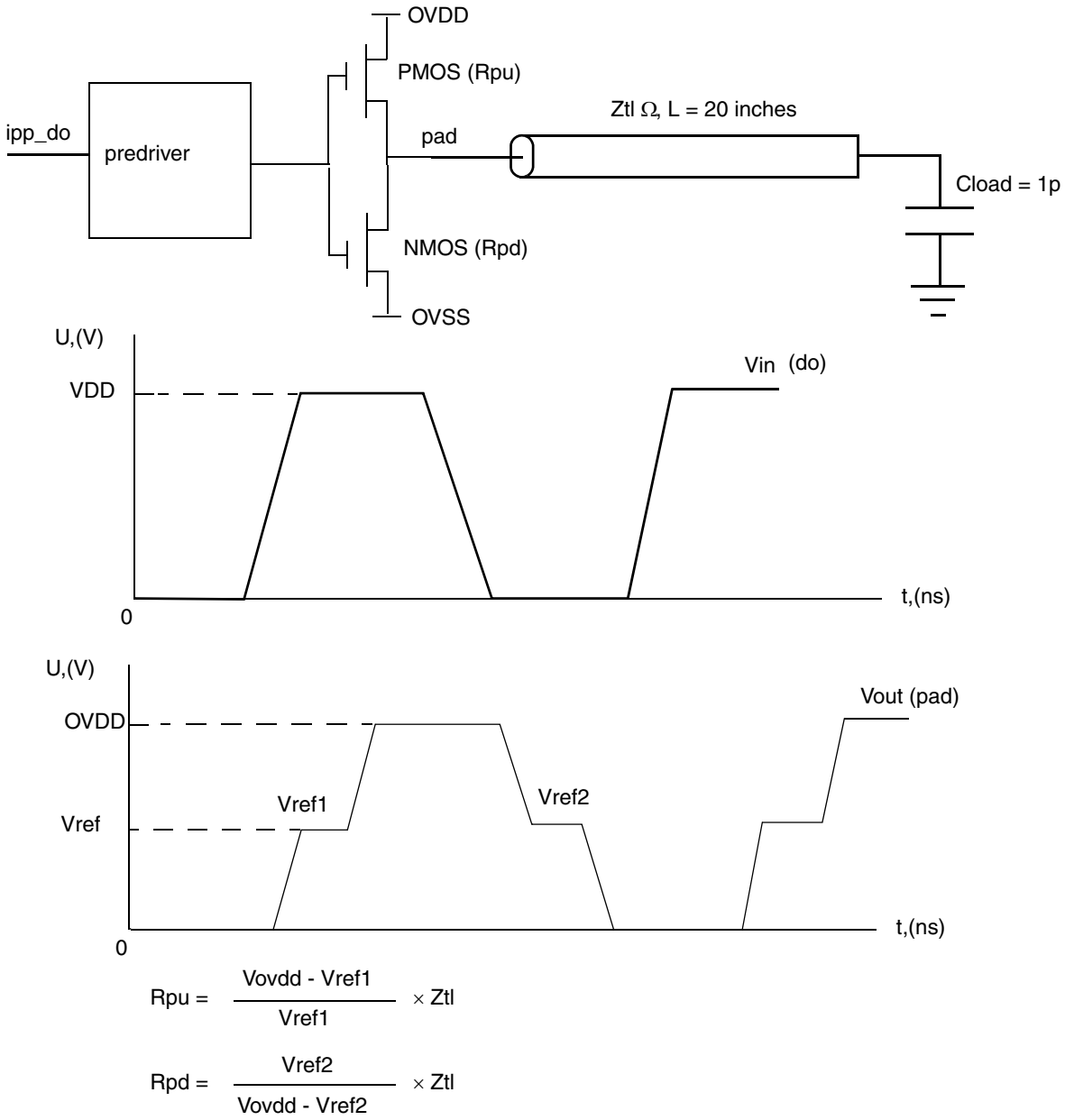

Figure 6. Impedance Matching Load for Measurement

Table 42. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see 2]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see 2]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see 2]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see 2]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see 2]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see 3,2]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see 2]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see 2]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see 2]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see 5,6]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see 5,6]	—	ns

1 GPMI's Async Mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 24), NF16/NF17 is different from the definition in non-EDO mode (Figure 23). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 6ULL Reference Manual*). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 26 to Figure 28 show the write and read timing of Source Synchronous Mode.

clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.3 Samsung Toggle Mode AC Timing

4.11.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.11.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

4.11.3.2 Read and Write Timing

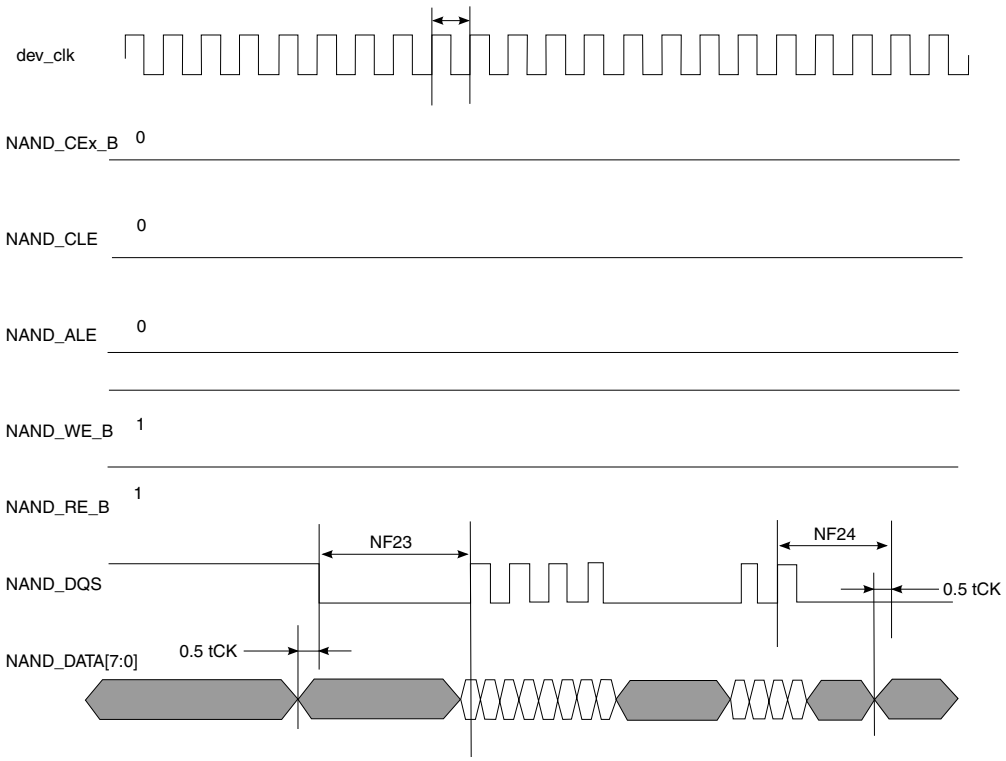

Figure 30. Samsung Toggle Mode Data Write Timing

4.12.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.12.2.1 ECSPI Master Mode Timing

Figure 35 depicts the timing of ECSPI in master mode. Table 47 lists the ECSPI master mode timing characteristics.

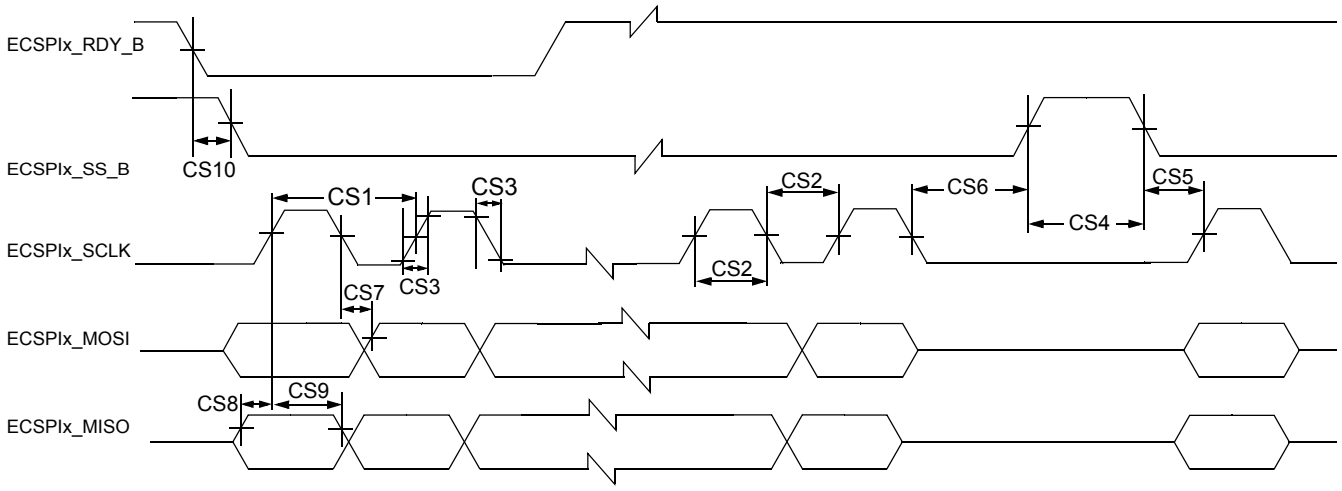

Figure 35. ECSPI Master Mode Timing Diagram

Table 47. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	14	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.7, “I/O AC Parameters”.”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.4.4 HS200 Mode Timing

Figure 43 depicts the timing of HS200 mode, and Table 53 lists the HS200 timing characteristics.

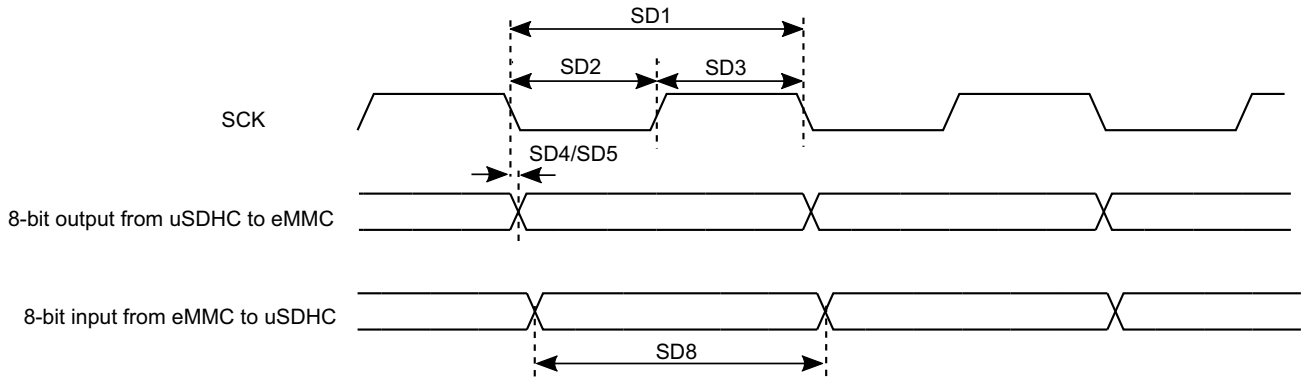

Figure 43. HS200 Mode Timing

Table 53. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.12.4.5 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1 supply are identical to those shown in Table 24, "Single Voltage GPIO DC Parameters," on page 38.

4.12.5 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.12.10 QUAD SPI (QSPI) Timing Parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.12.10.1 SDR Mode

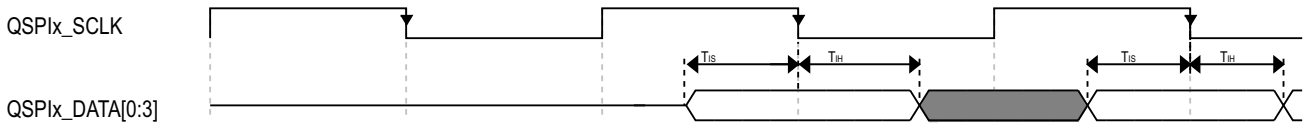

Figure 51. QuadSPI Input/Read Timing (SDR mode with internal sampling)

Table 62. QuadSPI Input Timing (SDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

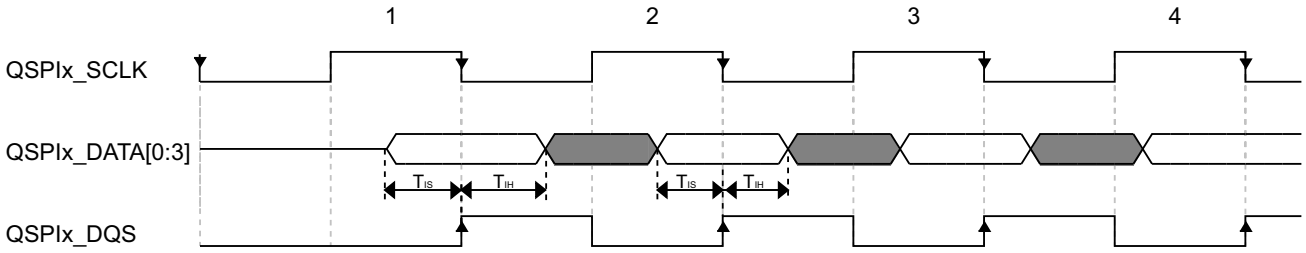

Figure 52. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Table 63. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

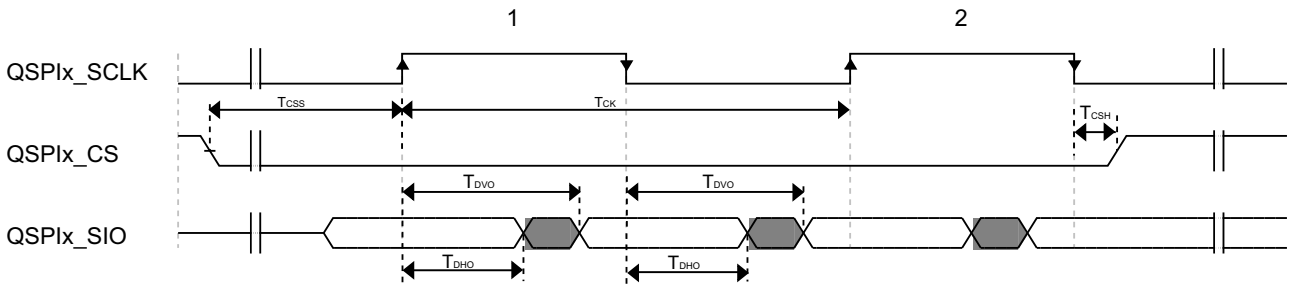

Figure 56. QuadSPI Output/Write Timing (DDR mode)

Table 67. QuadSPI Output/Write Timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	(0.25 x T_{SCLK}) + 2	ns
T_{DHO}	Output data hold time	(0.25 x T_{SCLK}) - 0.5	—	ns
T_{CK}	SCK clock period	20	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6ULL Reference Manual (IMX6ULLRM)* for more details.

4.12.11 SAI/I2S Switching Specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 68. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	2 x t_{sys}	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	4 x t_{sys}	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 68 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 75 lists the receive timing characteristics.

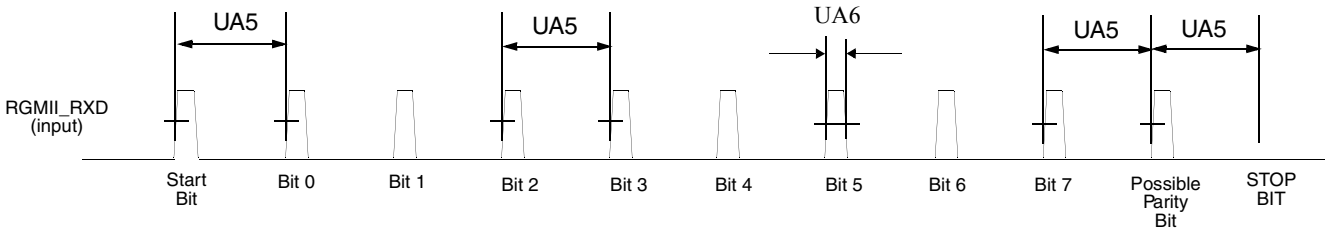

Figure 68. UART IrDA Mode Receive Timing Diagram

Table 75. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.
2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.15 USB PHY Parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

Table 76. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

1 Typical values assume VDDAD = 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential differences

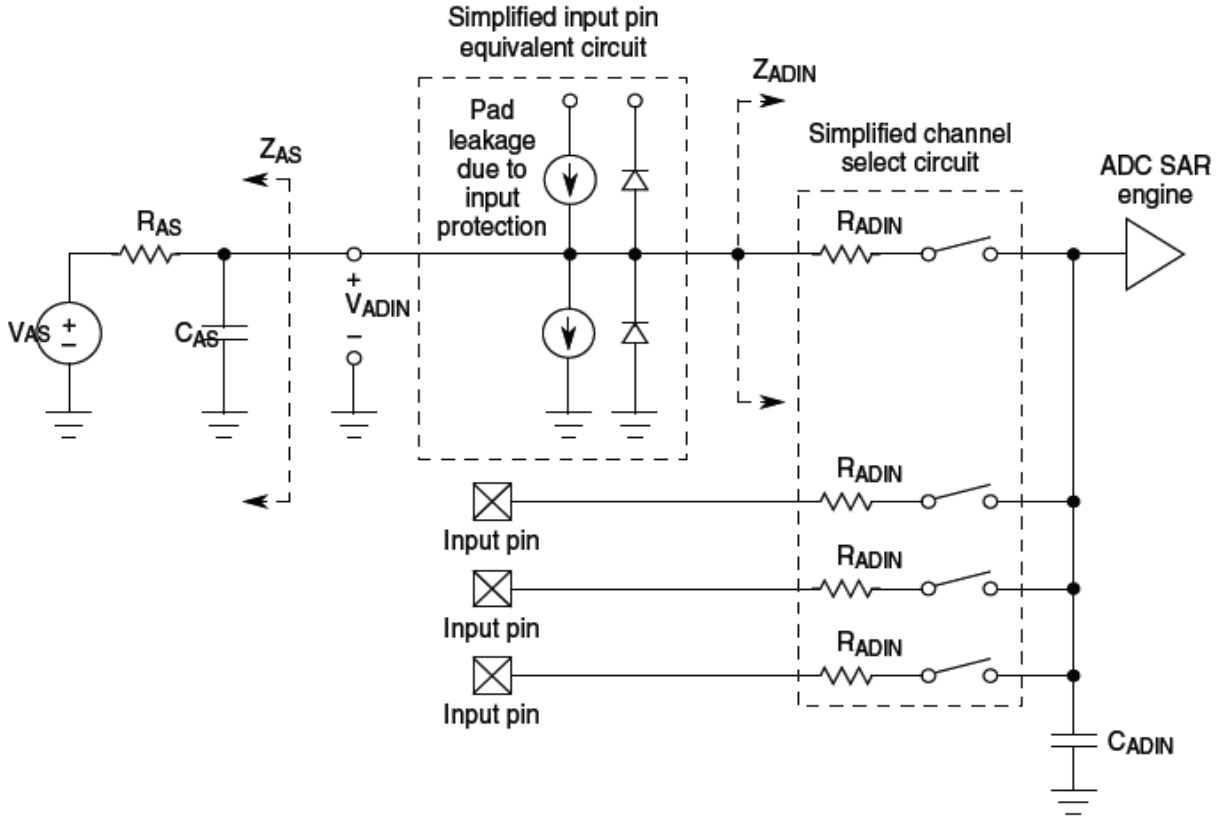

Figure 69. 12-bit ADC Input Impedance Equivalency Diagram

Table 78. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	Details
LCD_DATA00	Input with 100 K pull-down	BT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DATA01	Input with 100 K pull-down	BT_CFG1[1]	
LCD_DATA02	Input with 100 K pull-down	BT_CFG1[2]	
LCD_DATA03	Input with 100 K pull-down	BT_CFG1[3]	
LCD_DATA04	Input with 100 K pull-down	BT_CFG1[4]	
LCD_DATA05	Input with 100 K pull-down	BT_CFG1[5]	
LCD_DATA06	Input with 100 K pull-down	BT_CFG1[6]	
LCD_DATA07	Input with 100 K pull-down	BT_CFG1[7]	
LCD_DATA08	Input with 100 K pull-down	BT_CFG2[0]	
LCD_DATA09	Input with 100 K pull-down	BT_CFG2[1]	
LCD_DATA10	Input with 100 K pull-down	BT_CFG2[2]	
LCD_DATA11	Input with 100 K pull-down	BT_CFG2[3]	
LCD_DATA12	Input with 100 K pull-down	BT_CFG2[4]	
LCD_DATA13	Input with 100 K pull-down	BT_CFG2[5]	
LCD_DATA14	Input with 100 K pull-down	BT_CFG2[6]	
LCD_DATA15	Input with 100 K pull-down	BT_CFG2[7]	
LCD_DATA16	Input with 100 K pull-down	BT_CFG4[0]	
LCD_DATA17	Input with 100 K pull-down	BT_CFG4[1]	
LCD_DATA18	Input with 100 K pull-down	BT_CFG4[2]	
LCD_DATA19	Input with 100 K pull-down	BT_CFG4[3]	
LCD_DATA20	Input with 100 K pull-down	BT_CFG4[4]	
LCD_DATA21	Input with 100 K pull-down	BT_CFG4[5]	
LCD_DATA22	Input with 100 K pull-down	BT_CFG4[6]	
LCD_DATA23	Input with 100 K pull-down	BT_CFG4[7]	

5.2 Boot Device Interface Allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 79. QSPI Boot trough QSPI

Ball Name	Signal Name	Mux Mode	Common	Quad Mode	+ Port A DQS	+ Port A CS1	+ Port B	+ Port B DQS	+ Port B CS1
NAND_WP_B	qspi.A_SCLK	Alt2	Yes	Yes					
NAND_DQS	qspi.A_SS0_B	Alt2	Yes	Yes					

6.1.2 14 x 14 mm Supplies Contact Assignments and Functional Contact Assignments

Table 90 shows the device connection list for ground, sense, and reference contact signals.

Table 90. 14x14 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	M13	—
DRAM_VREF	P4	—
GPANIO	R13	—
NGND_KEL0	M12	—
NVCC_CSI	F4	—
NVCC_DRAM	G6, H6, J6, K6, L6, M6	—
NVCC_DRAM_2P5	N6	—
NVCC_ENET	F13	—
NVCC_GPIO	J13	—
NVCC_LCD	E13	—
NVCC_NAND	E7	—
NVCC_PLL	P13	—
NVCC_SD1	C4	—
NVCC_UART	H13	—
VDD_ARM_CAP	G9, G10, G11, H11	—
VDD_HIGH_CAP	R14, R15	—
VDD_HIGH_IN	N13	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G8, H8, J8, J11, K8, K11, L8, L9, L10, L11	—
VDD_SOC_IN	H9, H10, J9, J10, K9, 10	—
VDD_USB_CAP	R12	—
VDDA_ADC_3P3	L13	—
VSS	A1, A17, C3, C7, C11, C15, E8, E11, F6, F7, F8, F9, F10,F11, F12, G3, G5, G7, G12, G15, H7, H12, J5, J7, J12, K7, K12, L3, L7, L12, M7, M8, M9, M10, M11, N3, N5, R3, R5, R7, R11, R16, R17, T14, U1, U14, U17	—

Table 91. 14 x 14 mm Functional Contact Assignments (continued)

LCD_ENABLE	B8	NVCC_LCD	GPIO	ALT5	GPIO3_IO1	Input	Keeper
LCD_HSYNC	D9	NVCC_LCD	GPIO	ALT5	GPIO3_IO2	Input	Keeper
LCD_RESET	E9	NVCC_LCD	GPIO	ALT5	GPIO3_IO4	Input	Keeper
LCD_VSYNC	C9	NVCC_LCD	GPIO	ALT5	GPIO3_IO3	Input	Keeper
NAND_ALE	B4	NVCC_NAND	GPIO	ALT5	GPIO4_IO10	Input	Keeper
NAND_CE0_B	C5	NVCC_NAND	GPIO	ALT5	GPIO4_IO13	Input	Keeper
NAND_CE1_B	B5	NVCC_NAND	GPIO	ALT5	GPIO4_IO14	Input	Keeper
NAND_CLE	A4	NVCC_NAND	GPIO	ALT5	GPIO4_IO15	Input	Keeper
NAND_DATA00	D7	NVCC_NAND	GPIO	ALT5	GPIO4_IO2	Input	Keeper
NAND_DATA01	B7	NVCC_NAND	GPIO	ALT5	GPIO4_IO3	Input	Keeper
NAND_DATA02	A7	NVCC_NAND	GPIO	ALT5	GPIO4_IO4	Input	Keeper
NAND_DATA03	D6	NVCC_NAND	GPIO	ALT5	GPIO4_IO5	Input	Keeper
NAND_DATA04	C6	NVCC_NAND	GPIO	ALT5	GPIO4_IO6	Input	Keeper
NAND_DATA05	B6	NVCC_NAND	GPIO	ALT5	GPIO4_IO7	Input	Keeper
NAND_DATA06	A6	NVCC_NAND	GPIO	ALT5	GPIO4_IO8	Input	Keeper
NAND_DATA07	A5	NVCC_NAND	GPIO	ALT5	GPIO4_IO9	Input	Keeper
NAND_DQS	E6	NVCC_NAND	GPIO	ALT5	GPIO4_IO16	Input	Keeper
NAND_RE_B	D8	NVCC_NAND	GPIO	ALT5	GPIO4_IO0	Input	Keeper
NAND_READY_B	A3	NVCC_NAND	GPIO	ALT5	GPIO4_IO12	Input	Keeper
NAND_WE_B	C8	NVCC_NAND	GPIO	ALT5	GPIO4_IO1	Input	Keeper
NAND_WP_B	D5	NVCC_NAND	GPIO	ALT5	GPIO4_IO11	Input	Keeper
ONOFF	R8	VDD_SNVS_IN	SRC	ALT0	SRC_RESET_B	Input	100 kΩ pull-up
POR_B	P8	VDD_SNVS_IN	SRC	ALT0	SRC_POR_B	Input	100 kΩ pull-up
RTC_XTALI	T11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALI	—	—
RTC_XTALO	U11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALO	—	—
SD1_CLK	C1	NVCC_SD	GPIO	ALT5	GPIO2_IO17	Input	Keeper
SD1_CMD	C2	NVCC_SD	GPIO	ALT5	GPIO2_IO16	Input	Keeper
SD1_DATA0	B3	NVCC_SD	GPIO	ALT5	GPIO2_IO18	Input	Keeper
SD1_DATA1	B2	NVCC_SD	GPIO	ALT5	GPIO2_IO19	Input	Keeper
SD1_DATA2	B1	NVCC_SD	GPIO	ALT5	GPIO2_IO20	Input	Keeper
SD1_DATA3	A2	NVCC_SD	GPIO	ALT5	GPIO2_IO21	Input	Keeper

Table 95. 9x9 mm, 0.5 mm Pitch, Ball Map (continued)

	U	T	R
1	VSS	DRAM_VREF	DRAM_DM1
2	DRAM_DATA09	DRAM_ZQPAD	DRAM_DATA11
3	DRAM_DATA07	DRAM_DATA00	VSS
4	DRAM_DQM0	DRAM_DATA02	DRAM_DATA06
5	DRAM_DATA04	DRAM_DATA03	DRAM_SDQS0_N
6	VSS	DRAM_DATA05	ONOFF
7	CCM_PMIC_STBY_REQ	SNVS_PMIC_ON_REQ	SNVS_TAMPER6
8	BOOT_MODE1	BOOT_MODE0	SNVS_TAMPER0
9	USB_OTG2_VBUS	USB_OTG1_VBUS	VSS
10	USB_OTG2_DP	USB_OTG2_DN	POR_B
11	VDD_HIGH_CAP	GPANAIO	USB_OTG1_DN
12	RTC_XTALO	RTC_XTALI	VSS
13	VSS	NVCC_PLL	JTAG_MOD
14	XTALO	XTALI	JTAG_TMS
15	VDD_HIGH_IN	USB_OTG1_CHD_B	VSS
16	CCM_CLK1_N	CCM_CLK1_P	JTAG_TDO
17	VSS	VDDA_ADC_3P3	JTAG_TCK
	U	T	R