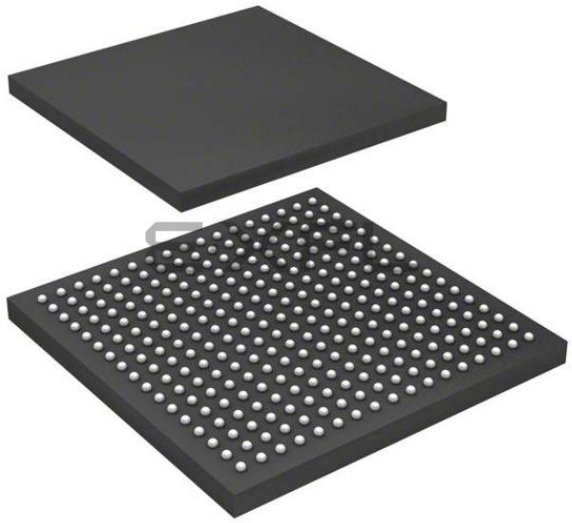

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y2cvm05ab

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPDC	Electrophoretic Display Controller	Multimedia Peripherals	The EPDC is a feature-rich, low power, and high performance direct-drive active matrix EPD controller. It is specially designed to drive E-INK^{TM} EPD panels, supporting a wide variety of TFT backplanes.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.
RNGB	Random Number Generator	Security	Random number generating module.
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 15. Low Power Mode Current and Power Consumption (continued)

SYSTEM IDLE: LDO Enabled	• LDO_ARM and LDO_SOC are set to 1.15 V • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.325 V)	9	mA
		VDD_HIGH_IN (3.0 V)	9.7	
		VDD_SNVS_IN (3.0 V)	0.04	
		Total	41.15	mW
SYSTEM IDLE: LDO Bypassed	• LDO_ARM and LDO_SOC are set to bypass mode • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.25 V)	8.5	mA
		VDD_HIGH_IN (3.0 V)	8.8	
		VDD_SNVS_IN (3.0 V)	0.04	
		Total	37.15	mW
LOW POWER IDLE: LDO Enabled	• LDO_SOC is set to 1.15 V, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (1.025 V)	1.6	mA
		VDD_HIGH_IN (3.0 V)	1.25	
		VDD_SNVS_IN (3.0 V)	0.03	
		Total	5.48	mW
LOW POWER IDLE: LDO Bypassed	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (0.9 V)	1.5	mA
		VDD_HIGH_IN (3.0 V)	0.3	
		VDD_SNVS_IN (3.0 V)	0.05	
		Total	2.4	mW
SUSPEND:	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are shut off • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • High-speed peripheral are powered off	VDD_SOC_IN (0.9 V)	0.3	mA
		VDD_HIGH_IN (3.0 V)	0.03	
		VDD_SNVS_IN (3.0 V)	0.03	
		Total	0.45	mW
SNVS:	• All SOC digital logic, analog module are shut off • 32 kHz RTC is alive • Tamper detection circuit remains active	VDD_SOC_IN (0 V)	0	mA
		VDD_HIGH_IN (0 V)	0	
		VDD_SNVS_IN (3.0 V)	0.03	
		Total	0.09	mW

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	22 pF Cload, slow slew rate 22 pF Cload, fast slew rate	—	—	1.84/2.06 1.09/1.35	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	22 pF Cload, slow slew rate 22 pF Cload, fast slew rate	—	—	2.44/2.75 1.75/2.02	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	22 pF Cload, slow slew rate 22 pF Cload, fast slew rate	—	—	3.26/3.70 2.47/2.92	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	22 pF Cload, slow slew rate 22 pF Cload, fast slew rate	—	—	5.26/6.19 4.88/5.77	ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes. For details on supported DDR memory configurations, see Section 4.10, "Multi-Mode DDR Controller (MMDC)".

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6ULL Applications Processor* (IMX6ULLHDG).

Table 31 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns

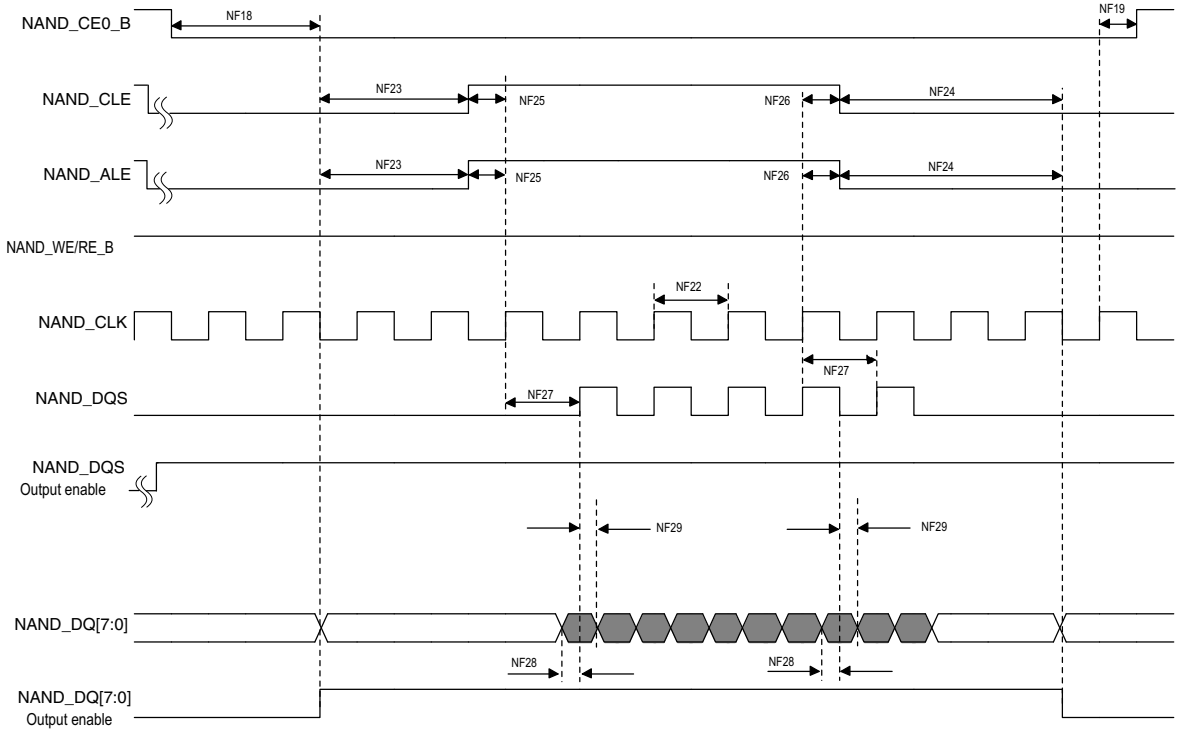

Figure 27. Source Synchronous Mode Data Write Timing Diagram

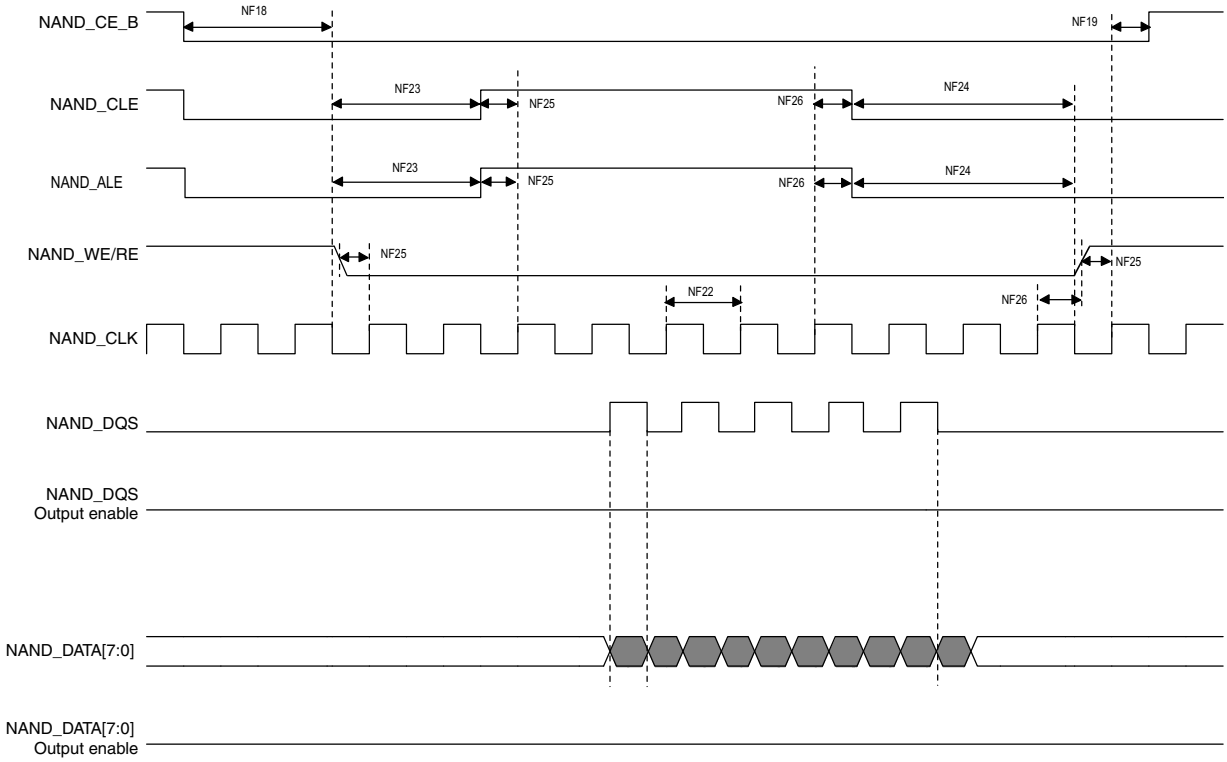

Figure 28. Source Synchronous Mode Data Read Timing Diagram

4.12.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.12.2.1 ECSPI Master Mode Timing

Figure 35 depicts the timing of ECSPI in master mode. Table 47 lists the ECSPI master mode timing characteristics.

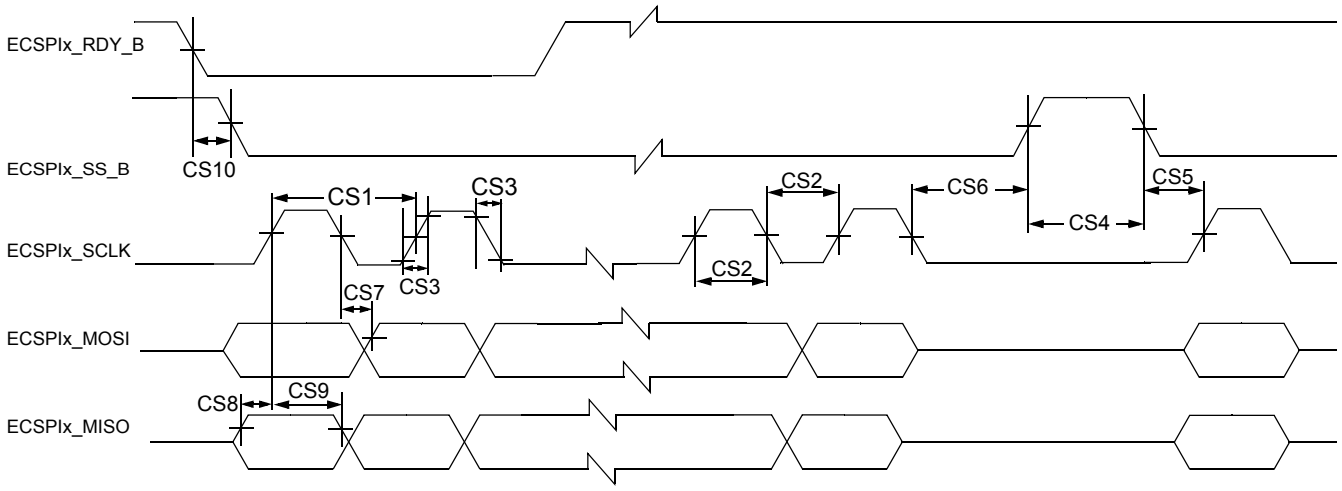

Figure 35. ECSPI Master Mode Timing Diagram

Table 47. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	14	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.7, “I/O AC Parameters”.”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

Table 49. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before ESAI_RX_CLK falling edge	— —	— —	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after ESAI_RX_CLK falling edge	— —	— —	6.0 0.0	— —	x ck i ck s	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 49. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
85	ESAI_TX_CLK rising edge to transmitter #0 drive enable assertion	— —	— —	— —	17.0 11.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
88	ESAI_TX_CLK rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	14.0 9.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
92	ESAI_TX_FS input (wl) to data out enable from high impedance	—	—	—	21.0	—	ns
93	ESAI_TX_FS input (wl) to transmitter #0 drive enable assertion	—	—	—	14.0	—	ns
94	Flag output valid after ESAI_TX_CLK rising edge	—	—	— —	14.0 9.0	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

4.12.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.12.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 40 depicts the timing of SD/eMMC4.3, and Table 50 lists the SD/eMMC4.3 timing characteristics.

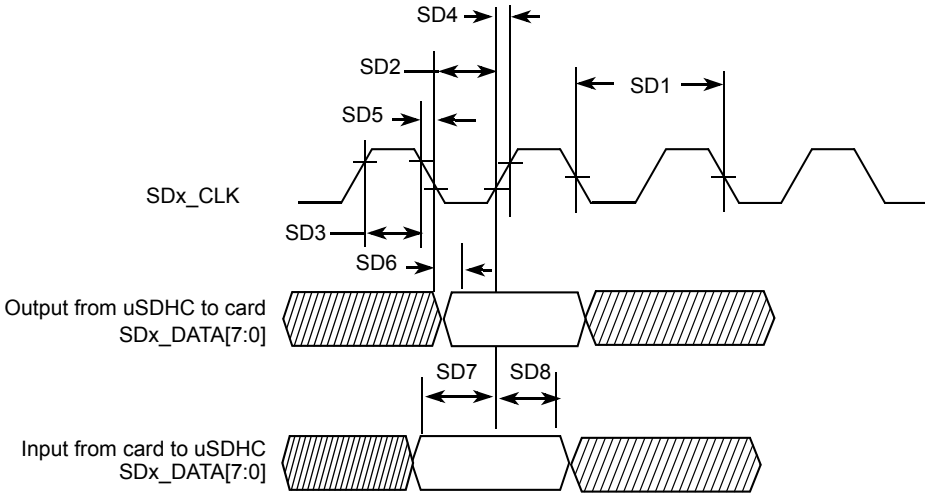

Figure 40. SD/eMMC4.3 Timing

Table 50. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

4.12.9 LCD Controller (LCDIF) Parameters

Figure 50 shows the LCDIF timing and Table 60 lists the timing parameters.

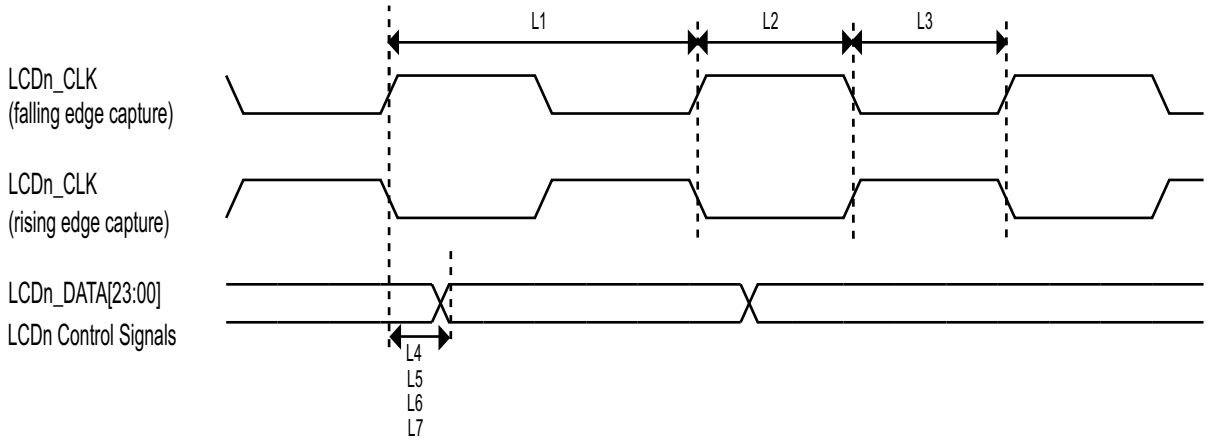

Figure 50. LCD Timing

Table 60. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	150	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.12.9.1 LCDIF Signal Mapping

Table 61 lists the details about the mapping signals.

Table 61. LCD Timing Parameters

Pin name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	—	—	—	—	CCIR_CLK
LCD_VSYNC* (Two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	—
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	—
LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	—

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

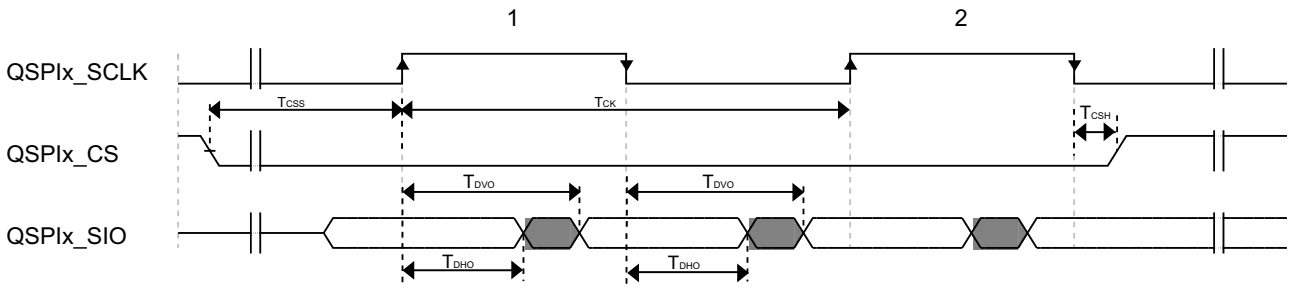

Figure 56. QuadSPI Output/Write Timing (DDR mode)

Table 67. QuadSPI Output/Write Timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	(0.25 x T_{SCLK}) + 2	ns
T_{DHO}	Output data hold time	(0.25 x T_{SCLK}) - 0.5	—	ns
T_{CK}	SCK clock period	20	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6ULL Reference Manual (IMX6ULLRM)* for more details.

4.12.11 SAI/I2S Switching Specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 68. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	2 x t_{sys}	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	4 x t_{sys}	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period

Table 76. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

1 Typical values assume VDDAD = 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential differences

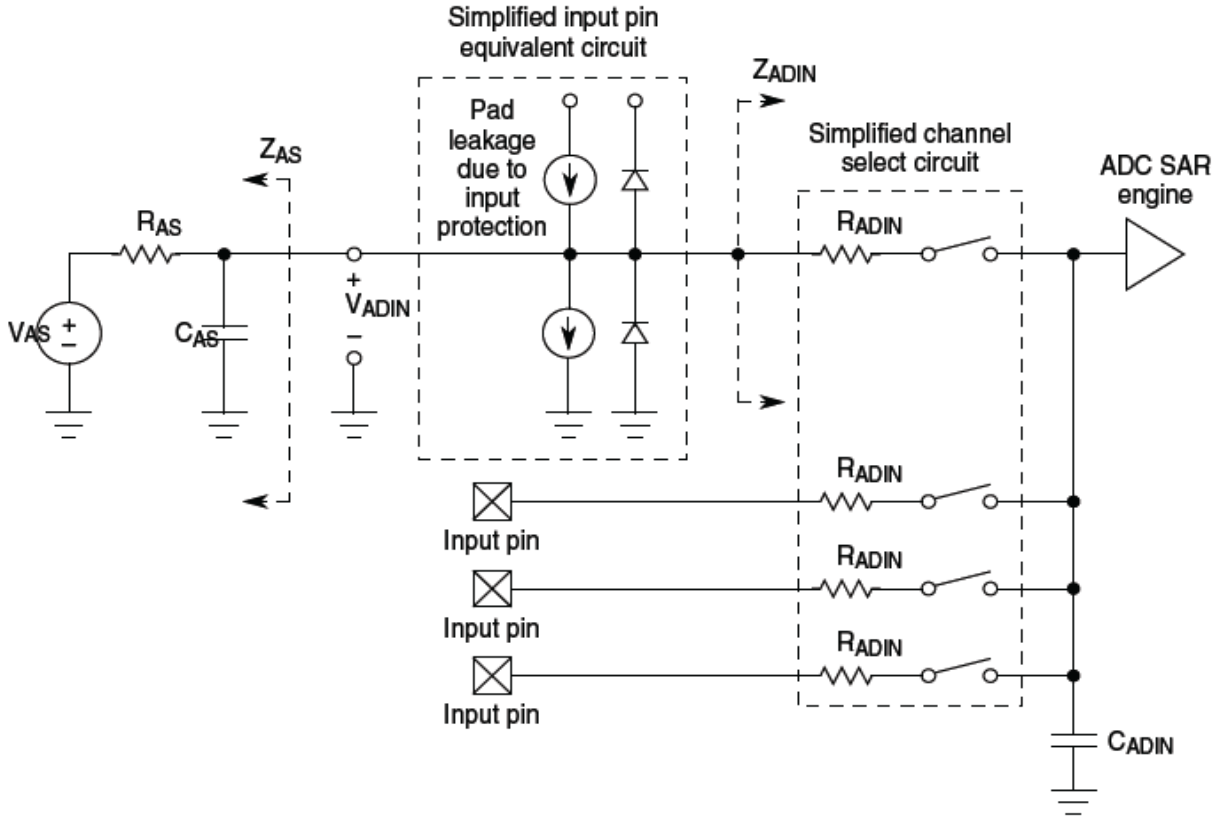

Figure 69. 12-bit ADC Input Impedance Equivalency Diagram

Table 78. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	Details
LCD_DATA00	Input with 100 K pull-down	BT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DATA01	Input with 100 K pull-down	BT_CFG1[1]	
LCD_DATA02	Input with 100 K pull-down	BT_CFG1[2]	
LCD_DATA03	Input with 100 K pull-down	BT_CFG1[3]	
LCD_DATA04	Input with 100 K pull-down	BT_CFG1[4]	
LCD_DATA05	Input with 100 K pull-down	BT_CFG1[5]	
LCD_DATA06	Input with 100 K pull-down	BT_CFG1[6]	
LCD_DATA07	Input with 100 K pull-down	BT_CFG1[7]	
LCD_DATA08	Input with 100 K pull-down	BT_CFG2[0]	
LCD_DATA09	Input with 100 K pull-down	BT_CFG2[1]	
LCD_DATA10	Input with 100 K pull-down	BT_CFG2[2]	
LCD_DATA11	Input with 100 K pull-down	BT_CFG2[3]	
LCD_DATA12	Input with 100 K pull-down	BT_CFG2[4]	
LCD_DATA13	Input with 100 K pull-down	BT_CFG2[5]	
LCD_DATA14	Input with 100 K pull-down	BT_CFG2[6]	
LCD_DATA15	Input with 100 K pull-down	BT_CFG2[7]	
LCD_DATA16	Input with 100 K pull-down	BT_CFG4[0]	
LCD_DATA17	Input with 100 K pull-down	BT_CFG4[1]	
LCD_DATA18	Input with 100 K pull-down	BT_CFG4[2]	
LCD_DATA19	Input with 100 K pull-down	BT_CFG4[3]	
LCD_DATA20	Input with 100 K pull-down	BT_CFG4[4]	
LCD_DATA21	Input with 100 K pull-down	BT_CFG4[5]	
LCD_DATA22	Input with 100 K pull-down	BT_CFG4[6]	
LCD_DATA23	Input with 100 K pull-down	BT_CFG4[7]	

5.2 Boot Device Interface Allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 79. QSPI Boot trough QSPI

Ball Name	Signal Name	Mux Mode	Common	Quad Mode	+ Port A DQS	+ Port A CS1	+ Port B	+ Port B DQS	+ Port B CS1
NAND_WP_B	qspi.A_SCLK	Alt2	Yes	Yes					
NAND_DQS	qspi.A_SS0_B	Alt2	Yes	Yes					

Table 84. NAND Boot through GPMI (continued)

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_WE_B	rawnand.WE_B	Alt 0	Yes		
NAND_DATA00	rawnand.DATA00	Alt 0	Yes		
NAND_DATA01	rawnand.DATA01	Alt 0	Yes		
NAND_DATA02	rawnand.DATA02	Alt 0	Yes		
NAND_DATA03	rawnand.DATA03	Alt 0	Yes		
NAND_DATA04	rawnand.DATA04	Alt 0	Yes		
NAND_DATA05	rawnand.DATA05	Alt 0	Yes		
NAND_DATA06	rawnand.DATA06	Alt 0	Yes		
NAND_DATA07	rawnand.DATA07	Alt 0	Yes		
NAND_DQS	rawnand.DQS	Alt 0	Yes		
CSI_MCLK	rawnand.CE2_B	Alt 2			Yes
CSI_PIXCLK	rawnand.CE3_B	Alt 2			Yes

Table 85. SD/MMC Boot through USDHC1

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)	SDMMC MFG mode
UART1_RTS_B	usdhc1.CD_B	Alt 2					Yes
SD1_CLK	usdhc1.CLK	Alt 0	Yes				
SD1_CMD	usdhc1.CMD	Alt 0	Yes				
SD1_DATA0	usdhc1.DATA0	Alt 0	Yes				
SD1_DATA1	usdhc1.DATA1	Alt 0		Yes	Yes		
SD1_DATA2	usdhc1.DATA2	Alt 0		Yes	Yes		
SD1_DATA3	usdhc1.DATA3	Alt 0	Yes				
NAND_READY_B	usdhc1.DATA4	Alt 1			Yes		
NAND_CE0_B	usdhc1.DATA5	Alt 1			Yes		
NAND_CE1_B	usdhc1.DATA6	Alt 1			Yes		
NAND_CLE	usdhc1.DATA7	Alt 1			Yes		
GPIO1_IO09	GPIO1_IO09[1]	Alt 5				Yes	
GPIO1_IO05	usdhc1.VSELECT	Alt 4				Yes	

[1] The Boot ROM uses GPIO1_IO09 to implement SD1_RESET_B.

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14 x 14 mm Package Information

6.1.1 14 x 14 mm, 0.8 mm Pitch, Ball Matrix

Figure 70 shows the top, bottom, and side views of the 14 x 14 mm BGA package.

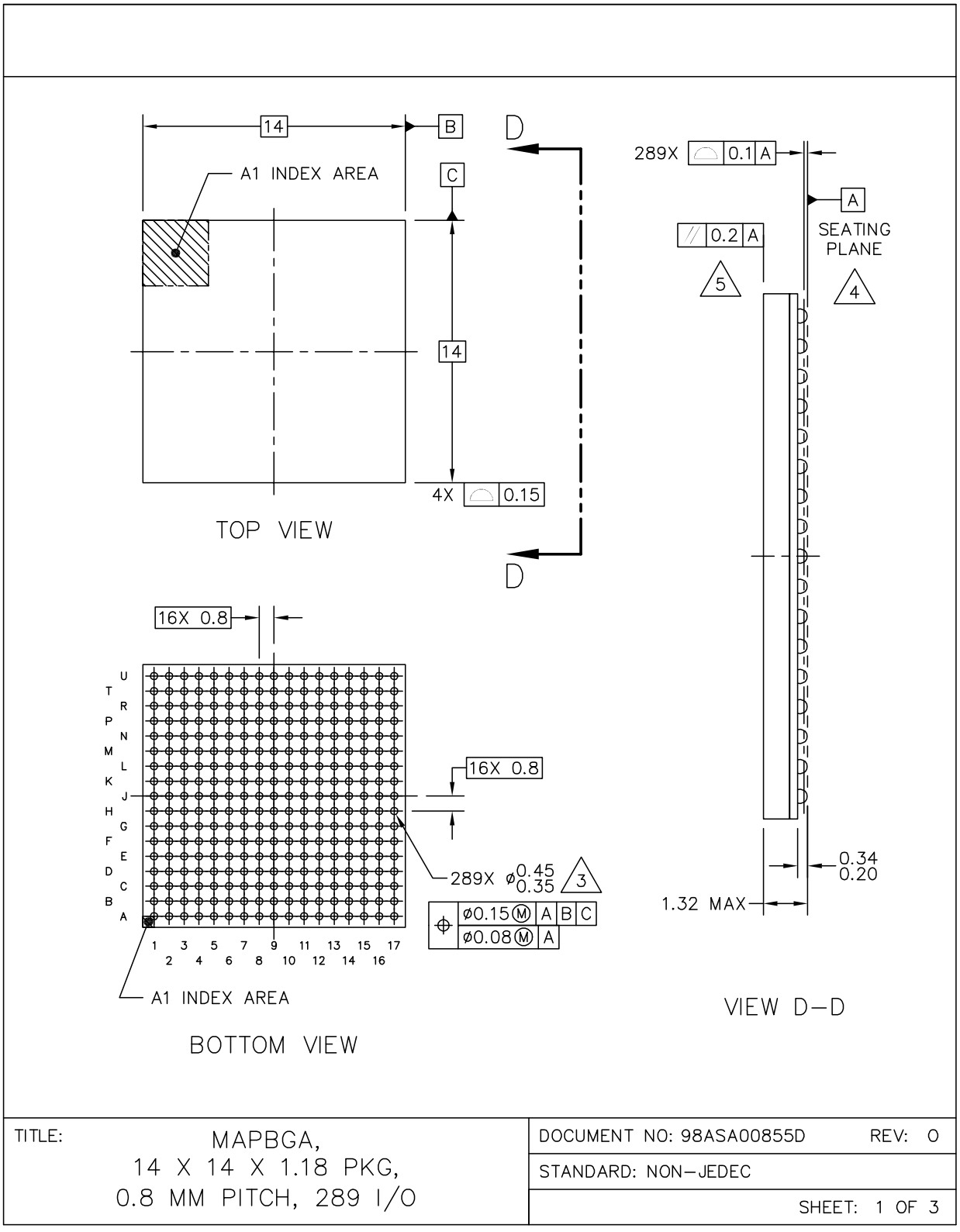

Figure 70. 14 x 14 mm BGA, Case x Package Top, Bottom, and Side Views

Table 91. 14 x 14 mm Functional Contact Assignments (continued)

DRAM_SDQS0_P	P6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	100 kΩ pull-down
DRAM_SDQS1_N	T2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_N	Input	100 kΩ pull-down
DRAM_SDQS1_P	T1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	100 kΩ pull-down
DRAM_SDWE_B	J1	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	100 kΩ pull-up
DRAM_ZQPAD	N4	NVCC_DRAM	GPIO	—	DRAM_ZQPAD	Input	Keeper
ENET1_RX_DATA0	F16	NVCC_ENET	GPIO	ALT5	GPIO2_IO0	Input	Keeper
ENET1_RX_DATA1	E17	NVCC_ENET	GPIO	ALT5	GPIO2_IO1	Input	Keeper
ENET1_RX_EN	E16	NVCC_ENET	GPIO	ALT5	GPIO2_IO2	Input	Keeper
ENET1_RX_ER	D15	NVCC_ENET	GPIO	ALT5	GPIO2_IO7	Input	Keeper
ENET1_TX_CLK	F14	NVCC_ENET	GPIO	ALT5	GPIO2_IO6	Input	Keeper
ENET1_TX_DATA0	E15	NVCC_ENET	GPIO	ALT5	GPIO2_IO3	Input	Keeper
ENET1_TX_DATA1	E14	NVCC_ENET	GPIO	ALT5	GPIO2_IO4	Input	Keeper
ENET1_TX_EN	F15	NVCC_ENET	GPIO	ALT5	GPIO2_IO5	Input	Keeper
ENET2_RX_DATA0	C17	NVCC_ENET	GPIO	ALT5	GPIO2_IO8	Input	Keeper
ENET2_RX_DATA1	C16	NVCC_ENET	GPIO	ALT5	GPIO2_IO9	Input	Keeper
ENET2_RX_EN	B17	NVCC_ENET	GPIO	ALT5	GPIO2_IO10	Input	Keeper
ENET2_RX_ER	D16	NVCC_ENET	GPIO	ALT5	GPIO2_IO15	Input	Keeper
ENET2_TX_CLK	D17	NVCC_ENET	GPIO	ALT5	GPIO2_IO14	Input	Keeper
ENET2_TX_DATA0	A15	NVCC_ENET	GPIO	ALT5	GPIO2_IO11	Input	Keeper
ENET2_TX_DATA1	A16	NVCC_ENET	GPIO	ALT5	GPIO2_IO12	Input	Keeper
ENET2_TX_EN	B15	NVCC_ENET	GPIO	ALT5	GPIO2_IO13	Input	Keeper
GPIO1_IO00	K13	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	L15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	L14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	L17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	M16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	M17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	K17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	L16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	N17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	M15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper

Table 94. 9 x 9 mm Functional Contact Assignments (continued)

DRAM_ADDR07	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	J1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	E3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	E2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	G4	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	L1	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T3	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	N5	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	P1	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 94. 9 x 9 mm Functional Contact Assignments (continued)

JTAG_MOD	R13	NVCC_GPIO	SJC	ALT0	SJC_MOD	Input	100 kΩ pull-up
JTAG_TCK	R17	NVCC_GPIO	SJC	ALT0	SJC_TCK	Input	47 kΩ pull-up
JTAG_TDI	P17	NVCC_GPIO	SJC	ALT0	SJC_TDI	Input	47 kΩ pull-up
JTAG_TDO	R16	NVCC_GPIO	SJC	ALT0	SJC_TDO	Output	Keeper
JTAG_TMS	R14	NVCC_GPIO	SJC	ALT0	SJC_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	P13	NVCC_GPIO	SJC	ALT0	SJC_TRSTB	Input	47 kΩ pull-up
LCD_CLK	C11	NVCC_LCD	GPIO	ALT5	GPIO3_IO0	Input	Keeper
LCD_DATA00	D11	NVCC_LCD	GPIO	ALT5	GPIO3_IO5	Input	Keeper
LCD_DATA01	B12	NVCC_LCD	GPIO	ALT5	GPIO3_IO6	Input	Keeper
LCD_DATA02	D10	NVCC_LCD	GPIO	ALT5	GPIO3_IO7	Input	Keeper
LCD_DATA03	B11	NVCC_LCD	GPIO	ALT5	GPIO3_IO8	Input	Keeper
LCD_DATA04	A11	NVCC_LCD	GPIO	ALT5	GPIO3_IO9	Input	Keeper
LCD_DATA05	D12	NVCC_LCD	GPIO	ALT5	GPIO3_IO10	Input	Keeper
LCD_DATA06	D13	NVCC_LCD	GPIO	ALT5	GPIO3_IO11	Input	Keeper
LCD_DATA07	C12	NVCC_LCD	GPIO	ALT5	GPIO3_IO12	Input	Keeper
LCD_DATA08	B13	NVCC_LCD	GPIO	ALT5	GPIO3_IO13	Input	Keeper
LCD_DATA09	A13	NVCC_LCD	GPIO	ALT5	GPIO3_IO14	Input	Keeper
LCD_DATA10	D14	NVCC_LCD	GPIO	ALT5	GPIO3_IO15	Input	Keeper
LCD_DATA11	C13	NVCC_LCD	GPIO	ALT5	GPIO3_IO16	Input	Keeper
LCD_DATA12	C14	NVCC_LCD	GPIO	ALT5	GPIO3_IO17	Input	Keeper
LCD_DATA13	A14	NVCC_LCD	GPIO	ALT5	GPIO3_IO18	Input	Keeper
LCD_DATA14	B14	NVCC_LCD	GPIO	ALT5	GPIO3_IO19	Input	Keeper
LCD_DATA15	A16	NVCC_LCD	GPIO	ALT5	GPIO3_IO20	Input	Keeper
LCD_DATA16	A15	NVCC_LCD	GPIO	ALT5	GPIO3_IO21	Input	Keeper
LCD_DATA17	D15	NVCC_LCD	GPIO	ALT5	GPIO3_IO22	Input	Keeper
LCD_DATA18	B15	NVCC_LCD	GPIO	ALT5	GPIO3_IO23	Input	Keeper
LCD_DATA19	E12	NVCC_LCD	GPIO	ALT5	GPIO3_IO24	Input	Keeper
LCD_DATA20	B17	NVCC_LCD	GPIO	ALT5	GPIO3_IO25	Input	Keeper
LCD_DATA21	C16	NVCC_LCD	GPIO	ALT5	GPIO3_IO26	Input	Keeper
LCD_DATA22	B16	NVCC_LCD	GPIO	ALT5	GPIO3_IO27	Input	Keeper
LCD_DATA23	C17	NVCC_LCD	GPIO	ALT5	GPIO3_IO28	Input	Keeper

Table 95. 9x9 mm, 0.5 mm Pitch, Ball Map (continued)

P	N	M	L	K	J	H
DRAM_DATA08	DRAM_DATA14	VSS	DRAM_CS0_B	DRAM_SDCKE1	DRAM_ADDR09	DRAM_ADDR02
DRAM_DATA15	DRAM_DATA13	DRAM_ADDR10	DRAM_SDCKE0	DRAM_ODT0	DRAM_ADDR03	DRAM_ADDR05
DRAM_DATA10	DRAM_SDQS1_P	VSS	DRAM_ADDR12	DRAM_SDCLK0_P	VSS	DRAM_SDBA0
DRAM_DATA12	DRAM_SDQS1_N	DRAM_ADDR04	DRAM_RAS_B	DRAM_SDCLK0_N	DRAM_ADDR07	DRAM_ADDR13
DRAM_SDQS0_P	DRAM_DATA01	NVCC_DRAM	NVCC_DRAM	DRAM_ADDR11	DRAM_ADDR08	DRAM_CSI_B
SNVS_TAMPER1	NVCC_DRAM			NVCC_DRAM_2P5		VSS
SNVS_TAMPER4	TEST_MODE		VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER5	SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER9	SNVS_TAMPER7		VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER3	SNVS_DAMPER2	NGND_KEL0	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
USB_OTG1_DP	VDD_USB_CAP		VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
VDD_SNVS_IN	VDD_SNVS_CAP			VSS		VSS
JTAG_TRST_B	ADC_VREFH	NVCC_GPIO	NVCC_UART	UART5_TX_DATA	UART5_RX_DATA	ENET2_RX_ER
GPIO1_IO08	GPIO1_IO07	GPIO1_IO00	UART1_CTS_B	UART1_RTS_B	UART2_RTS_B	ENET2_TX_CLK
GPIO1_IO05	GPIO1_IO06	GPIO_IO01	UART1_TX_DATA	UART3_RX_DATA	VSS	UART3_RTS_B
GPIO1_IO09	GPIO1_IO03	GPIO1_IO02	UART2_TX-DATA	UART2_RX_DATA	UART4_TX_DATA	UART3_CTS_B
JTAG_TDI	GPIO1_IO04	VSS	UART1_RX_DATA	UART3_TX_DATA	UART2_CTS_B	UART4_RX_DATA
P	N	M	L	K	J	H