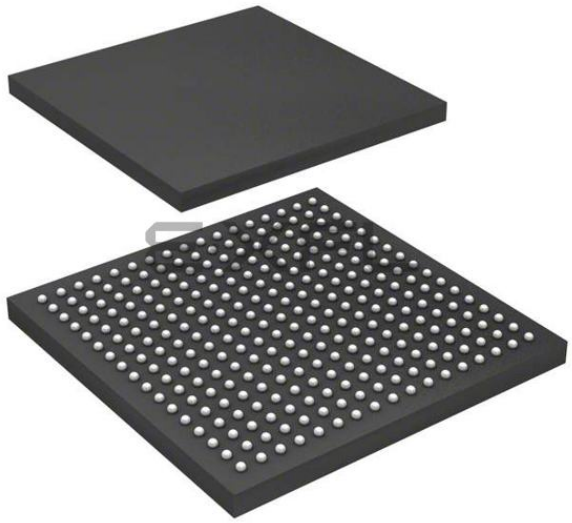

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	792MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y2cvm08ab

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6ULL features, see Section 1.2, “Features"”.

1.1 Ordering Information

Table 1 provides examples of orderable part numbers covered by this data sheet.

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y0CVM05AA MCIMX6Y0CVM05AB	Features supports: • 528 MHz, industrial grade for general purpose • No security • No LCD/CSI • No CAN • Ethernet x1 • USB OTG x1 • ADC x1 • UART x4 • SAI x1 • No ESAI • Timer x2 • PWM x4 • I2C x2 • SPI x2	14 x 14 mm, 0.8 pitch MAPBGA	-40 to +105
MCIMX6Y1CVM05AA MCIMX6Y1CVM05AB	Features supports: • 528 MHz, industrial grade for general purpose • Basic security • No LCD/CSI • CAN x1 • Ethernet x1 • USB OTG x2 • ADC x1 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14 mm, 0.8 pitch MAPBGA	-40 to +105

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y1CVK05AA MCIMX6Y1CVK05AB	Features supports: • 528 MHz, industrial grade for general purpose • Basic security • No LCD/CSI • CAN x1 • Ethernet x1 • USB OTG x2 • ADC x1 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	9 x 9 mm, 0.5 pitch MAPBGA	-40 to +105
MCIMX6Y2CVM05AA MCIMX6Y2CVM05AB	Features supports: • 528 MHz, industrial grade for general purpose • Basic security • With LCD/CSI • CAN x2 • Ethernet x2 • USB OTG x2 • ADC x2 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14mm, 0.8 pitch MAPBGA	-40 to +105

Table 8. 14 x 14 (VM) Thermal Resistance Data (continued)

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	48.6	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	32.9	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	21.8	°C/W	4
Junction to Case	—	$R_{\theta JC}$	19.3	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2.3	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB}	12.0	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB

4.1.2.2 9 x 9 MM (VK) Package Thermal Resistance

Table 9 displays the 9 x 9 MM (VK) thermal resistance data.

Table 9. 9 x 9 MM (VK) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single-layer board (1s)	$R_{\theta JA}$	65.6	°C/W	1,2
Junction to Ambient Natural Convection	Four-layer board (2s2p)	$R_{\theta JA}$	36.2	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	51.2	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	31.8	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	17.1	°C/W	4
Junction to Case	—	$R_{\theta JC}$	14.5	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.6	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB_CSB}	11.1	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistances between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

4.1.3 Operating Ranges

Table 10 provides the operating ranges of the i.MX 6ULL processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6ULL Reference Manual* (IMX6ULLRM).

Table 10. Operating Ranges

Parameter Description	Symbol	Operating Conditions	Min	Typ	Max[1]	Unit	Comment
Run Mode: LDO Enabled	VDD_SOC_IN	A7 core at 792 MHz	1.325	—	1.5	V	VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point (VDD_ARM_CAP and VDD_SOC_CAP) for correct supply voltage regulation.
		A7 core at 528 MHz and below	1.275	—	1.5		
	VDD_ARM_CAP	A7 core at 792 MHz	1.2		1.26	V	—
		A7 core at 528 MHz	1.15	—	1.26		
		A7 core at 396 MHz	1.00	—	1.26		
		A7 core at 198 MHz	0.925	—	1.26		
	VDD_SOC_CAP	—	1.15	—	1.26	V	—
Run Mode: LDO Bypassed	VDD_SOC_IN	A7 core operations at 528 MHz or below.	1.15	—	1.26	V	A7 core operation above 528 MHz is not supported when LDO is bypassed.

Table 14. Power Supply State in Power Modes

Power Rail	RUN	Low Power	SNVS	OFF
VDD_SOC_IN	ON	ON	OFF	OFF
VDD_HIGH_IN	ON	ON	OFF	OFF
VDD_SNVS	ON	ON	ON	OFF
USB_OTG1_VBUS USB_OTG2_VBUS	ON / OFF	ON / OFF	OFF	OFF
NVCC_DRAM_2P5	ON	ON	OFF	OFF
VDDA_ADC_3P3	ON / OFF	ON / OFF	OFF	OFF
NVCC_DRAM	ON	ON	OFF	OFF
NVCC_XXX	ON / OFF	ON / OFF	OFF	OFF

4.1.6.1 RUN Mode

In RUN mode, the CPU is active and running, and the analog / digital peripheral modules inside the processor will be enabled. In this mode, all the external power rails to the processor have to be ON and the

SoC will be able to draw as many current.

Typically, when the CPU is doing DVFS, it switches the VDD_ARM voltage according to Table 10.

4.1.6.2 Low Power Mode

When the CPU is not running, the processor can enter low power mode. i.MX 6ULL processor supports a very flexible set of power mode configurations in low power mode.

Typically there are three low power modes used, System IDLE, Low Power IDLE, and SUSPEND:

- System IDLE—This is a mode that the CPU can automatically enter when there is no thread running. All the peripherals can keep working and the CPU's state is retained so the interrupt response can be very short. The cores are able to individually enter the WAIT state.
- Low Power IDLE—This mode is for the case when the system needs to have lower power but still keep some of the peripherals alive. Most of the peripherals, analog modules, and PHYs are shut off. The interrupt response in this mode is expected to be longer than the System IDLE, but its power is much lower.
- Suspend—This mode has the greatest power savings; all clocks, unused analog/PHYs, and peripherals are off. The external DRAM stays in Self-Refresh mode. The exit time from this mode is much longer.

Table 15 shows the current core consumption (not including I/O) of i.MX 6ULL processors in selected low power modes.

Table 15. Low Power Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical	Units

[1] The DC parameters are for external clock input only.

4.6.2 Single Voltage General Purpose I/O (GPIO) DC Parameters

Table 24 shows DC parameters for GPIO pads. The parameters in Table 24 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 24. Single Voltage GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (ipp_dse=001,010) Ioh= -1mA (ipp_dse=011,100,101,110,111)	OVDD-0.15	–	V
Low-level output voltage[1]	VOL	Iol= 0.1mA (ipp_dse=001,010) Iol= 1mA (ipp_dse=011,100,101,110,111)	–	0.15	V
High-Level input voltage[1,2]	VIH	—	0.7 x OVDD	OVDD	V
Low-Level input voltage[1,2]	VIL	—	0	0.3 x OVDD	V
Input Hysteresis (OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	200	—	mV
Input Hysteresis (OVDD=3.3V	VHYS_HighVDD	OVDD=3.3V	200	—	mV
Schmitt trigger VT+[2,3]	VTH+	—	0.5 x OVDD	—	mV
Schmitt trigger VT-[2,3]	VTH-	—	—	0.5 x OVDD	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V	—	212	uA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=OVDD	—	1	uA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V	—	100	uA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=oOVDD	—	1	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V	—	48	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=OVDD	—	1	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=OVDD	—	48	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V	—	1	uA
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD	-1	1	uA
Keeper Circuit Resistance	R_Keeper	VI =0.3 x OVDD, VI = 0.7 x OVDD	105	175	kΩ

[1] Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

[2] To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

[3] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω ± 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω ± 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6ULL processors for the following I/O types:

- Single Voltage General Purpose I/O (GPIO)

- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

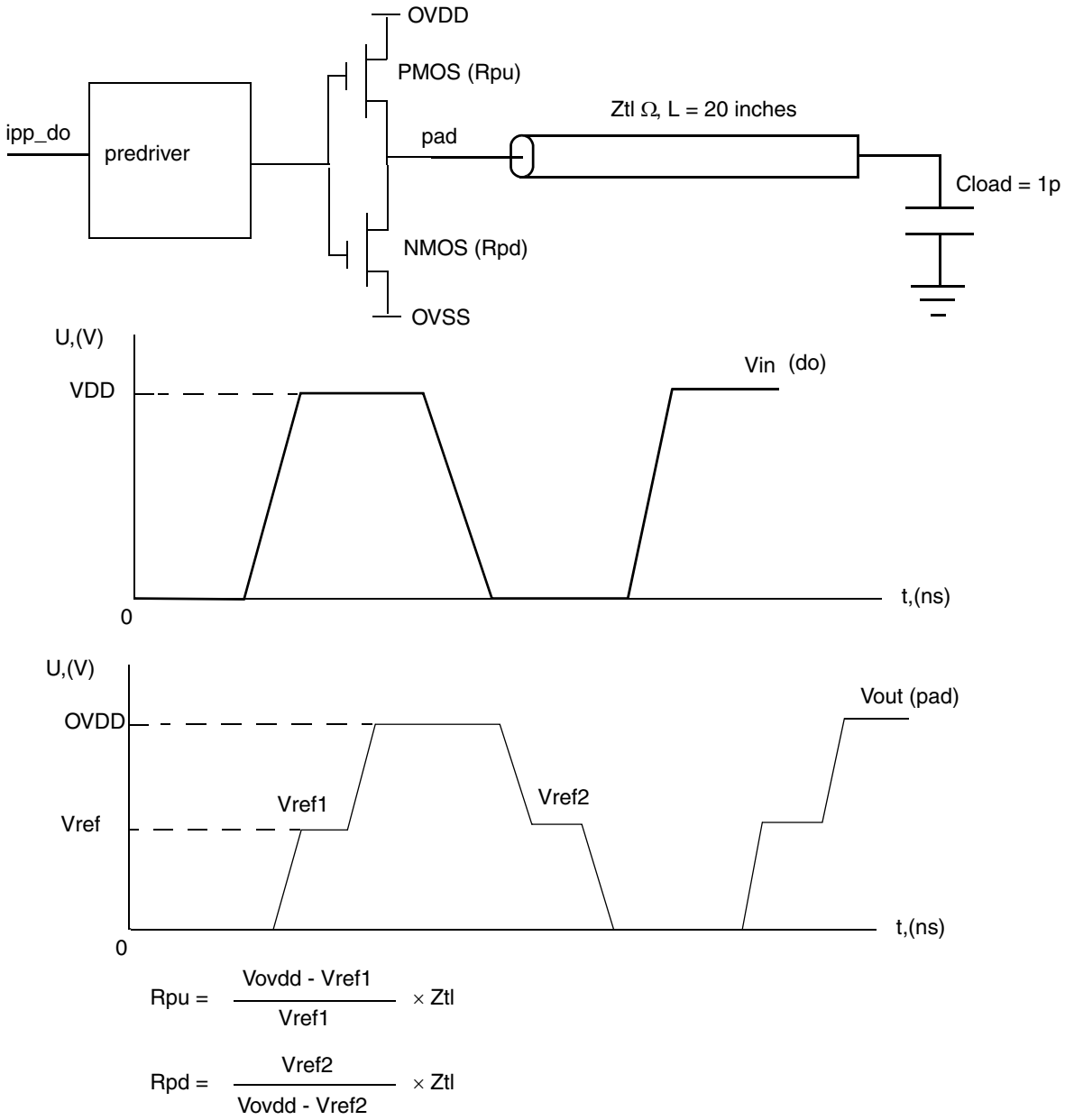

Figure 6. Impedance Matching Load for Measurement

Table 39. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

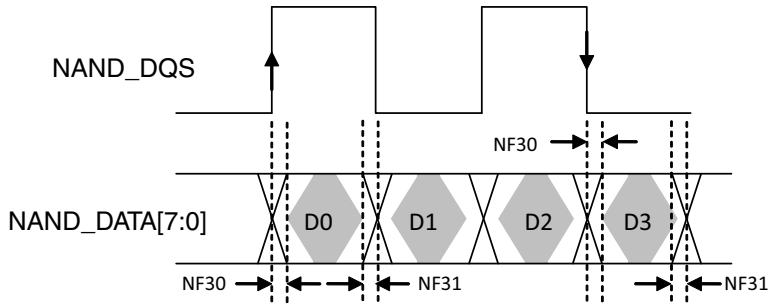

Figure 29. NAND_DQS/NAND_DQ Read Valid Window

Table 43. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see [2]]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see [2]]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	Clock period	tCK	—		ns
NF23	Preamble delay	tPRE	PRE_DELAY × T - 0.29 [see [2]]		ns
NF24	Postamble delay	tPOST	POST_DELAY × T - 0.78 [see [2]]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see [2]]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		—
NF29	Data write hold	—	0.25 × tCK - 0.85		—
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	—

1 GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK(GPMI clock period) -0.075ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6ULL Reference Manual*). Generally, the typical delay value of this register is equal to 0x7 which means 1/4

Table 49. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before ESAI_RX_CLK falling edge	— —	— —	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after ESAI_RX_CLK falling edge	— —	— —	6.0 0.0	— —	x ck i ck s	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

4.12.7 I²C Bus Characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

4.12.8 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 49 depicts the timing of the PWM, and Table 59 lists the PWM timing parameters.

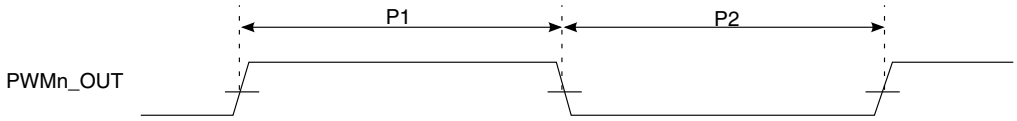

Figure 49. PWM Timing

Table 59. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	66	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

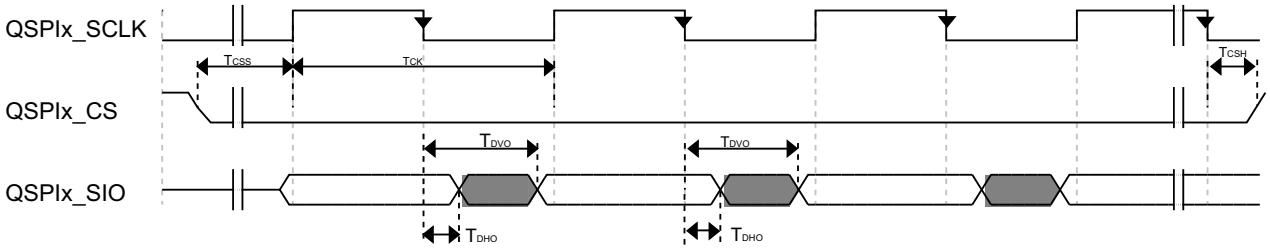

Figure 53. QuadSPI Output/Write Timing (SDR mode)

Table 64. QuadSPI Output/Write Timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	-0.5	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6ULL Reference Manual (IMX6ULLRM)* for more details.

Table 68. Master Mode SAI Timing (continued)

Num	Characteristic	Min	Max	Unit
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

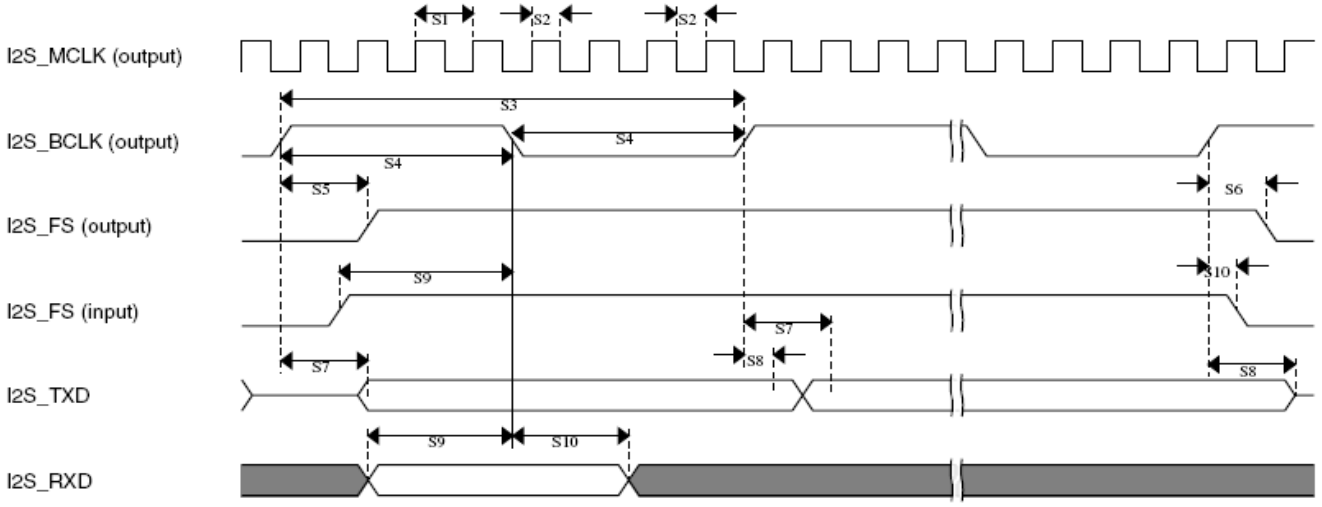

Figure 57. SAI Timing — Master Modes

Table 69. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

Table 70. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.12.13 SPDIF Timing Parameters

The Sony/Philips Digital Interface Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 71, Figure 63, and Figure 64 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 71. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

4.12.14.1.2 UART Receiver

Figure 66 depicts the RS-232 serial mode receives timing with 8 data bit/1 stop bit format. Table 73 lists serial mode receive timing characteristics.

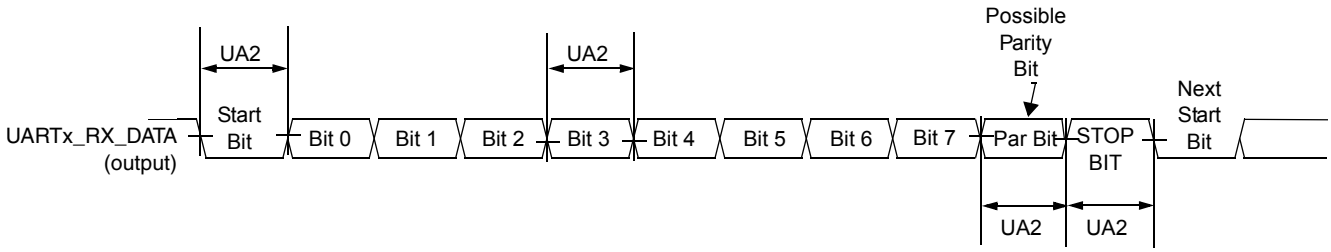

Figure 66. UART RS-232 Serial Mode Receive Timing Diagram

Table 73. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.14.1.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 67 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 74 lists the transmit timing characteristics.

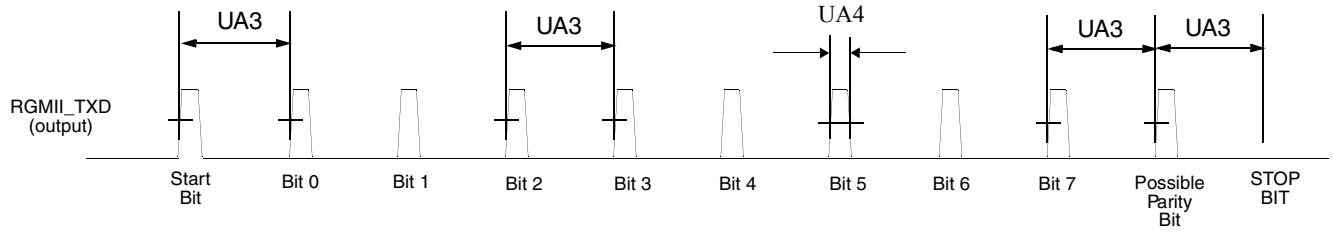

Figure 67. UART IrDA Mode Transmit Timing Diagram

Table 74. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

Table 77. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv	—	28	—	cycles	—
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv	—	0.7	—	µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
[P:][C:] Total Unadjusted Error	12 bit mode	TUE	—	4.5	—	LSB 1 LSB = (V_{REFH} - V_{REFL})/2 N	—
	10 bit mode		—	2	—		
	8 bit mode		—	1.5	—		
[P:][C:] Differential Non-Linearity	12 bit mode	DNL	—	1	—	LSB	—
	10bit mode		—	0.5	—		
	8 bit mode		—	0.2	—		

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 78 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6ULL Fuse Map document and the System Boot chapter in *i.MX 6ULL Reference Manual (IMX6ULLRM)*.

Table 78. Fuses and Associated Pins Used for Boot

Pin	Direction at reset	eFuse name	Details
BOOT_MODE0	Input with 100 K pull-down	N/A	Boot mode selection
BOOT_MODE1	Input with 100 K pull-down	N/A	Boot mode selection

Table 92. 14 x 14 mm, 0.8 mm Pitch, Ball Map (continued)

P	N	M	L	K	J	H
DRAM_SDCLK0_P	DRAM_ODT0	DRAM_SDBA0	DRAM_ADDR05	DRAM_ADDR02	DRAM_SDWE_B	DRAM_SDBA1
DRAM_SDCLK0_N	DRAM_CS0_B	DRAM_ADDR03	DRAM_ADDR09	DRAM_SDBA2	DRAM_CAS_B	DRAM_ADDR01
DRAM_DATA13	VSS	DRAM_SDCKE0	VSS	DRAM_ADDR11	DRAM_SDCKE1	DRAM_ADDR13
DRAM_VREF	DRAM_ZQPAD	DRAM_ADDR10	DRAM_ADDR12	DRAM_ADDR04	DRAM_ADDR08	DRAM_ADDR07
DRAM_DATA12	VSS	DRAM_RAS_B	DRAM_ADDR00	DRAM_ADDR15	VSS	DRAM_CS1_B
DRAM_SDQS0_P	NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
DRAM_SDQS0_N	TEST_MODE	VSS	VSS	VSS	VSS	VSS
POR_B	SNVS_TAMPER5	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER4	SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN
SNVS_TAMPER3	SNVS_TAMPER7	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN
SNVS_TAMPER2	SNVS_TAMPER6	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP
VDD_SNVS_IN	VDD_SNVS_CAP	NGND_KEL0	VSS	VSS	VSS	VSS
NVCC_PLL	VDD_HIGH_IN	ADC_VREFH	VDDA_ADC_3P3	GPIO1_IO00	NVCC_GPIO	NVCC_UART
JTAG_TMS	JTAG_TRST_B	JTAG_TCK	GPIO1_IO02	UART1_TX_DATA	UART1_RTS_B	UART2_RTS_B
JTAG_MOD	JTAG_TDO	GPIO1_IO09	GPIO1_IO01	UART1_CTS_B	UART2_CTS_B	UART3_CTS_B
CCM_CLK1_N	JTAG_TDI	GPIO1_IO04	GPIO1_IO07	UART1_RX_DATA	UART2_RX_DATA	UART3_RX_DATA
CCM_CLK1_P	GPIO1_IO08	GPIO1_IO05	GPIO1_IO03	GPIO1_IO06	UART2_TX_DATA	UART3_TX_DATA
P	N	M	L	K	J	H

Table 94. 9 x 9 mm Functional Contact Assignments (continued)

LCD_ENABLE	A10	NVCC_LCD	GPIO	ALT5	GPIO3_IO1	Input	Keeper
LCD_HSYNC	B10	NVCC_LCD	GPIO	ALT5	GPIO3_IO2	Input	Keeper
LCD_RESET	E10	NVCC_LCD	GPIO	ALT5	GPIO3_IO4	Input	Keeper
LCD_VSYNC	C10	NVCC_LCD	GPIO	ALT5	GPIO3_IO3	Input	Keeper
NAND_ALE	D8	NVCC_NAND	GPIO	ALT5	GPIO4_IO10	Input	Keeper
NAND_CE0_B	E8	NVCC_NAND	GPIO	ALT5	GPIO4_IO13	Input	Keeper
NAND_CE1_B	B6	NVCC_NAND	GPIO	ALT5	GPIO4_IO14	Input	Keeper
NAND_CLE	B7	NVCC_NAND	GPIO	ALT5	GPIO4_IO15	Input	Keeper
NAND_DATA00	D7	NVCC_NAND	GPIO	ALT5	GPIO4_IO2	Input	Keeper
NAND_DATA01	A9	NVCC_NAND	GPIO	ALT5	GPIO4_IO3	Input	Keeper
NAND_DATA02	C9	NVCC_NAND	GPIO	ALT5	GPIO4_IO4	Input	Keeper
NAND_DATA03	C7	NVCC_NAND	GPIO	ALT5	GPIO4_IO5	Input	Keeper
NAND_DATA04	C8	NVCC_NAND	GPIO	ALT5	GPIO4_IO6	Input	Keeper
NAND_DATA05	A6	NVCC_NAND	GPIO	ALT5	GPIO4_IO7	Input	Keeper
NAND_DATA06	B9	NVCC_NAND	GPIO	ALT5	GPIO4_IO8	Input	Keeper
NAND_DATA07	B8	NVCC_NAND	GPIO	ALT5	GPIO4_IO9	Input	Keeper
NAND_DQS	E6	NVCC_NAND	GPIO	ALT5	GPIO4_IO16	Input	Keeper
NAND_RE_B	D9	NVCC_NAND	GPIO	ALT5	GPIO4_IO0	Input	Keeper
NAND_READY_B	E9	NVCC_NAND	GPIO	ALT5	GPIO4_IO12	Input	Keeper
NAND_WE_B	A8	NVCC_NAND	GPIO	ALT5	GPIO4_IO1	Input	Keeper
NAND_WP_B	D6	NVCC_NAND	GPIO	ALT5	GPIO4_IO11	Input	Keeper
ONOFF	R6	VDD_SNVS_IN	SRC	ALT0	SRC_RESET_B	Input	100 kΩ pull-up
POR_B	R10	VDD_SNVS_IN	SRC	ALT0	SRC_POR_B	Input	100 kΩ pull-up
RTC_XTALI	T12	VDD_SNVS_CAP	ANALOG	—	RTC_XTALI	—	—
RTC_XTALO	U12	VDD_SNVS_CAP	ANALOG	—	RTC_XTALO	—	—
SD1_CLK	C5	NVCC_SD	GPIO	ALT5	GPIO2_IO17	Input	Keeper
SD1_CMD	C6	NVCC_SD	GPIO	ALT5	GPIO2_IO16	Input	Keeper
SD1_DATA0	A5	NVCC_SD	GPIO	ALT5	GPIO2_IO18	Input	Keeper
SD1_DATA1	A4	NVCC_SD	GPIO	ALT5	GPIO2_IO19	Input	Keeper
SD1_DATA2	B5	NVCC_SD	GPIO	ALT5	GPIO2_IO20	Input	Keeper
SD1_DATA3	B4	NVCC_SD	GPIO	ALT5	GPIO2_IO21	Input	Keeper