

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

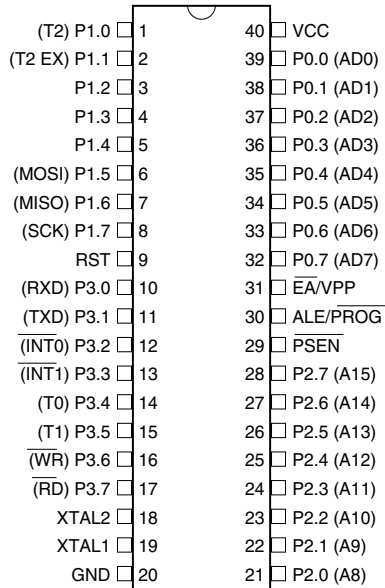
Applications of "[Embedded - Microcontrollers](#)"

Details

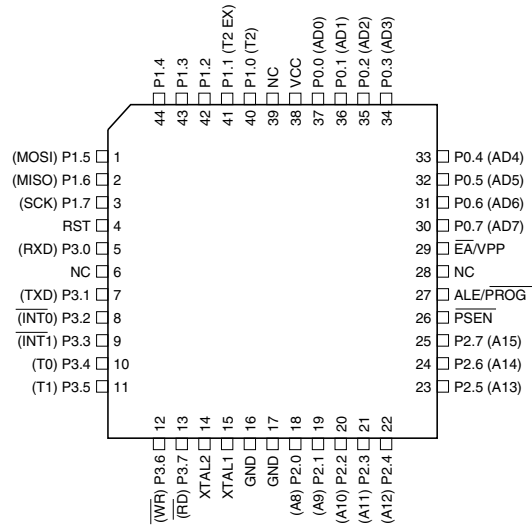
| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | UART/USART |
| Peripherals | WDT |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 4V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at89ls52-16au |

2. Pin Configurations

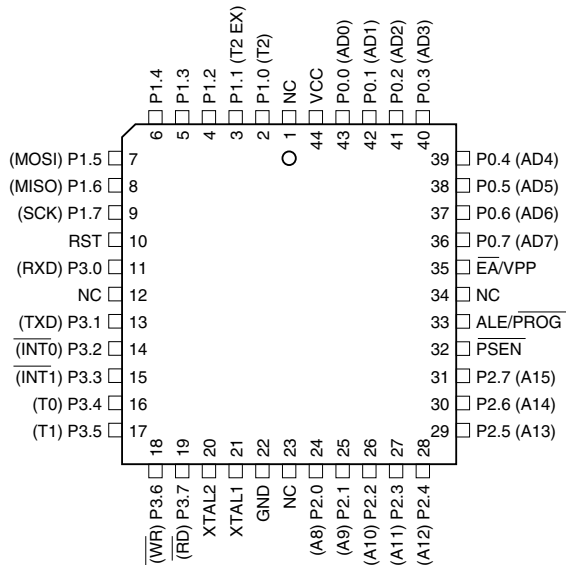
2.1 40-lead PDIP



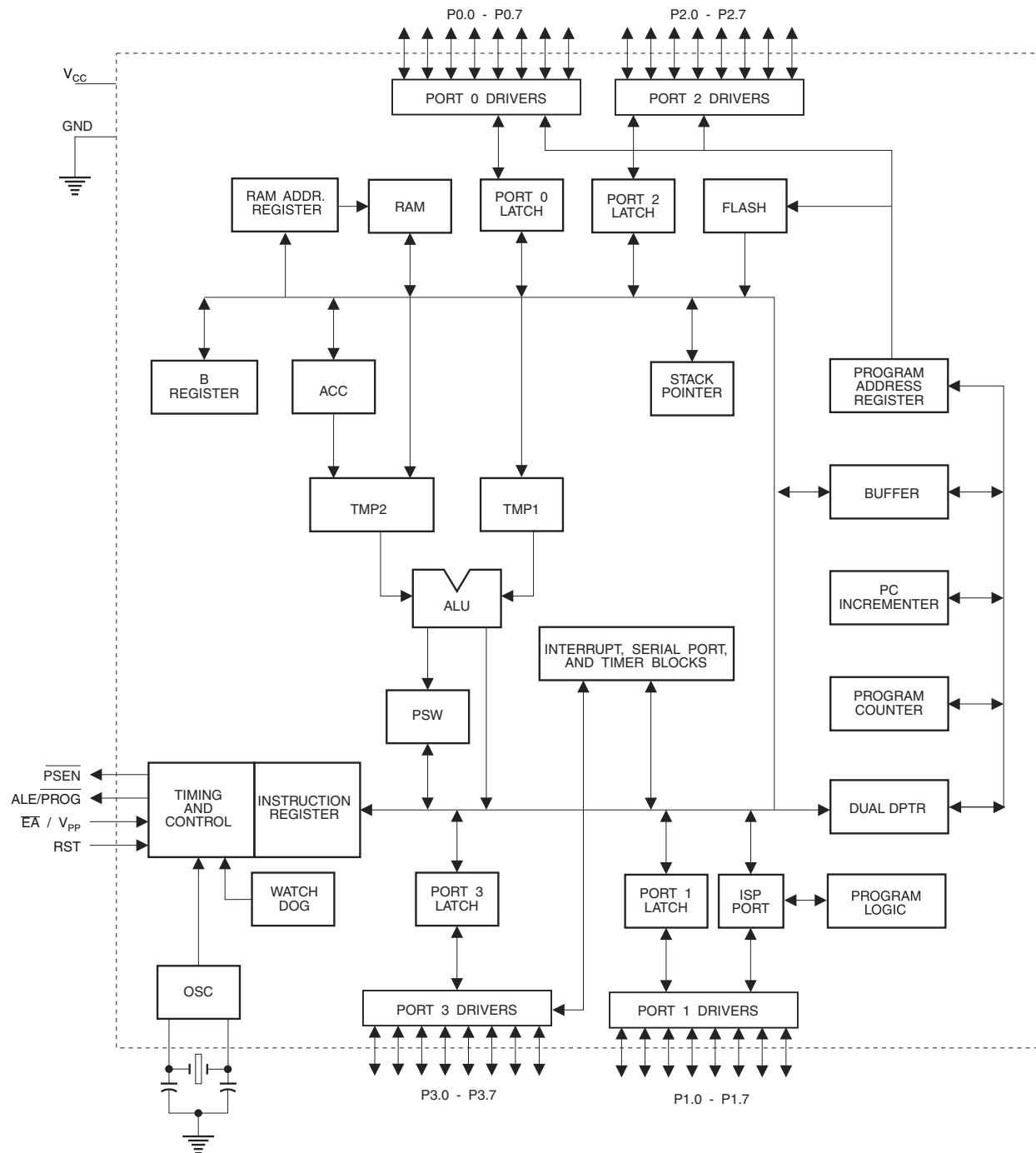
2.3 44-lead TQFP



2.2 44-lead PLCC



3. Block Diagram



4. Pin Description

4.1 VCC

Supply voltage.

4.2 GND

Ground.

4.3 Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

4.4 Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

| Port Pin | Alternate Functions |
|----------|---|
| P1.0 | T2 (external count input to Timer/Counter 2), clock-out |
| P1.1 | T2EX (Timer/Counter 2 capture/reload trigger and direction control) |
| P1.5 | MOSI (used for In-System Programming) |
| P1.6 | MISO (used for In-System Programming) |
| P1.7 | SCK (used for In-System Programming) |

4.5 Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

4.6 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89LS52, as shown in the following table.

| Port Pin | Alternate Functions |
|----------|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{INT0}$ (external interrupt 0) |
| P3.3 | $\overline{INT1}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 1 external input) |
| P3.6 | \overline{WR} (external data memory write strobe) |
| P3.7 | \overline{RD} (external data memory read strobe) |

4.7 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

4.8 ALE/ \overline{PROG}

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (\overline{PROG}) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.9 \overline{PSEN}

Program Store Enable (\overline{PSEN}) is the read strobe to external program memory.

When the AT89LS52 is executing code from external program memory, \overline{PSEN} is activated twice each machine cycle, except that two \overline{PSEN} activations are skipped during each access to external data memory.

4.10 \overline{EA}/VPP

External Access Enable. \overline{EA} must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, \overline{EA} will be internally latched on reset.

\overline{EA} should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

4.11 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.12 XTAL2

Output from the inverting oscillator amplifier.

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 5-2) and T2MOD (shown in Table 10-2) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 5-1. AT89LS52 SFR Map and Reset Values

| | | | | | | | | |
|------|-------------------|-------------------|--------------------|--------------------|------------------|------------------|--------------------|-------------------------|
| 0F8H | | | | | | | | 0FFH |
| 0F0H | B 00000000 | | | | | | | 0F7H |
| 0E8H | | | | | | | | 0EFH |
| 0E0H | ACC 00000000 | | | | | | | 0E7H |
| 0D8H | | | | | | | | 0DFH |
| 0D0H | PSW 00000000 | | | | | | | 0D7H |
| 0C8H | T2CON 00000000 | T2MOD XXXXXX00 | RCAP2L 00000000 | RCAP2H 00000000 | TL2 00000000 | TH2 00000000 | | 0CFH |
| 0C0H | | | | | | | | 0C7H |
| 0B8H | IP XX000000 | | | | | | | 0BFH |
| 0B0H | P3 11111111 | | | | | | | 0B7H |
| 0A8H | IE 0X000000 | | | | | | | 0AFH |
| 0A0H | P2 11111111 | | AUXR1 XXXXXXX0 | | | | WDTRST XXXXXXXX | 0A7H |
| 98H | SCON 00000000 | SBUF XXXXXXXX | | | | | | 9FH |
| 90H | P1 11111111 | | | | | | | 97H |
| 88H | TCON 00000000 | TMOD 00000000 | TL0 00000000 | TL1 00000000 | TH0 00000000 | TH1 00000000 | AUXR XXX00XX0 | 8FH |
| 80H | P0 11111111 | SP 00000111 | DP0L 00000000 | DP0H 00000000 | DP1L 00000000 | DP1H 00000000 | | PCON 0XXX0000 87H |

Table 5-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H

Reset Value = 0000 0000B

Bit Addressable

| | | | | | | | | |
|-----|-----|------|------|------|-------|-----|--------------------|----------------------|
| Bit | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/ $\overline{T2}$ | CP/ $\overline{RL2}$ |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|----------------------|--|
| TF2 | Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1. |
| EXF2 | Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1). |
| RCLK | Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock. |
| TCLK | Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock. |
| EXEN2 | Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX. |
| TR2 | Start/Stop control for Timer 2. TR2 = 1 starts the timer. |
| C/ $\overline{T2}$ | Timer or counter select for Timer 2. C/ $\overline{T2}$ = 0 for timer function. C/ $\overline{T2}$ = 1 for external event counter (falling edge triggered). |
| CP/ $\overline{RL2}$ | Capture/Reload select. CP/ $\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/ $\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow. |

Table 5-3. AUXR: Auxiliary Register

AUXR

Address = 8EH

Reset Value = XXX00XX0B

Not Bit Addressable

| | | | | | | | | |
|-----|---|---|---|--------|--------|---|---|--------|
| | — | — | — | WDIDLE | DISRTO | — | — | DISALE |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

—

Reserved for future expansion

DISALE

Disable/Enable ALE

DISALE

Operating Mode

0

ALE is emitted at a constant rate of 1/6 the oscillator frequency

1

ALE is active only during a MOVX or MOVC instruction

DISRTO

Disable/Enable Reset out

DISRTO

0

Reset pin is driven High after WDT times out

1

Reset pin is input only

WDIDLE

Disable/Enable WDT in IDLE mode

WDIDLE

0

WDT continues to count in IDLE mode

1

WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **always** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to “1” during power up. It can be set and rest under software control and is not affected by reset.

Table 5-4. AUXR1: Auxiliary Register 1

| | | | | | | | | |
|-------|-------------------------------|-----------------------------------|---|---|---|---|---|-----|
| AUXR1 | Address = A2H | Reset Value = XXXXXXX0B | | | | | | |
| | Not Bit Addressable | | | | | | | |
| | | — | — | — | — | — | — | DPS |
| | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| — | Reserved for future expansion | | | | | | | |
| DPS | Data Pointer Register Select | | | | | | | |
| | DPS | | | | | | | |
| | 0 | Selects DPTR Registers DP0L, DP0H | | | | | | |
| | 1 | Selects DPTR Registers DP1L, DP1H | | | | | | |

6. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

6.1 Program Memory

If the \overline{EA} pin is connected to GND, all program fetches are directed to external memory.

On the AT89LS52, if \overline{EA} is connected to V_{CC} , program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are directed to external memory.

6.2 Data Memory

The AT89LS52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access of the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

7. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

7.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $98 \times TOSC$, where $TOSC = 1/FOSC$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

7.2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89LS52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89LS52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

Figure 10-2. Timer 2 Auto Reload Mode (DCEN = 0)

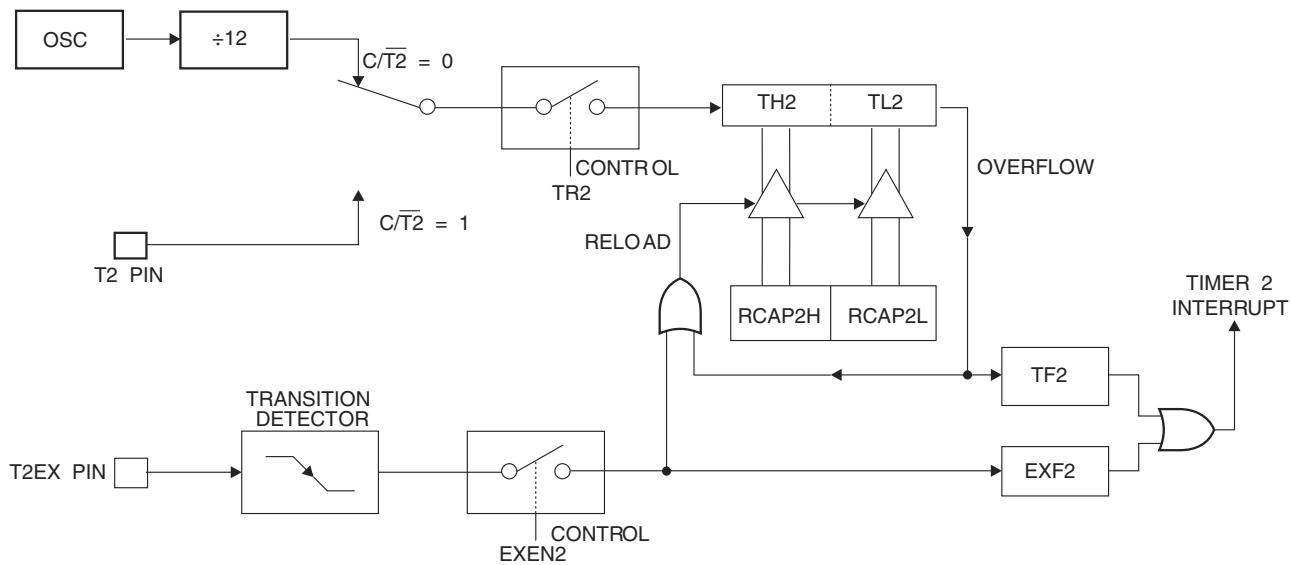


Table 10-2. T2MOD – Timer 2 Mode Control Register

| | | | | | | | | |
|----------------------|---|---|---|---|---|--------------------------|------|------|
| T2MOD Address = 0C9H | | | | | | Reset Value = XXXX XX00B | | |
| Not Bit Addressable | | | | | | | | |
| Bit | – | – | – | – | – | – | T2OE | DCEN |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|--------|--|
| – | Not implemented, reserved for future |
| T2OE | Timer 2 Output Enable bit |
| DCEN | When set, this bit allows Timer 2 to be configured as an up/down counter |

Figure 10-3. Timer 2 Auto Reload Mode (DCEN = 1)

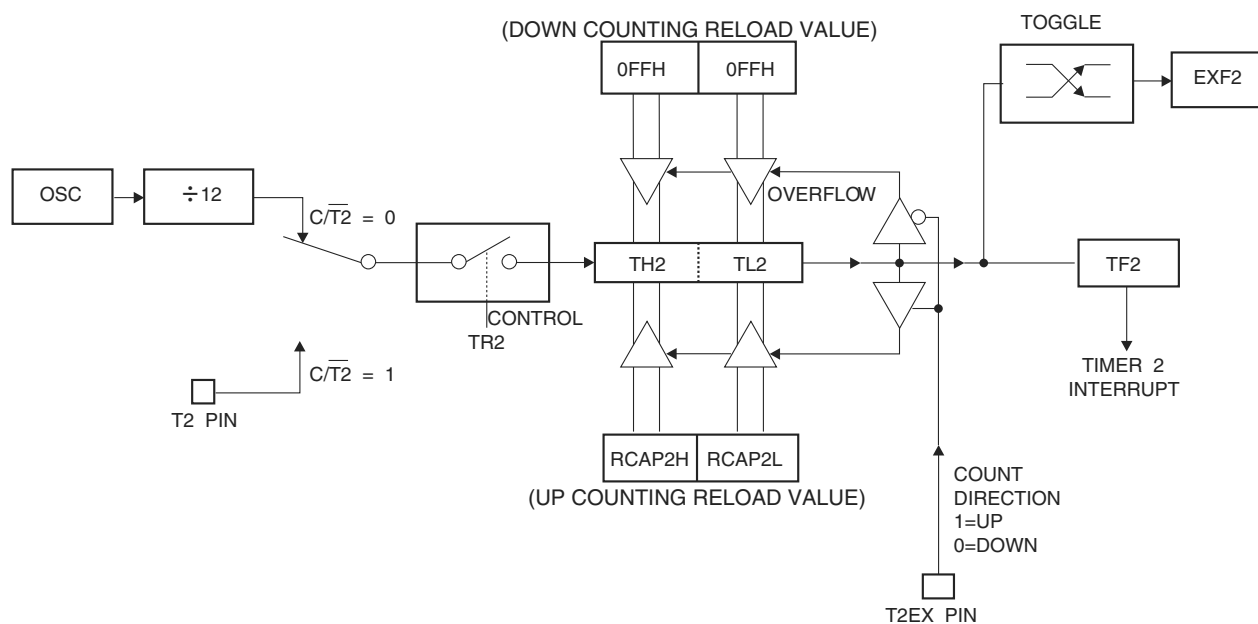
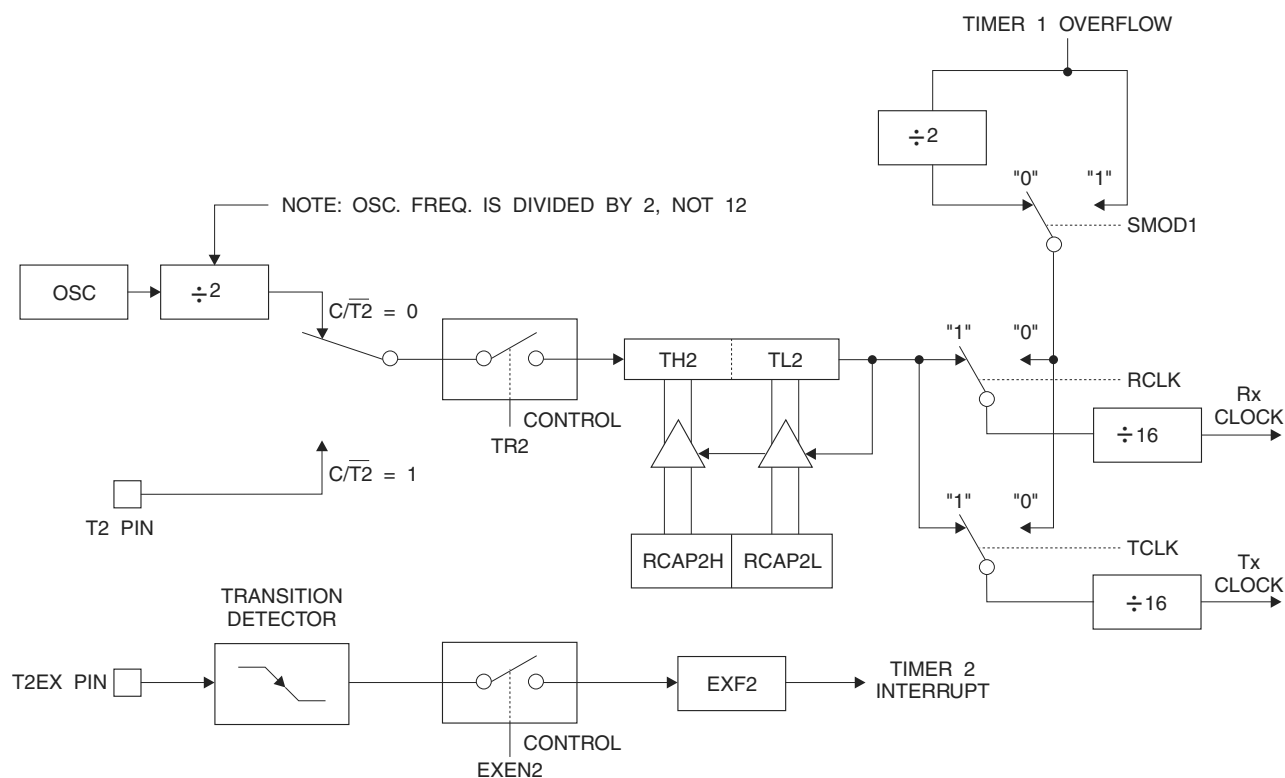


Figure 10-4. Timer 2 in Baud Rate Generator Mode



11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 5-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 10-4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - \text{RCAP2H}, \text{RCAP2L}]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

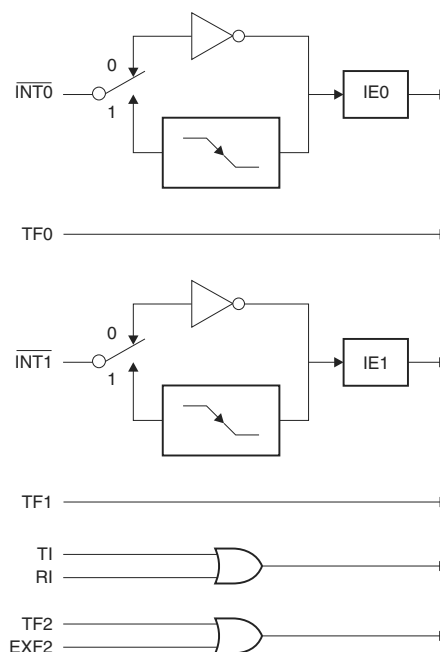
Timer 2 as a baud rate generator is shown in Figure 10-4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.



The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 13-1. Interrupt Sources

14. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 16-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

15. Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.






Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

20. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 20-1. Flash Programming Modes

| Mode | V _{CC} | RST | $\overline{\text{PSEN}}$ | ALE/ $\overline{\text{PROG}}$ | $\overline{\text{EA}}/$ V _{PP} | P2.6 | P2.7 | P3.3 | P3.6 | P3.7 | P0.7-0 Data | P2.4-0 | P1.7-0 |
|------------------------|-----------------|-----|--------------------------|---|--|------|------|------|------|------|------------------------|---------|--------|
| | | | | | | | | | | | | Address | |
| Write Code Data | 5V | H | L |  ⁽²⁾ | 12V | L | H | H | H | H | D _{IN} | A12-8 | A7-0 |
| Read Code Data | 5V | H | L | H | H | L | L | L | H | H | D _{OUT} | A12-8 | A7-0 |
| Write Lock Bit 1 | 5V | H | L |  ⁽³⁾ | 12V | H | H | H | H | H | X | X | X |
| Write Lock Bit 2 | 5V | H | L |  ⁽³⁾ | 12V | H | H | H | L | L | X | X | X |
| Write Lock Bit 3 | 5V | H | L |  ⁽³⁾ | 12V | H | L | H | H | L | X | X | X |
| Read Lock Bits 1, 2, 3 | 5V | H | L | H | H | H | H | L | H | L | P0.2, P0.3, P0.4 | X | X |
| Chip Erase | 5V | H | L |  ⁽¹⁾ | 12V | H | L | H | L | L | X | X | X |
| Read Atmel ID | 5V | H | L | H | H | L | L | L | L | L | 1EH | X 0000 | 00H |
| Read Device ID | 5V | H | L | H | H | L | L | L | L | L | 62H | X 0001 | 00H |
| Read Device ID | 5V | H | L | H | H | L | L | L | L | L | 06H | X 0010 | 00H |

- Notes:
1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
 2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
 3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
 4. RDY/BSY signal is output on P3.0 during programming.
 5. X = don't care.

Figure 20-1. Programming the Flash Memory (Parallel Mode)

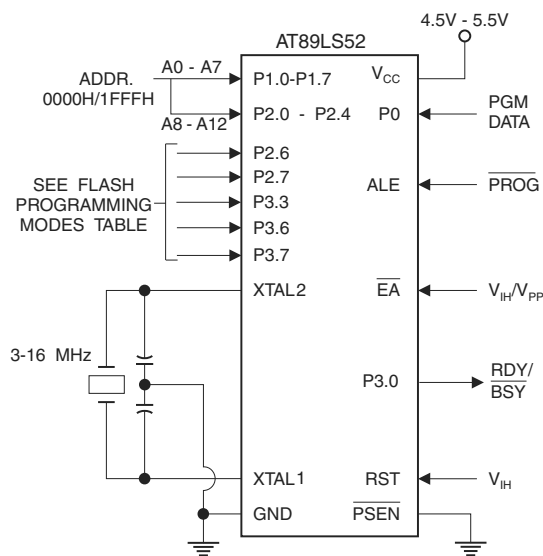
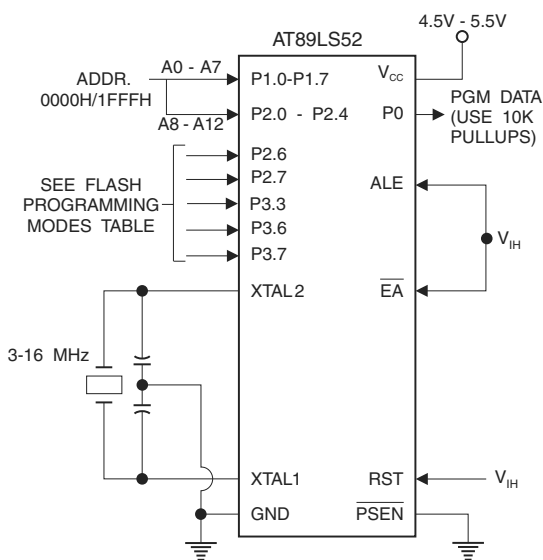
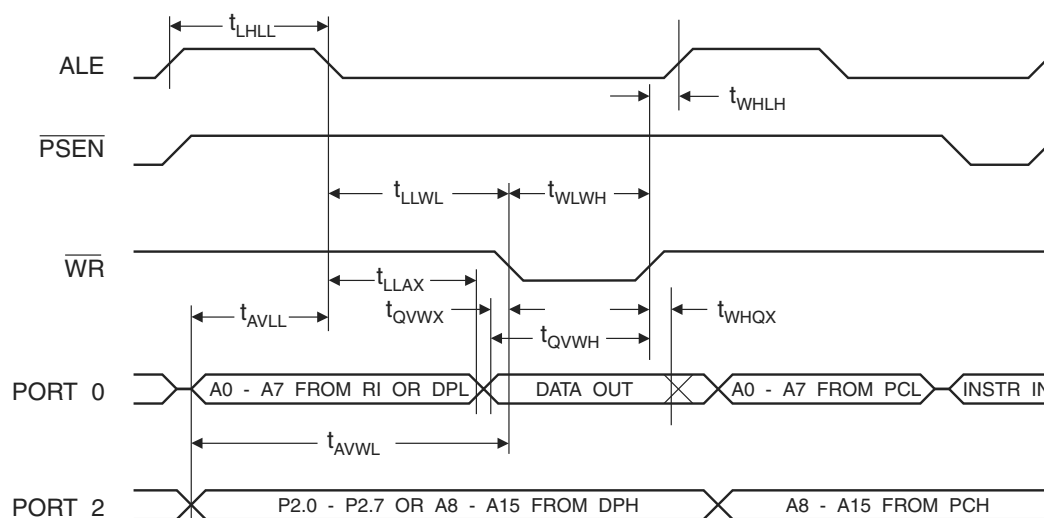


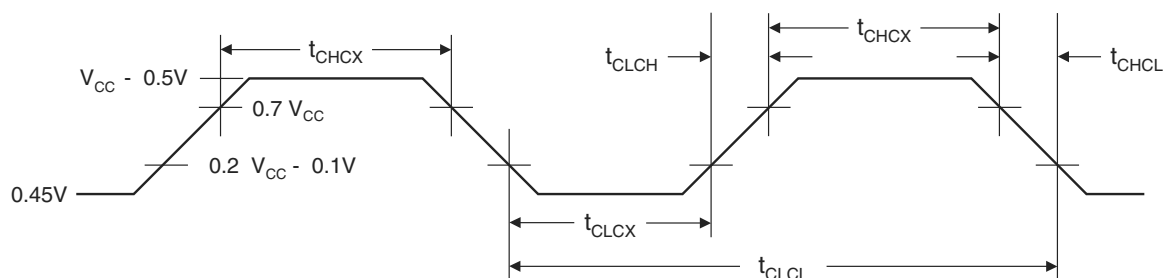
Figure 20-2. Verifying the Flash Memory (Parallel Mode)



29. External Data Memory Write Cycle



30. External Clock Drive Waveforms



31. External Clock Drive

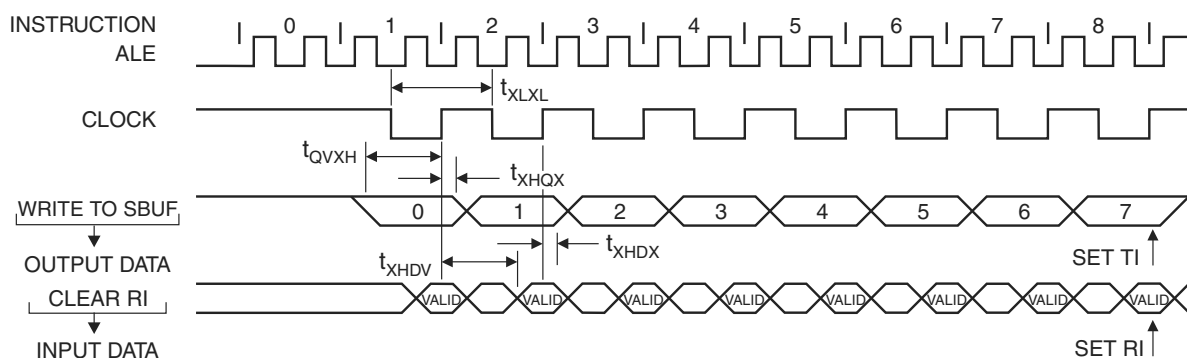
| Symbol | Parameter | Min | Max | Units |
|--------------|----------------------|------|-----|-------|
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 16 | MHz |
| t_{CLCL} | Clock Period | 62.5 | | ns |
| t_{CHCX} | High Time | 20 | | ns |
| t_{CLCX} | Low Time | 20 | | ns |
| t_{CLCH} | Rise Time | | 20 | ns |
| t_{CHCL} | Fall Time | | 20 | ns |

32. Serial Port Timing: Shift Register Mode Test Conditions

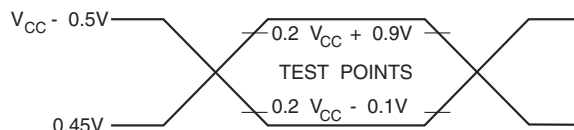
The values in this table are valid for $V_{CC} = 2.7V$ to $4.0V$ and Load Capacitance = 80 pF .

| Symbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|------------|--|------------|-----|---------------------|---------------------|---------|
| | | Min | Max | Min | Max | |
| t_{XLXL} | Serial Port Clock Cycle Time | 1.0 | | $12 t_{CLCL}$ | | μs |
| t_{QVXH} | Output Data Setup to Clock Rising Edge | 700 | | $10 t_{CLCL} - 133$ | | ns |
| t_{XHGX} | Output Data Hold After Clock Rising Edge | 50 | | $2 t_{CLCL} - 80$ | | ns |
| t_{XHDX} | Input Data Hold After Clock Rising Edge | 0 | | 0 | | ns |
| t_{XHDV} | Clock Rising Edge to Input Data Valid | | 700 | | $10 t_{CLCL} - 133$ | ns |

33. Shift Register Mode Timing Waveforms

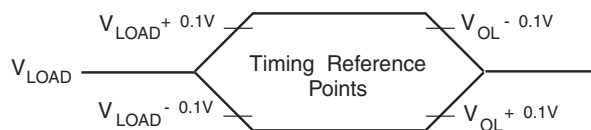


34. AC Testing Input/Output Waveforms⁽¹⁾



Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

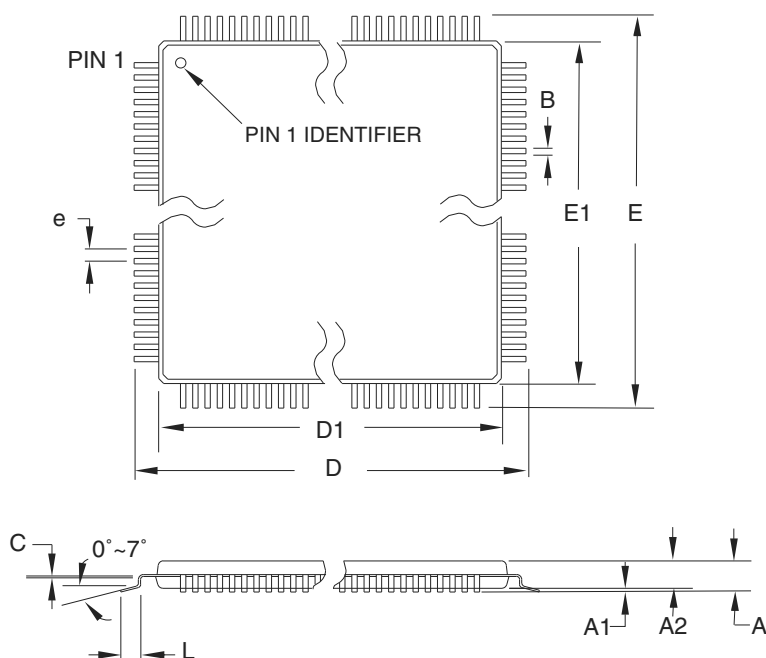
35. Float Waveforms⁽¹⁾



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

37. Packaging Information

37.1 44A



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-------|-------|--------|
| A | — | — | 1.20 | |
| A1 | 0.05 | — | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | — | 0.45 | |
| C | 0.09 | — | 0.20 | |
| L | 0.45 | — | 0.75 | |
| e | 0.80 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

| | | | |
|--|--|---------------------------|------------------|
| 2325 Orchard Parkway San Jose, CA 95131 | TITLE 44A , 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | DRAWING NO. 44A | REV. B |
|--|--|---------------------------|------------------|