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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	3.6MHz
Connectivity	-
Peripherals	LED, Power-Fail Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	2KB (1K x 16)
Program Memory Type	EEPROM
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	24-DIP (0.300", 7.62mm)
Supplier Device Package	24-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq3210-emx

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Digital I/O Pin
 Relative to Ground -0.5V to ($V_{DDINT} + 0.5V$)
 Voltage Range on Any Analog I/O Pin
 Relative to Ground -0.5V to ($V_{DDINT} + 0.5V$)
 Voltage Range on V_{DD} Relative to Ground -0.5V to +10.5V
 Voltage Range on FEED Relative to Ground -0.5V to +20V

Continuous Output Current (any single I/O pin) 25mA
 Continuous Output Current (all I/O pins combined) 25mA
 Operating Temperature Range -40°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Soldering Temperature See IPC/JEDEC
 J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = V_{DD(MIN)}$ to $V_{DD(MAX)}$, $C_{REGOUT} = 10\mu F + 0.1\mu F$, $C_{VDD} = 1\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		6.0	9.0	9.5	V
Internal Regulated Supply Voltage	V_{DDINT}		4.5	5.0	5.5	V
Voltage Regulator Output	V_{REGOUT}	Maximum $I_{SOURCE} = 50mA$	4.5	5.0	5.5	V
Low-Battery Detection Threshold	V_{BF}	0°C to +85°C	7.0		7.51	V
		-40°C	6.9		7.6	
Power-Fail Reset	V_{RST}		4.15		4.6	V
Active Current	I_{DD1}	/1 mode (Note 2) sysclk = f_{HFXIN}		6.4	9.0	mA
	I_{DD2}	/2 mode (Note 2) sysclk = $f_{HFXIN} / 2$		4.0	6.0	mA
	I_{DD3}	/4 mode (Note 2) sysclk = $f_{HFXIN} / 4$		2.9	4.5	mA
	I_{DD4}	/8 mode (Note 2) sysclk = $f_{HFXIN} / 8$		2.3	3.5	mA
	I_{DD5}	PMM1 mode (Note 2) sysclk = $f_{HFXIN} / 256$		1.7	3.0	mA
	I_{DD6}	8kHz ring mode (Note 2)		0.6	1.2	mA
Stop-Mode Current	I_{STOP1}	Brownout detector off, wake-up timer on, $T_A = +50^\circ C$ (Note 3), $V_{DD} = 9V$		7.5	33.0	μA
	I_{STOP2}	Brownout detector off, wake-up timer on, $T_A = +25^\circ C$, $V_{DD} = 9V$		5.5	13	
	I_{STOP3}	Brownout detector on, wake-up timer on, $T_A = +25^\circ C$, $V_{DD} = 9V$		51	80	
RESET Pullup	R_{RST}	$V_{RST} = 0.4V$, $V_{REGOUT} = 5.5V$	102	150	250	k Ω

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = V_{DD(MIN)}$ to $V_{DD(MAX)}$, $C_{REGOUT} = 10\mu F + 0.1\mu F$, $C_{VDD} = 1\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O AND OSCILLATOR						
Input High Voltage: Px.x and HFXIN	V_{IH}	XTRC = 0/1	0.85 x V_{DDINT}			V
Input Low Voltage: Px.x and HFXIN	V_{IL}	XTRC = 0/1			0.15 x V_{DDINT}	V
Output High Voltage: Px.x	V_{OH}	$I_{SOURCE} = 4mA$	0.85 x V_{DDINT}			V
Output Low Voltage: Px.x (except P0.7)	V_{OL}	$I_{SINK} = 4mA$			0.4	V
Output Low Voltage: P0.7	V_{OL1}	$I_{SINK} = 10mA$			0.4	V
Input Low Current (All Ports)	I_L	Input mode with weak pullup disabled	-1		+1	μA
Input Low Current (All Ports)	I_L	Input mode with weak pullup active, $V_{IL} = 0.4V$, $V_{DDINT} = 5.5V$		-31	-50	μA
CLOCK SOURCES						
External-Clock Frequency	f_{HFIN}	External crystal	1.00		3.58	MHz
		External oscillator	0		3.58	
Internal Ring Oscillator	f_{RO}			8		kHz
JTAG PROGRAMMING						
TCK Frequency	f_{TCK}	JTAG programming (Note 3). Sysclk is a function of f_{HFXIN} and the clock divisor; see I_{DDX} parameters above	0		sysclk / 8	MHz
MEMORY CHARACTERISTICS (Note 3)						
EEPROM Write/Erase Cycles		$\theta_{JA} = +85^\circ C$	15,000			Cycles
		$\theta_{JA} = +25^\circ C$	60,000			Cycles
EEPROM Data Retention			10			Years

Note 1: Specifications to $-40^\circ C$ are guaranteed by design and are not production tested.

Note 2: Measured on the V_{DD} pin with $V_{DD} = 9.5V$, $f_{HFXIN} = 3.58MHz$, program EEPROM contains checkerboard, and not in reset.

Note 3: Specification guaranteed by design but not production tested.

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	VREF/P0.4	Voltage Reference Input/Output or General-Purpose, Digital I/O, Type D Port. This pin functions as either the output of the internal voltage reference or as a bidirectional I/O. This pin can also be driven with an external voltage to provide an optional voltage reference. The pin defaults to a digital input with a weak pullup after a reset.
3	CMP0/P0.3	Analog Voltage Comparator Output or General-Purpose, Digital I/O, Type D Port. This pin functions as either the output of the analog voltage comparator or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
4	T2P/P0.2	Timer 2 Input/Output or General-Purpose, Digital I/O, Type D Port. This pin functions as either the input or output of Timer 2 or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
5	T2PB/P0.1	Secondary Timer 2 Input/Output or General-Purpose, Digital I/O, Type D Port. This pin functions as either the secondary output of Timer 2 or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
6	P0.0	General-Purpose, Digital I/O, Type D Port. This pin functions as a bidirectional I/O, and defaults to a digital input with a weak pullup after a reset.
7	P1.6	General-Purpose, Digital I/O, Type D Port. This pin functions as a bidirectional I/O, and defaults to a digital input with a weak pullup after a reset.
8	P1.5	General-Purpose, Digital I/O, Type D Port. This pin functions as a bidirectional I/O, and defaults to a digital input with a weak pullup after a reset.
9	TDO/P1.4	Debug Port Signal TDO or General-Purpose, Digital I/O, Type D Port. This pin functions as either the TDO signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
10	TCK/P1.3	Debug Port Signal TCK or General-Purpose, Digital I/O, Type D Port. This pin functions as either the TCK signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
11	HFXIN	Oscillator Input. Connect an external crystal or resonator between HFXIN and HFXOUT for system clock generation. When using a crystal, a load capacitor of approximately 22pF must be connected between this pin and ground. Alternatively, HFXIN is the input for an external clock source when HFXOUT is floating.
12	HFXOUT	Oscillator Output. Connect an external crystal or resonator between HFXIN and HFXOUT as the system clock. When using a crystal, a load capacitor of approximately 22pF must be connected between this pin and ground. Alternatively, float HFXOUT when an external high-frequency clock source is connected to the HFXIN pin.

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Pin Description (continued)

MAXQ3210

PIN	NAME	FUNCTION
13	FEED	Piezoelectric Horn Driver, Feedback. This input is connected to the feedback electrode of the horn. If FEED is not used, it should be grounded.
14	HORNB	Piezoelectric Horn Driver, Horn Brass. This output pin is connected to the piezo metal support electrode of the horn.
15	GND _{HORN}	Piezoelectric Horn Driver, Ground. This pin should be connected to GND, the same ground as pin 1. There is no special isolation required for this pin.
16	HORNS	Piezoelectric Horn Driver, Horn Silver. This output pin is connected to the ceramic electrode and provides the complementary output to HORNB when the horn output is enabled.
17	V _{DD}	Digital Power. This pin should be connected to a bypass capacitor to ground.
18	REGOUT	Voltage Regulator Output. This pin provides the regulated output of the internal voltage regulator. This pin requires sufficient bypass capacitance, preferably a parallel combination of 10μF and 0.1μF capacitors between this pin and ground.
19	TMS/P1.2	Debug Port Signal TMS or General-Purpose, Digital I/O, Type D Port. This pin functions as either the TMS signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
20	RESET/P1.1	Active-Low Reset Input or General-Purpose, Digital I/O, Type D Port. This pin defaults to the reset input mode of operation following a POR. The reset input mode can be deactivated and the digital I/O mode enabled by programming the RSTD bit to 1.
21	TDI/P1.0	Debug Port Signal TDI or General-Purpose, Digital I/O, Type D Port. This pin functions as either the TDI signal of the debug port or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
22	LED/P0.7	High-Current (Sink) Driver Output or General-Purpose, Digital I/O, Type D Port. This pin functions with a high-current pulldown to drive a device such as an LED or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
23	INT/P0.6	External Edge-Selectable Interrupt or General-Purpose, Digital I/O, Type D Port. This pin functions as either an external edge-selectable interrupt or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.
24	CMPI/P0.5	Analog Voltage Comparator Input or General-Purpose, Digital I/O, Type D Port. This pin functions as either the input to the analog voltage comparator or as a bidirectional I/O. The pin defaults to a digital input with a weak pullup after a reset.

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and the upper three bits containing the register subindex within that module. Any time that it is necessary to directly select one of the upper 24 index locations in a destination module, the prefix register PFX is needed to supply the extra destination bits. This prefix register write is inserted automatically by the assembler and requires only one additional execution cycle.

Memory Organization

The device incorporates several memory areas:

- 2kWords of utility ROM
- 1kWords of EEPROM for program storage
- 128bytes of EEPROM for data storage
- 64bytes of SRAM for storage of temporary variables
- 4-level stack memory for storage of program return addresses and general-purpose use

The memory is arranged by default in a Harvard architecture, with separate address spaces for program and data memory. A special pseudo-Von Neumann memory mode allows data memory to be mapped into program space, permitting code execution from data memory. This places the utility ROM, code, and data memory into a single contiguous memory map. This is useful for applications that require dynamic program modification or unique memory configurations. In addition, another mode allows program memory to be mapped into data space, permitting code constants to be accessed as data memory.

The incorporation of EEPROM for program storage allows the devices to be reprogrammed, eliminating the expense of throwing away one-time programmable devices during development and field upgrades. EEPROM can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

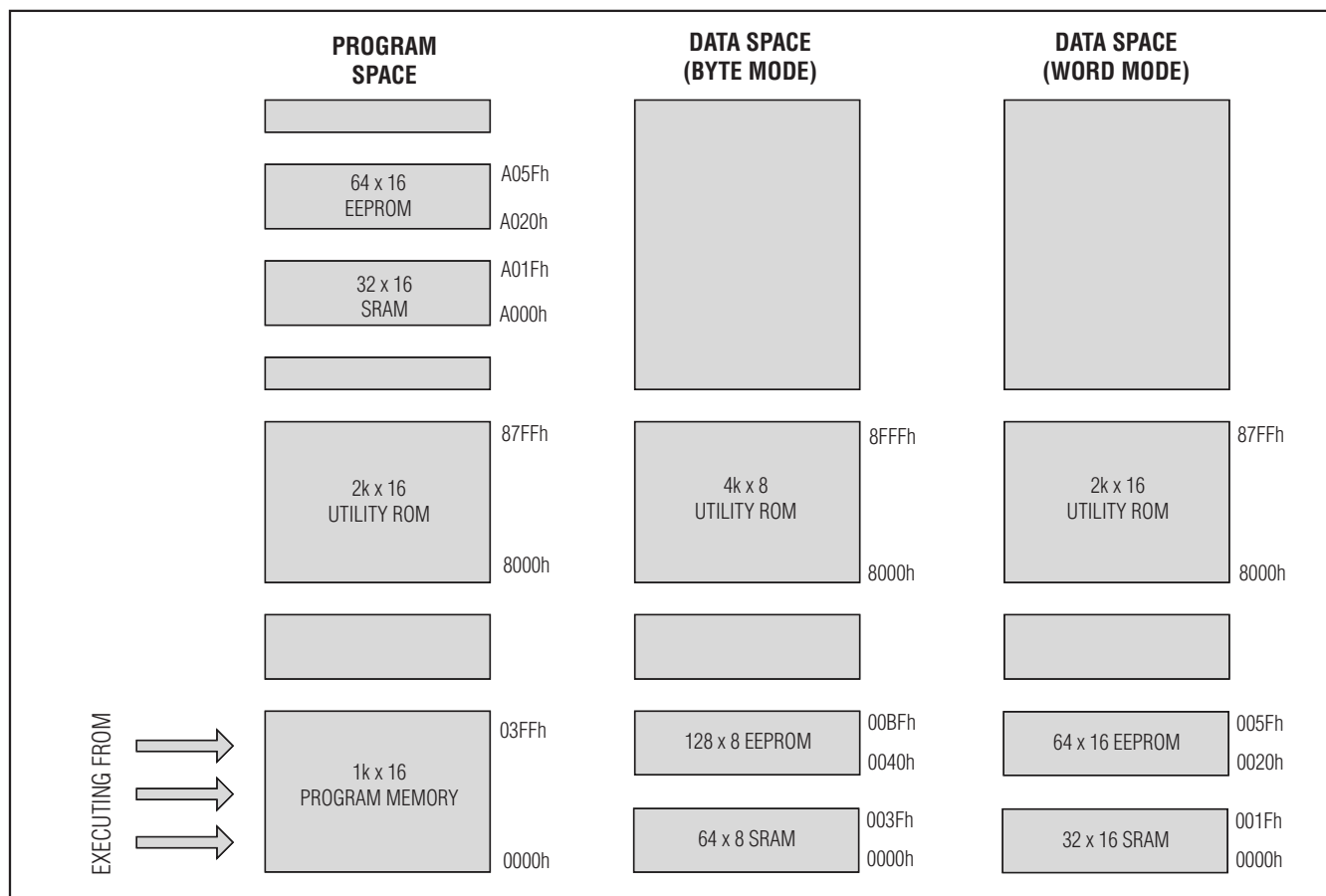


Figure 1. Memory Map

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In-Application Programming:

The in-application programming feature allows the microcontroller to modify its own program memory from its application software. This allows on-the-fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains user-accessible programming functions that erase and program memory. These functions are described in detail in the user's guide for this device.

Register Set

Most functions of the device are controlled by sets of registers. These registers provide a working space for

memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers and peripheral registers. The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality that may be included by different products based on the MAXQ architecture. This functionality is broken up into discrete modules so that only the features required for a given product need to be included. The following tables show the MAXQ3210 register set. Note that the accumulators are 8 bits wide for this device.

Table 1. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	A (9h)	PFX (Bh)	IP (Ch)	SP (Dh)	DPC (Eh)	DP (Fh)
0xh	AP	A[0]	PFX[0]	IP	—	—	—
1xh	APC	A[1]	PFX[1]	—	SP	—	—
2xh	—	A[2]	PFX[2]	—	IV	—	—
3xh	—	A[3]	PFX[3]	—	—	Offs	DP0
4xh	PSF	A[4]	PFX[4]	—	—	DPC	—
5xh	IC	A[5]	PFX[5]	—	—	GR	—
6xh	IMR	A[6]	PFX[6]	—	LC0	GRL	—
7xh	—	A[7]	PFX[7]	—	LC1	BP	DP1
8xh	SC	A[8]	—	—	—	GRS	—
9xh	—	A[9]	—	—	—	GRH	—
Axh	—	A[10]	—	—	—	GRXL	—
Bxh	<i>IIR</i>	A[11]	—	—	—	BP[offs]	—
Cxh	—	A[12]	—	—	—	—	—
Dxh	—	A[13]	—	—	—	—	—
Exh	CKCN	A[14]	—	—	—	—	—
Fxh	WDCN	A[15]	—	—	—	—	—

Note: Names that appear in *italics* indicate that all bits of a register are read-only. Names that appear in **bold** indicate that a register is 16 bits wide. Registers in module AP are bit addressable.

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Table 3. System Register Bit Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									0	0	0	0	0	0	0	0
APC									0	0	0	0	0	0	0	0
PSF									1	0	0	0	0	0	0	0
IC									0	0	0	0	0	0	0	0
IMR									0	0	0	0	0	0	0	0
SC									1	0	i	i	i	0	s	0
IIR									0	0	0	0	0	0	0	0
CKCN									s	s	s	0	0	0	0	0
WDCN									s	s	0	0	0	s	s	0
A[n] (0..15)									0	0	0	0	0	0	0	0
PFX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
IV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Offs									0	0	0	0	0	0	0	0
DPC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									0	0	0	0	0	0	0	0
BP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									0	0	0	0	0	0	0	0
GRXL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BP[offs]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: Bits marked with an "i" have an indeterminate value upon reset. Bits marked with an "s" have special behavior upon reset. Refer to the User's Guide Supplement for this device for more details.

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Table 4. Peripheral Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)		
	M0 (x0h)	M1 (x1h)	M2 (x2h)
0xh	PO0	CMPC	—
1xh	PO1	—	—
2xh	—	—	—
3xh	—	—	—
4xh	—	T2CNA	—
5xh	—	T2H	—
6xh	—	T2RH	—
7xh	EIE0	T2CH	—
8xh	<i>PI0</i>	T2CNB	—
9xh	<i>PI1</i>	T2V	—
Axh	—	T2R	—
Bxh	—	T2C	—
Cxh	HRNC	—	—
Dxh	PWCN	—	—
Exh	WUTC	—	—
Fxh	WUT	—	—

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)		
	M0 (x0h)	M1 (x1h)	M2 (x2h)
10xh	PD0	T2CFG	—
11xh	PD1	—	—
12xh	—	—	—
13xh	—	—	—
14xh	KEN0	—	—
15xh	KEN1	—	—
16xh	—	—	—
17xh	—	—	—
18xh	—	—	—
19xh	—	—	—
1Axh	—	—	—
1Bxh	ICDF	—	—
1Cxh	—	—	—
1Dxh	—	—	—
1Exh	—	—	—
1Fxh	—	—	—

Note: Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide.

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Table 5. Peripheral Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									PO0.7	PO0.6	PO0.5	PO0.4	PO0.3	PO0.2	PO0.1	PO0.0
PO1									—	PO1.6	PO1.5	PO1.4	PO1.3	PO1.2	PO1.1	PO1.0
EIO									—	—	—	—	—	IT0	EX0	IE0
PIO									PIO.7	PIO.6	PIO.5	PIO.4	PIO.3	PIO.2	PIO.1	PIO.0
PI1									—	PI1.6	PI1.5	PI1.4	PI1.3	PI1.2	PI1.1	PI1.0
HRNC									—	—	—	—	—	—	—	HRNE
PWCN									—	—	RSTD	REFO	LBF	LBIE	LBDE	BOD
WUTC									—	—	—	—	XTE	WTCS	WTF	WTE
WUT	WT19	WT18	WT17	WT16	WT15	WT14	WT13	WT12	WT11	WT10	WT9	WT8	WT7	WT6	WT5	WT4
PD0									PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
PD1									—	PD1.6	PD1.5	PD1.4	PD1.3	PD1.2	PD1.1	PD1.0
KEN0									KEN0.7	KEN0.6	KEN0.5	KEN0.4	KEN0.3	KEN0.2	KEN0.1	KEN0.0
KEN1									—	KEN1.6	KEN1.5	KEN1.4	KEN1.3	KEN1.2	KEN1.1	KEN1.0
ICDF									—	—	—	—	PSS1	PSS0	SPE	TXC
CMPC									CMON	ECMF	CMF	CMM	ECMO	CMO	CPOL	EXRF
T2CNA									ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
T2H									T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8
T2RH									T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8
T2CH									T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8
T2CNB									ET2L	T2OE1	T2POL1	TR2L	TF2	TCC2	TF2L	TC2L
T2V	T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8	T2V.7	T2V.6	T2V.5	T2V.4	T2V.3	T2V.2	T2V.1	T2V.0
T2R	T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8	T2R.7	T2R.6	T2R.5	T2R.4	T2R.3	T2R.2	T2R.1	T2R.0
T2C	T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8	T2C.7	T2C.6	T2C.5	T2C.4	T2C.3	T2C.2	T2C.1	T2C.0
T2CFG									—	DIV2	DIV1	DIV0	T2MD	CCF1	CCF0	C/T2

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Table 6. Peripheral Register Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									1	1	1	1	1	1	1	1
PO1									0	1	1	1	1	1	1	1
EI0									0	0	0	0	0	0	0	0
PI0									s	s	s	s	s	s	s	s
PI1									0	s	s	s	s	s	s	s
HRNC									0	0	0	0	0	0	0	0
PWCN									0	0	s	s	s	0	0	s
WUTC									0	0	0	0	0	0	0	0
WUT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PD0									0	0	0	0	0	0	0	0
PD1									0	0	0	0	0	0	0	0
KEN0									0	0	0	0	0	0	0	0
KEN1									0	0	0	0	0	0	0	0
ICDF									0	0	0	0	s	s	s	0
CMPC									0	0	1	0	0	0	0	0
T2CNA									0	0	0	0	0	0	0	0
T2H									0	0	0	0	0	0	0	0
T2RH									0	0	0	0	0	0	0	0
T2CH									0	0	0	0	0	0	0	0
T2CNB									0	0	0	0	0	0	0	0
T2V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG									0	0	0	0	0	0	0	0

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

System Timing

For maximum versatility, the MAXQ3210 generates its internal system clock from several sources:

- External clock source, including low-cost operation from 3.58MHz "Colorburst" crystal
- External crystal or ceramic resonator, using the internal oscillator
- External RC, using the internal relaxation oscillator
- Internal ring oscillator

A crystal warmup counter enhances operational reliability. Each time the external crystal oscillation must restart, such as after exiting stop mode, the device initiates a crystal warmup period of 65,536 oscillations.

This allows time for the crystal amplitude and frequency to stabilize before using it as a clock source. While in the warmup mode, the device operates from the internal 8kHz ring oscillator and can optionally switch back to the crystal as soon as the warmup period expires.

Internal Voltage Regulator

The MAXQ3210 features an internal voltage regulator that allows it to be powered from an external battery ranging from approximately 6.0V to 9.5V. A low-battery detect feature can set a flag and/or trigger an interrupt when enabled and the battery voltage falls below the V_{BF} threshold. The battery voltage is regulated to an internal voltage (V_{DDINT}) of approximately 5V. The REGOUT output pin provides 5V for use by external devices.

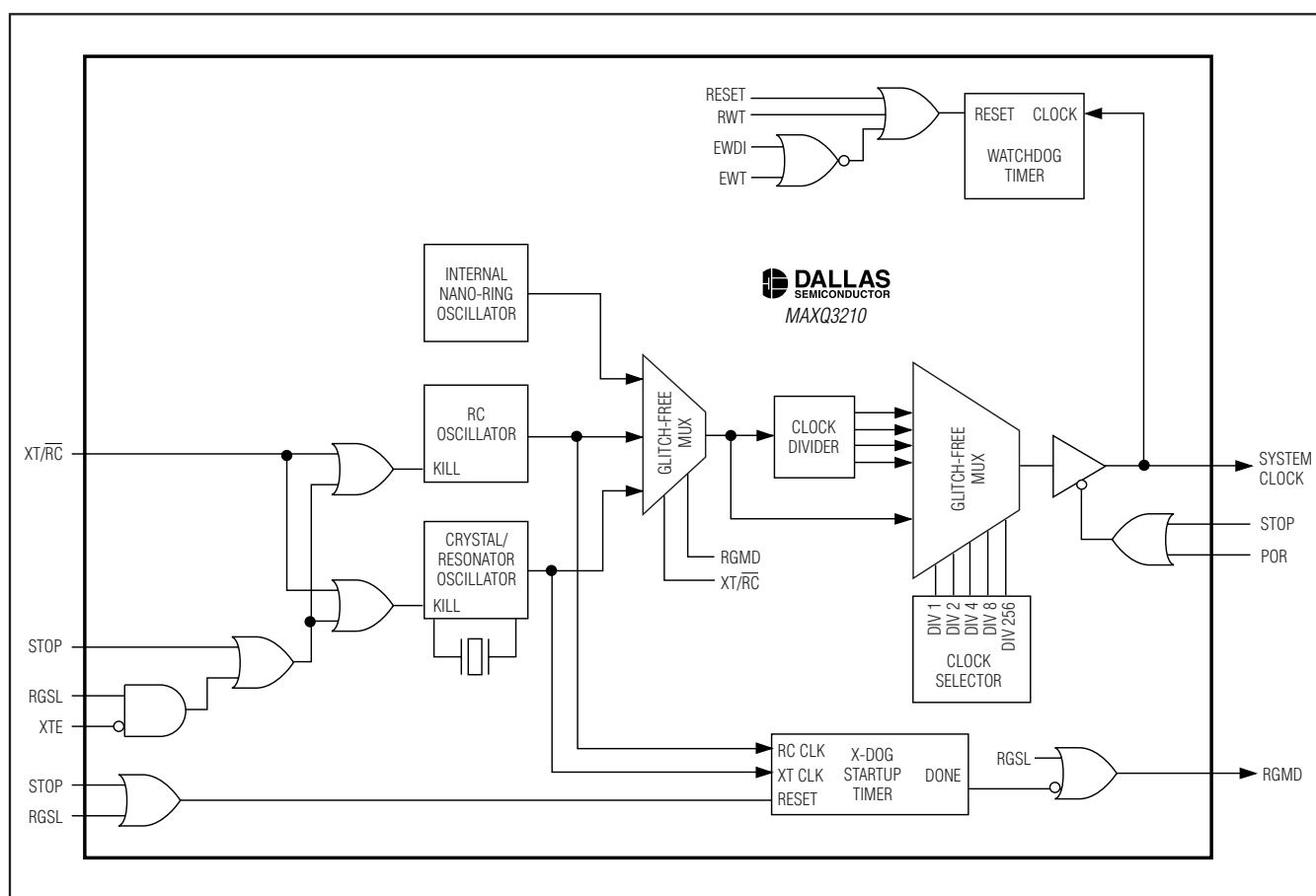


Figure 2. Clock Sources

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

Watchdog Timer Reset

The watchdog timer functions are described in the *MAXQ Family User's Guide*. Software can determine if a reset is caused by a watchdog timeout by checking the Watchdog Timer Reset Flag (WTRF) in the WDCN register. Execution resumes at location 8000h following a watchdog timer reset.

External System Reset

Asserting the external $\overline{\text{RESET}}$ pin low causes the device to enter the reset state. The external reset functions as described in the *MAXQ Family User's Guide*. Execution resumes at location 8000h after the $\overline{\text{RESET}}$ pin is released. The external system reset function is enabled by default on a power-on reset, but can be disabled and the pin used as general-purpose I/O by setting the Reset Pin Disable (RSTD) bit. The system designer is cautioned not to disable the reset pin early in the software as it could disable future JTAG access and/or bootloader capability.

I/O Ports

The microcontroller uses a form of Type D bidirectional I/O pins described in the *MAXQ Family User's Guide*. Each port has eight independent, general-purpose I/O pins and three configure/control registers. Many pins support alternate functions such as timers or interrupts, which are enabled, controlled, and monitored by dedicated peripheral registers. Using the alternate function automatically converts the pin to that function. The I/O pins on this device employ an optional "keeper" latch that helps to maintain the input pin state in the absence of external drive sources.

Port 0.7 is a special pin with a stronger pulldown capability to drive devices such as LEDs. It operates and is configured the same as other pins.

Type D port pins have Schmitt Trigger receivers and full CMOS output drivers, and can support special functions. The pin is either tri-stated or weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register. One pin of the device has interrupt capability.

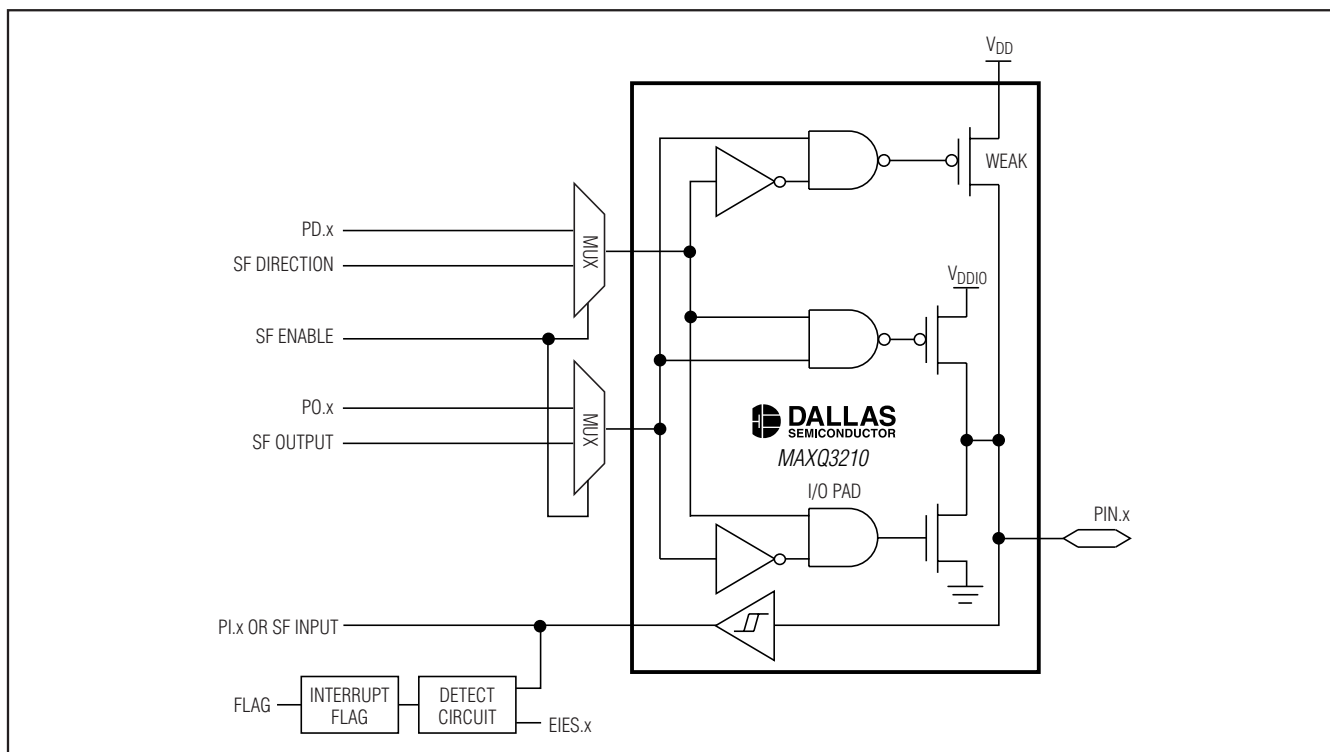


Figure 3. Type D Port Pin Schematic

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

Programmable Timer

The microcontroller incorporates one 16-bit programmable timer/counter. The type 2 timer (timer 2) can be used in counter/timer/capture/compare/PWM functions, allowing precise control of internal and external events. It also supports optional single-shot, external gating, and polarity control options.

Timer 2

The timer 2 peripheral includes the following:

- 16-bit auto-reload timer/counter
- 16-bit capture
- 16-bit counter
- 8-bit capture and 8-bit timer
- 8-bit counter and 8-bit timer

Wakeup Timer

The microcontroller includes a simple 20-bit wake-up timer that can be used to measure long intervals. The user-selectable timer period can be used to generate a long-period interrupt or wake the device out of stop mode. The timer can be clocked from either the currently active system clock or the 8kHz ring oscillator. In stop mode only the 8kHz ring oscillator is available as the wakeup timer clock source. As an interrupt, the feature increases overall performance by reducing many shorter timer interruptions to a single interrupt to measure the same long period. When used in stop mode, it provides the energy savings of the lowest power mode with periodic wakeup ability.

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupt-

ed, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer is controlled through bits in the WDCN register. Its timeout period can be set to one of four programmable intervals ranging from 2^{12} to 2^{21} system clocks in its default clock mode, allowing flexibility to support different types of applications. The interrupt occurs 512 system clocks before the reset, allowing the system to execute an interrupt and place the system in a known, safe state before the device performs a total system reset. At 3.58MHz, watchdog timeout periods can be programmed from 1.14ms to 149.94s, depending on the system clock mode.

Analog Comparator

The analog comparator is a one-bit, analog-to-digital comparator. The comparator input can be connected to a wide range of peripherals, including chemical sensors and motion or proximity detectors, or any other appropriate analog input. The comparator measures the analog input against either an external voltage reference or the internal +2.5V reference. When the level on the comparator input, CMPI, rises above the selected voltage reference, the CMO bit in the CMPC register is changed to the desired level. The device then responds by asserting an external signal and/or activating an internal interrupt request. The polarity of the external signal asserted is programmable. When not in use, the pins associated with the comparator are usable as general-purpose I/O.

In addition, the +2.5V reference is configurable to be output on the VREF pin. This provides an absolute voltage reference for use with data converters or other precision devices.

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The piezoelectric horn driver provides circuitry to drive a 3-pin piezoelectric horn/annunciator. These horns contain a ceramic element that bends or expands when a voltage is applied, generating a single tone capable of reaching 100dB. They can be used in a wide variety of applications requiring audible alerts such as theft, intrusion proximity or fire alarms, chemical sensors, door sensors, and safety monitors.



Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

In-Circuit Debug

Embedded debugging capability is available through the JTAG-compatible Test Access Port. Embedded debug hardware and embedded ROM firmware provide in-circuit debugging capability to the user application, eliminating the need for an expensive in-circuit emulator. Figure 5 shows a block diagram of the in-circuit debugger. The in-circuit debug features include:

- Hardware debug engine
- Set of registers able to set breakpoints on register, code, or data accesses
- Set of debug service routines stored in the utility ROM

The embedded hardware debug engine is an independent hardware block in the microcontroller. The debug engine can monitor internal activities and interact with selected internal registers while the CPU is executing user code. Collectively, the hardware and software features allow two basic modes of in-circuit debugging:

- Background mode allows the host to configure and set up the in-circuit debugger while the CPU continues to execute the application software at full speed. Debug mode can be invoked from background mode.
- Debug mode allows the debug engine to take control of the CPU, providing read/write access to internal registers and memory, and single-step trace operation.

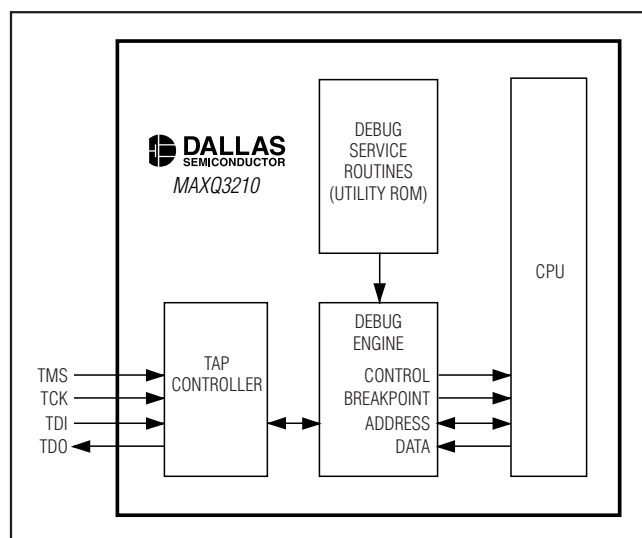


Figure 5. In-Circuit Debugger

Applications Information

Grounds and Bypassing

Careful PC board layout significantly minimizes crosstalk among the reference input, comparator outputs, and digital inputs. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Separate CMPI and VREF from each other by running a ground trace between these pins. Bypass VDD with a capacitor as low as 1μF and keep bypass capacitor leads short for best noise rejection.

Capacitor Selection and Regulator Stability

For general purposes, use a combination of a 10μF and 0.1μF capacitor on REGOUT. Note that the 0.1μF capacitor is always required on REGOUT and must be a good quality ceramic with low ESR. The internal regulator is designed to be stable with an output filter capacitor as low as 4.7μF and an ESR as high as 6Ω. Larger REGOUT capacitor values and lower ESR provide better supply-noise rejection and transient response. Note that some ceramic dielectric materials (e.g., Z5U and Y5V) exhibit a large temperature coefficient for both capacitance and ESR, and a larger REGOUT capacitance may be needed to ensure stability at low temperatures.

Applications

The low-power, high-performance RISC architecture of the MAXQ3210 makes it an excellent fit for many portable or battery-powered applications that require cost-effective computing. The analog comparator can function as an A/D converter when simple analog measurements are necessary, and the high-current I/O pin can drive a power or status LED. Combined with the high-output piezoelectric horn/transducer, the microcontroller can function as both the “brain” and “mouth” in a wide variety of monitoring applications.

The microcontroller includes an on-chip voltage regulator that allows it to be powered directly off a 9V battery. A low-battery detector allows the microcontroller to monitor its own battery condition. The internal voltage regulator can also drive external 5V circuitry while a 9V battery drives the system.

This device can also be used as a low-cost analog-to-digital converter (ADC). The single-slope conversion method can be easily implemented using the internal comparator and an internal timer. The basic implementation of such a converter is illustrated below. One of the benefits of this approach is the small number of

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

external components required: the transistor creates a constant current source, a ramp capacitor times the conversion, and a resistor and capacitor on the comparator input acting as a simple filter. The result is the addition of A/D capability to the end system at virtually no additional cost.

Additional Documentation

Designers must have four documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation.

- The MAXQ3210 data sheet, which contains electrical/timing specifications and pin descriptions, available at www.maxim-ic.com/MAXQ3210.
- The MAXQ3210 errata sheet for the specific device revision, available at www.maxim-ic.com/errata.
- The *MAXQ Family User's Guide*, which contains detailed information on core features and operation, including programming, available at www.maxim-ic.com/MAXQUG.

- The *MAXQ Family User's Guide: MAXQ3210/MAXQ3212 Supplement*, which contains detailed information on features specific to the MAXQ3210, available at www.maxim-ic.com/MAXQ32xxSUP.

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this microcontroller are available from Maxim/Dallas Semiconductor and third-party suppliers, including:

- Compilers
- In-circuit emulators
- Integrated development environments (IDEs)
- JTAG-to-serial converters for programming and debugging

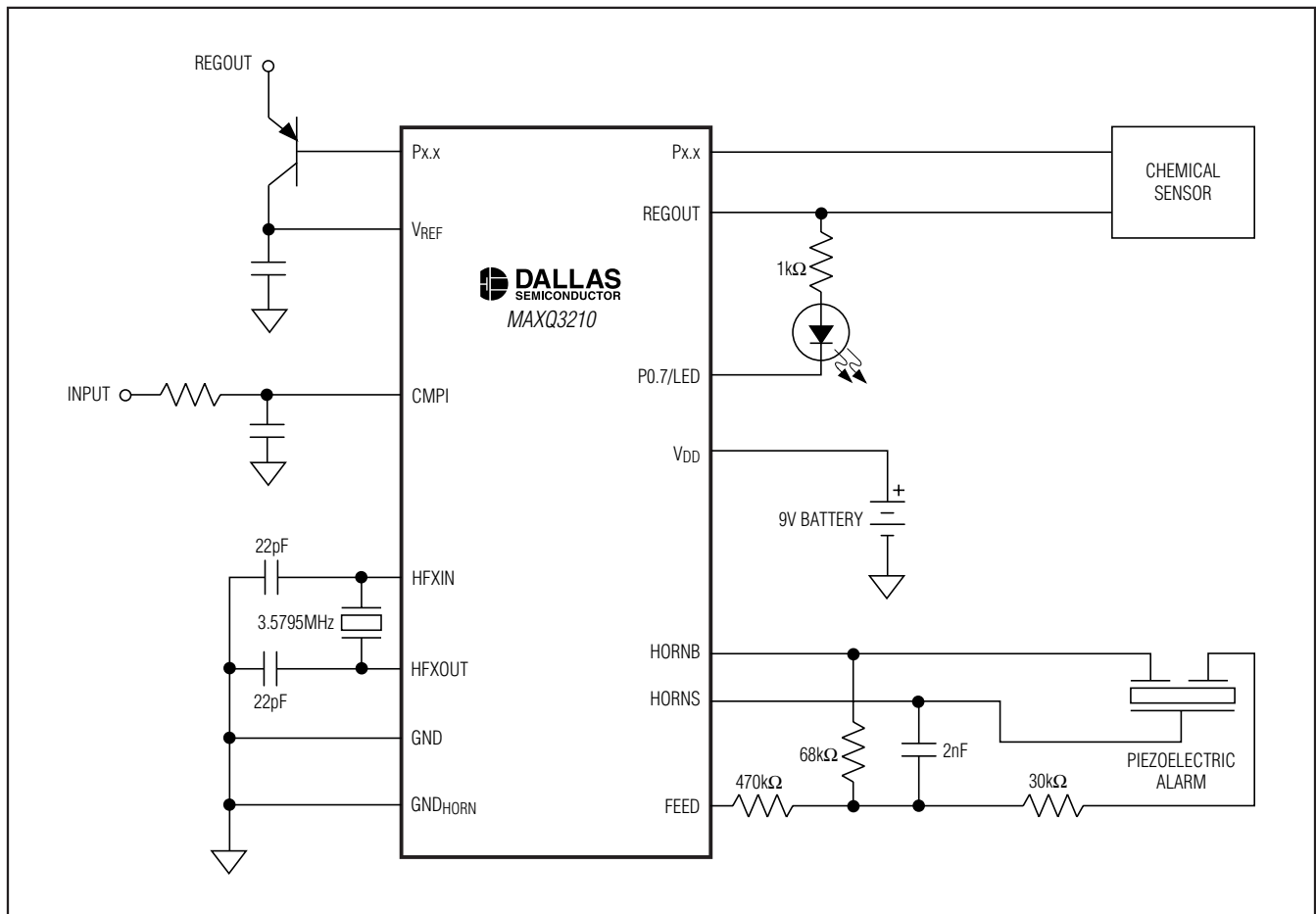
A partial list of development tool vendors can be found at www.maxim-ic.com/MAXQ_tools.

For technical support, go to www.maxim-ic.com/support.

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

Typical Chemical Sensor Application Using A Simple SAR ADC

MAXQ3210



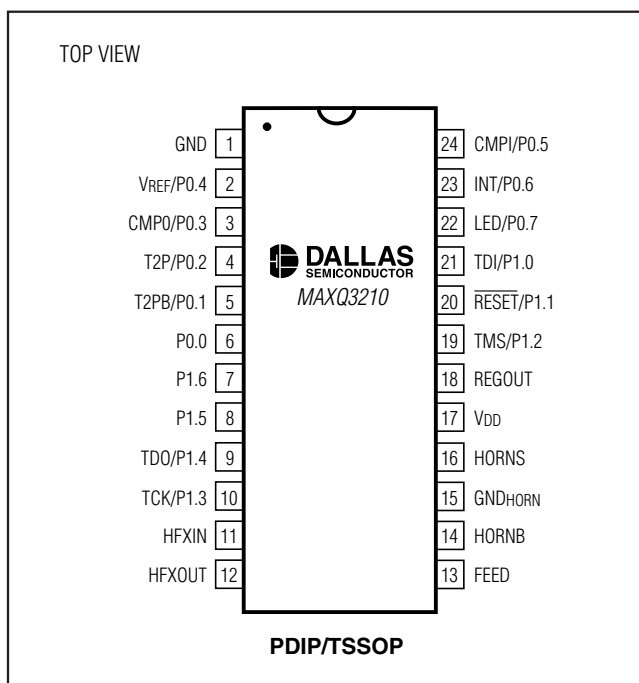
Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

Ordering Information

PART	TEMP RANGE	NOMINAL V _{DD} (V)	MEMORY	PIN-PACKAGE
MAXQ3210-EJX	-40°C to +85°C	9	1kWord EEPROM	24 TSSOP
MAXQ3210-EJX+	-40°C to +85°C	9	1kWord EEPROM	24 TSSOP
MAXQ3210-EMX	-40°C to +85°C	9	1kWord EEPROM	24 PDIP
MAXQ3210-EMX+	-40°C to +85°C	9	1kWord EEPROM	24 PDIP

+Denotes a Pb-free/RoHS-compliant package.

Pin Configuration



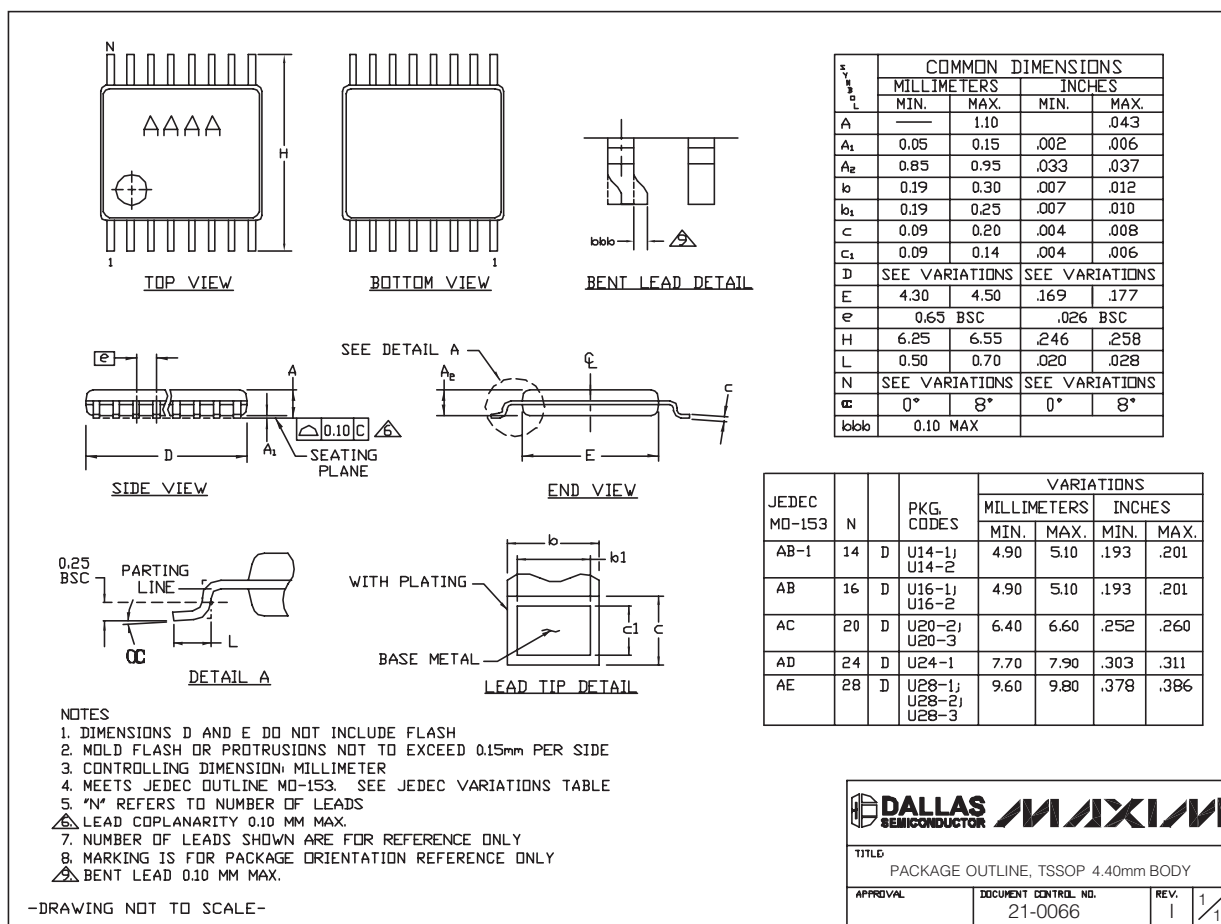
Revision History

- Rev 0; 1/06: Original release.
- Rev 1; 5/06: Changed units on Active Current (Electrical Characteristics) from "μA" to "mA" for IDD5 and IDD6.

Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



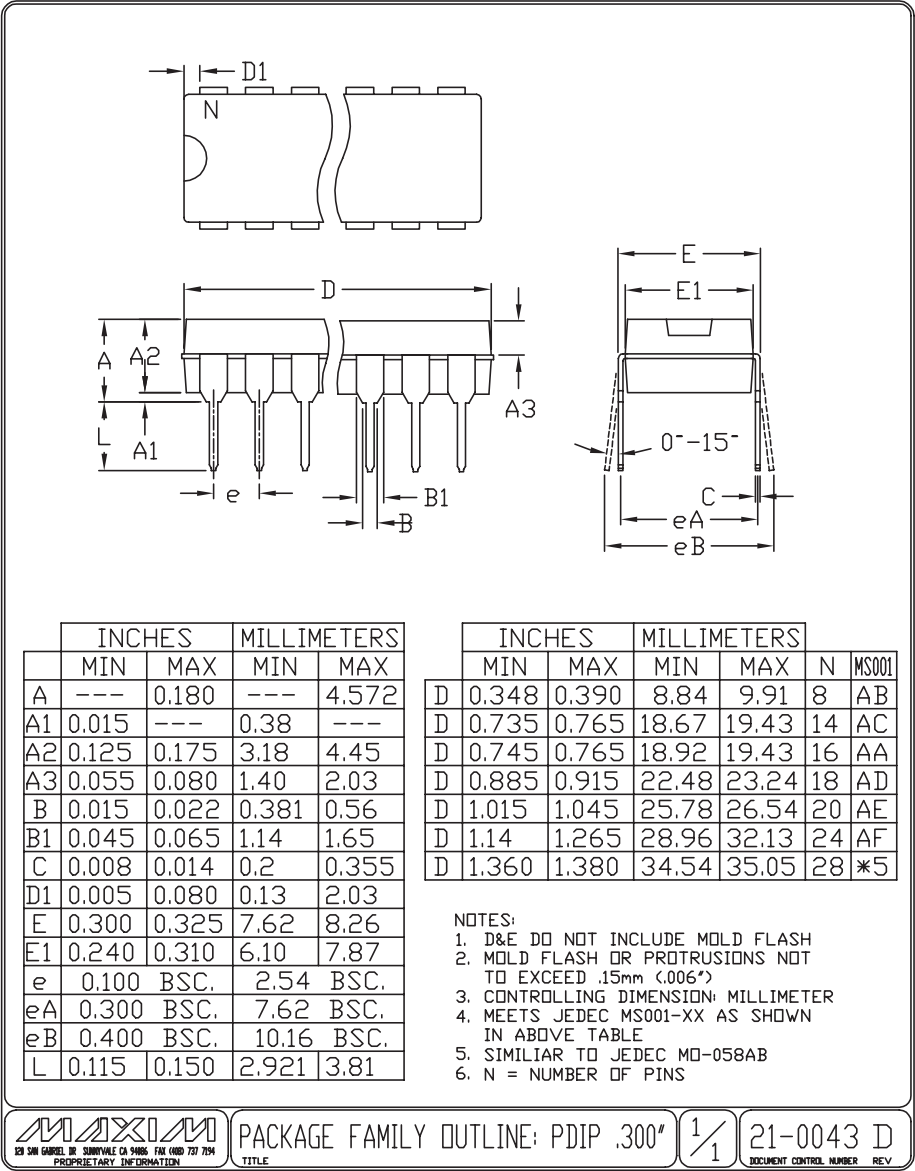
TSSOP4.40mm:EPS

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Microcontroller with Internal Voltage Regulator, Piezoelectric Horn Driver, and Comparator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



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