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What is "Embedded - Microcontrollers"?

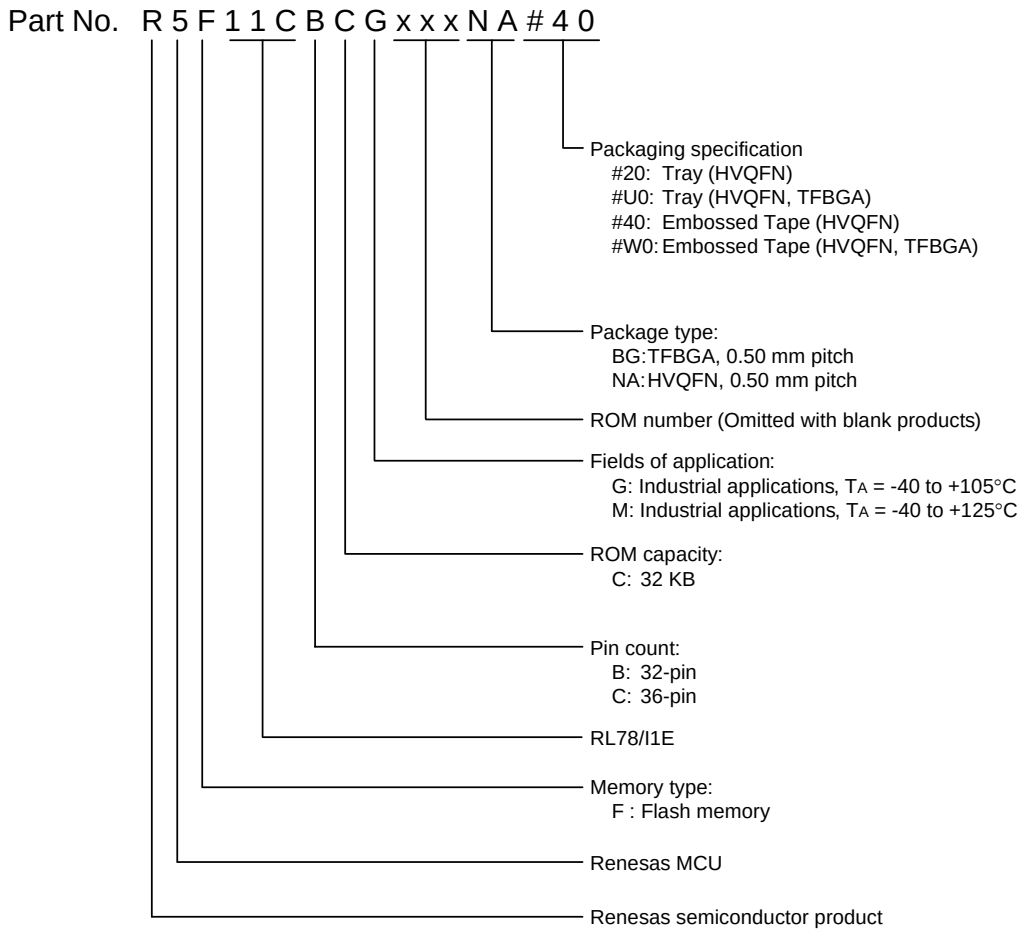
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	10
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b, 3x24b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11cbcgna-20

1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/I1E



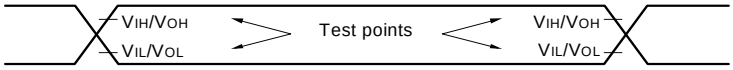
Pin count	Package	Fields of Application Note	Ordering Part Number
32 pins	32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)	G	R5F11CBCGNA#20 R5F11CBCGNA#40
		M	R5F11CBCMNA#U0 R5F11CBCMNA#W0
36 pins	36-pin plastic TFBGA (4 × 4 mm, 0.5 mm pitch)	G	R5F11CCCGBG#U0 R5F11CCCGBG#W0
		M	R5F11CCCMBG#U0 R5F11CCCMBG#W0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/I1E**.

Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

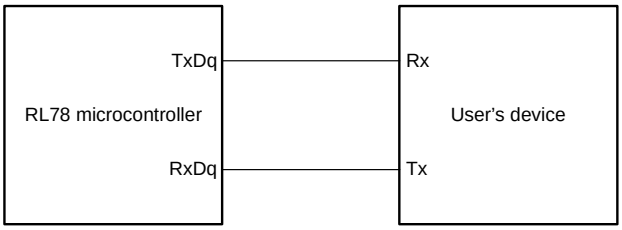
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1				f_{MCK}/12	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

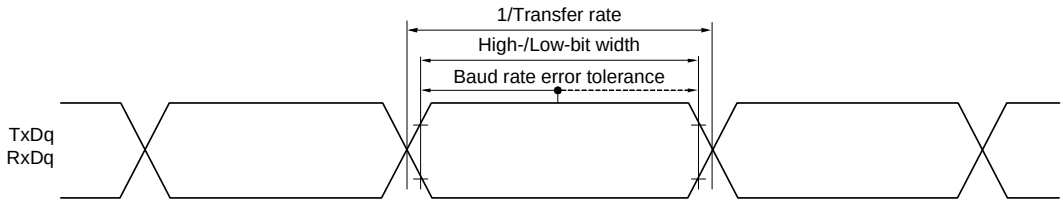
Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	250		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 24		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 36		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 30 pF Note 3			50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		12/f_{MCK} and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 66	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 113	ns
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	400		ns

Note 1. The maximum transfer rate in the SNOOZE mode is 1 Mbps.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/3)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	600		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	1000		ns
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 340		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 916		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 24		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 36		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 100		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/3)

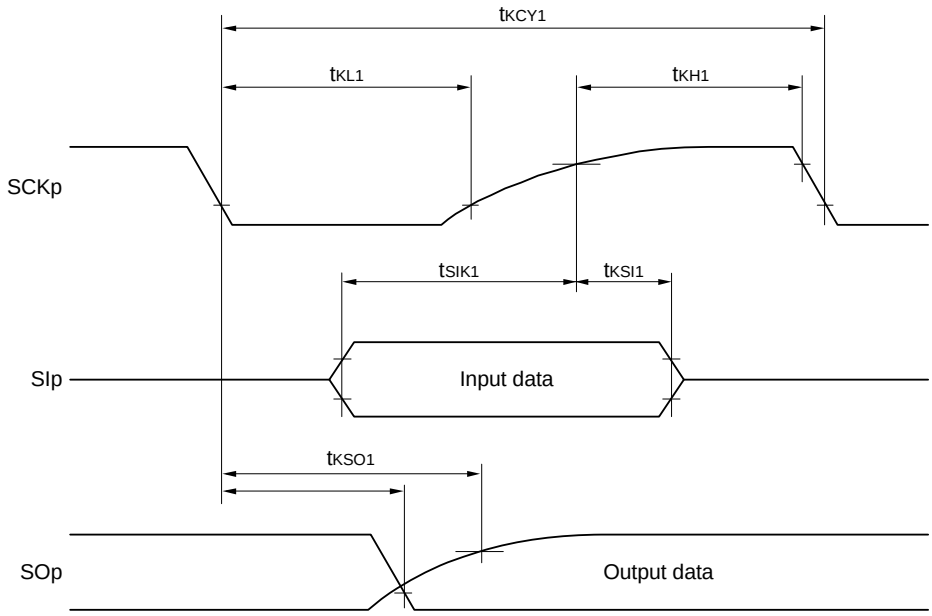
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) Note	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output Note	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

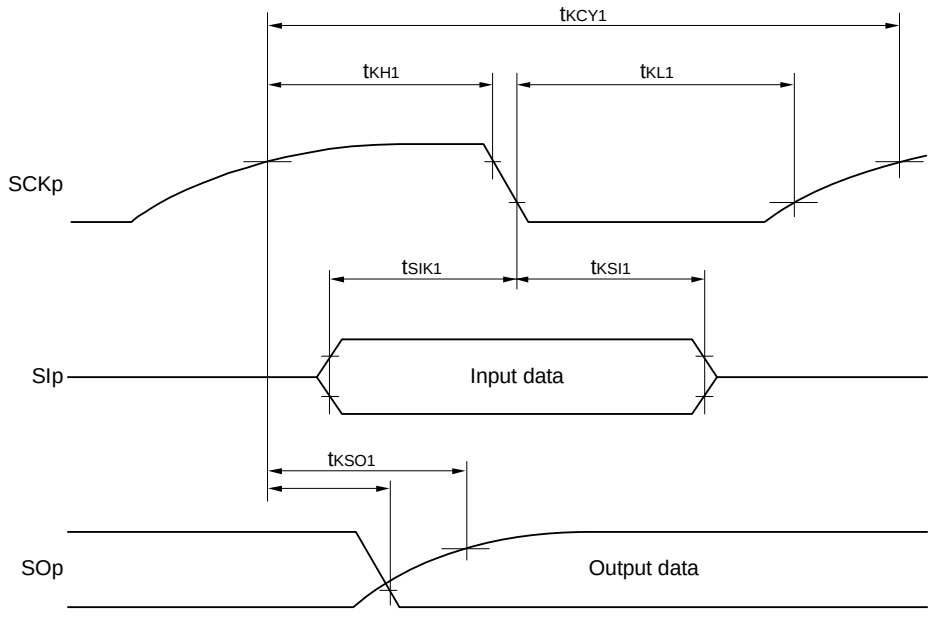
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

2.6.2 Sensor power supply (SBIAS)

(T_A = -40 to +105°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, C_{OUT} = 0.22 µF, V_{OUT} = 1.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage range	V_{OUT}		0.5		2.2	V
Output voltage setting steps	V_{STEP}			0.1		V
Output voltage precision	V_A	I_{OUT} = 1 mA	(-3)		(+3)	%
Maximum output current	I_{OUT}		5			mA
Short circuit current	I_{SHORT}	V_{OUT} = 0 V		40	65	mA
Load regulation	L_R	1 mA ≤ I_{OUT} ≤ 5 mA			(15)	mV
Power supply rejection ratio	PSRR	AV_{DD} = 5.0 V + 0.1 $V_{pp\ ripple}$ f = 100 Hz, I_{OUT} = 2.5 mA	(45)	(50)		dB

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

2.6.3 Temperature sensor

(T_A = -40 to +105°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature coefficient for sensor	TC_{SNS}			(756)		µV/°C
Sensor output voltage	V_{TEMP}	T_A = 25°C		226.4		mV

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

2.6.6 Configurable amplifier

(T_A = -40 to +105°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, V_{COM} = 1/2 AV_{DD}, internally connected voltage follower)

AMP0 configuration SW setting: Positive (+) pin = ANX1, negative (-) pin = ANX0

AMP1 configuration SW setting: Positive (+) pin = ANX3, negative (-) pin = ANX2

AMP2 configuration SW setting: Positive (+) pin = ANX5, negative (-) pin = ANX4

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{IN}		AV_{SS}		AV_{DD}	V
Output voltage	V_{OL}	I_L= -1 mA, AV_{DD} = 2.7 to 5.5 V		AV_{SS} +0.02	AV_{SS} +0.07	V
	V_{OH}	I_L= 1 mA, AV_{DD} = 2.7 to 5.5 V	AV_{DD} -0.15	AV_{DD} -0.02		V
Maximum output current	I_{OUT}	4.5 V ≤ AV_{DD} ≤ 5.5 V	±10			mA
		2.7 V ≤ AV_{DD} ≤ 5.5 V	±5			mA
Input-referred offset voltage	V_{OFF}	T_A = 25°C without trimming I_L = 0 mA, V_{COM} = 1.0 V		±1	±4	mV
		T_A = 25°C with trimming I_L = 0 mA, V_{COM} = 1.0 V			±0.35	mV
Temperature coefficient for inputreferred offset voltage	V_{OTC}	I_L = 0 mA		(±2)	(±8)	µV/°C
Slew rate	SR1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(0.1)		V/µs
	SR2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(0.8)		V/µs
Gain bandwidth	GBW1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(350)		kHz
	GBW2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(1.8)		MHz
Phase margin	θM1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(70)		deg
	θM2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(60)		deg
Settling time	tset1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(20)		µs
	tset2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(10)		µs
Peak-to-peak voltage noise	Enb	0.1 to 10 Hz Normal mode C_L = 50 pF, R_L = 10 kΩ		(2.0)		µVrms
Input-referred noise	En	f = 1 kHz, Normal mode C_L = 50 pF, R_L = 10 kΩ		(70)		nV/√Hz
Common mode rejection ratio	CMRR	f = 1 kHz, C_L = 50 pF, R_L = 10 kΩ		(70)		dB
Power supply rejection ratio	PSRR	2.7 V ≤ AV_{DD} ≤ 5.5 V f = 1 kHz, C_L = 50 pF, R_L = 10 kΩ		(62)		dB

(Remarks are listed on the next page.)

2.6.9 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				50	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

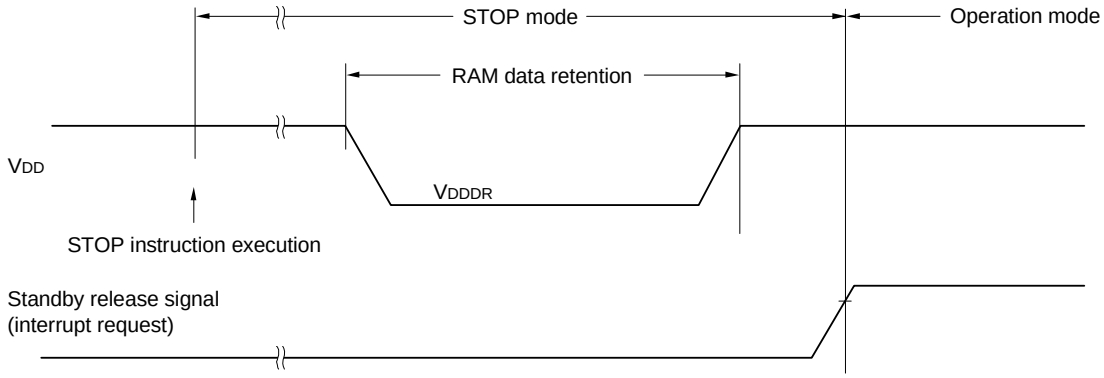
<R> 2.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 Notes 1, 2		5.5	V

Note 1. The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Note 2. Enter STOP mode before the supply voltage falls below the recommended operating voltage.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 5.5 V	1		32	MHz
<R> Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C Note 4	1,000			Times
<R> Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T_A = 25°C Note 4		1,000,000		
		Retained for 5 years T_A = 85°C Note 4	100,000			
		Retained for 20 years T_A = 85°C Note 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> **Note 4.** This temperature is the average value at which data are retained.

3.4 AC Characteristics

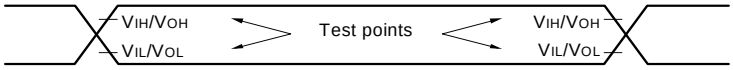
(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	µs
			2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
		In the self-programming mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	µs
			2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1.0		8.0	MHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V		24			ns
		2.4 V ≤ V_{DD} < 2.7 V		60			ns
TI00 to TI03, TI10, TI11 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK} + 10			ns
Timer RJ input cycle	f_C	TRJIO0	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
			2.4 V ≤ V_{DD} < 2.7 V	300			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO0	2.7 V ≤ V_{DD} ≤ 5.5 V	40			ns
			2.4 V ≤ V_{DD} < 2.7 V	120			ns
Timer RG input high-level width, low-level width	t_{TGIH}, t_{TGIL}	TRGIOA, TRGIOB		2.5/f_{CLK}			ns
TO00 to TO03, TO10, TO11, TRJIO0, TRJO0, TRGIOA, TRGIOB output frequency	f_{TO}		4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
			2.7 V ≤ V_{DD} ≤ 4.0 V			6	MHz
			2.4 V ≤ V_{DD} < 2.7 V			3	MHz
PCLBUZ0 output frequency	f_{PCL}		4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
			2.7 V ≤ V_{DD} ≤ 4.0 V			6	MHz
			2.4 V ≤ V_{DD} < 2.7 V			3	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP1 to INTP7		1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

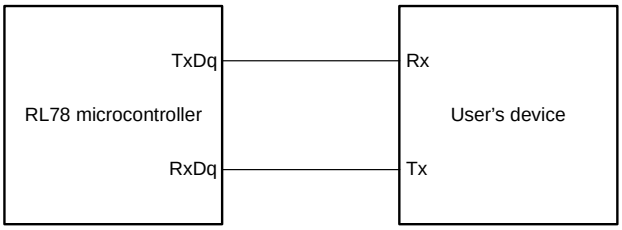
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1				fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 2		2.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

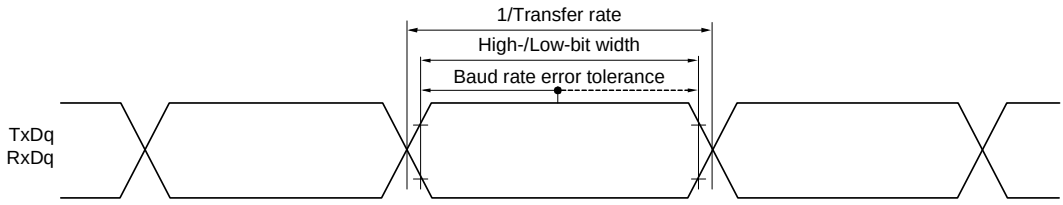
Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
24 MHz (2.7 V ≤ VDD ≤ 5.5 V)
16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



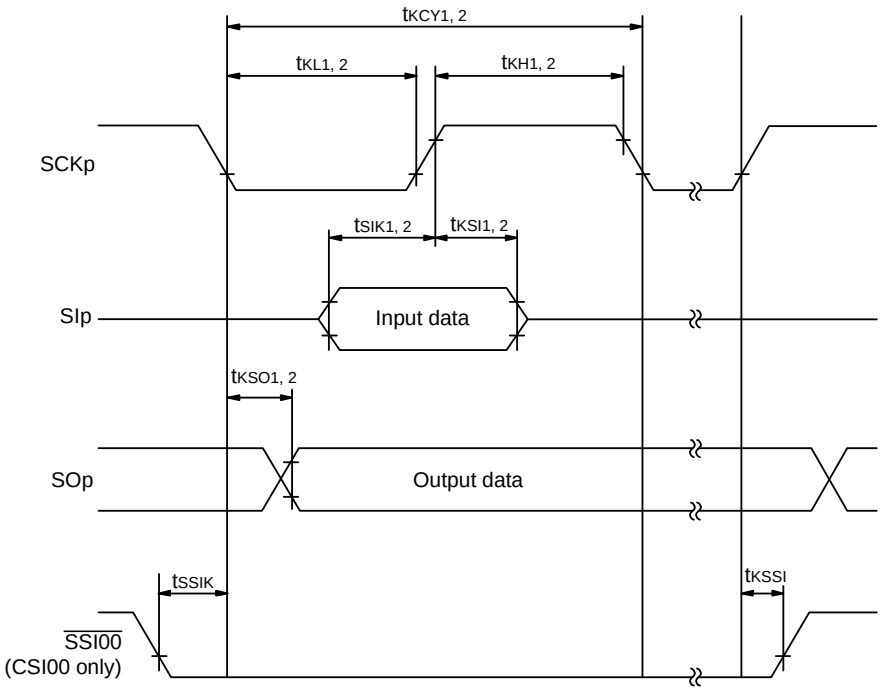
UART mode bit width (during communication at same potential) (reference)



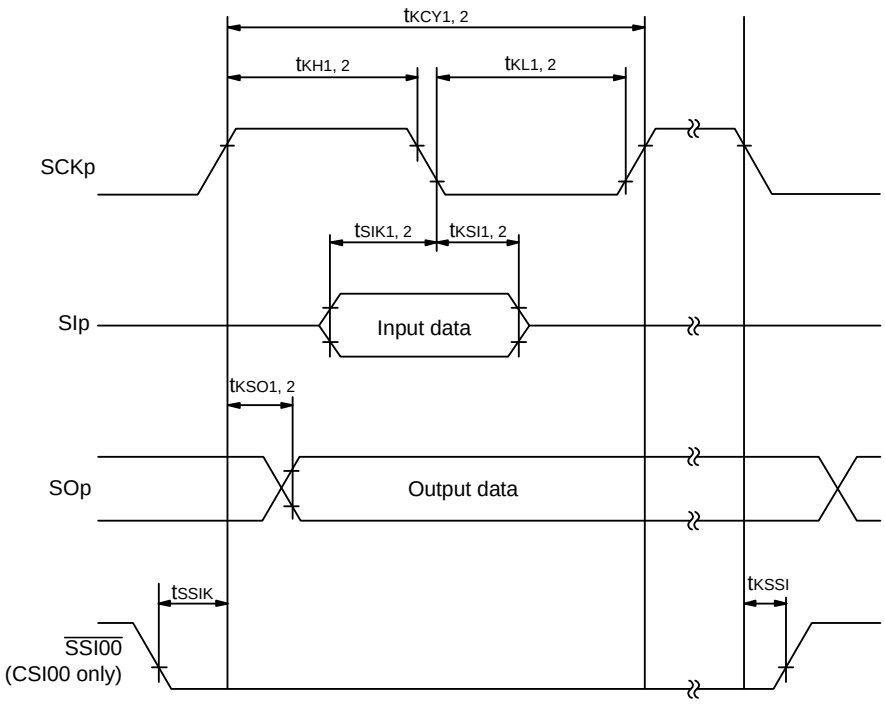
Remark 1. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01)
Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

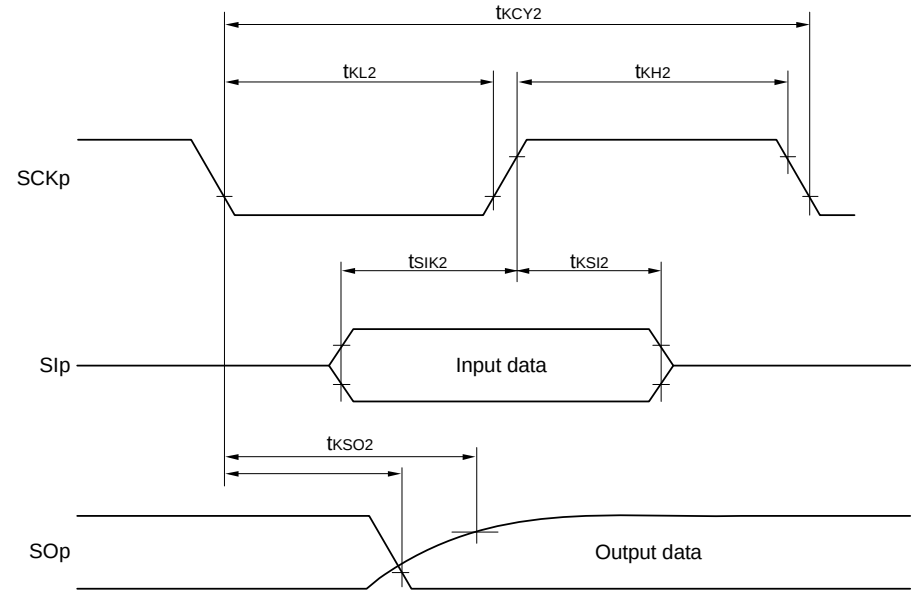
(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

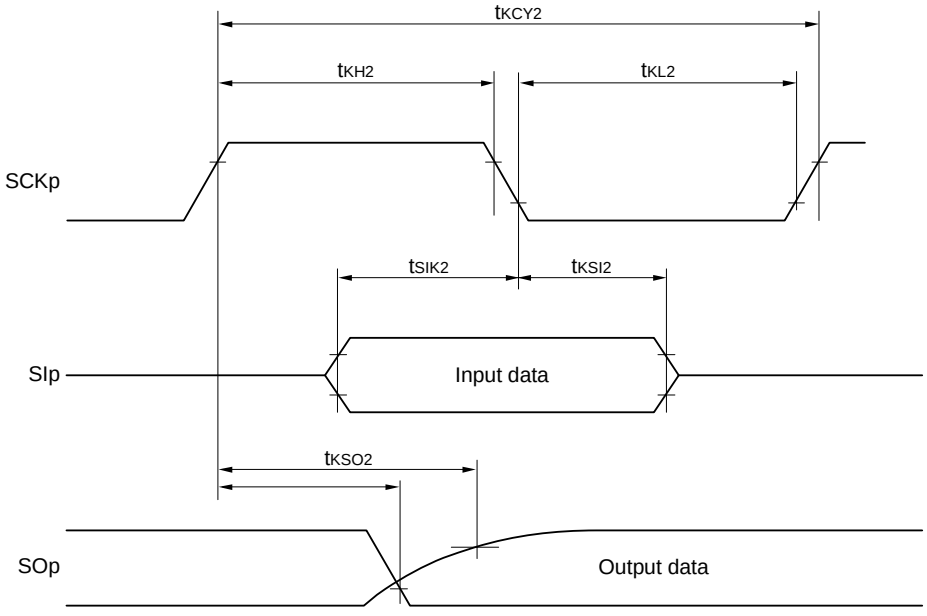
Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 24		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 36		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 - 100		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 40		ns
<R>		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40		ns
<R>		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 240	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 1146	ns

(Notes, Cautions, and Remarks are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

Remark 2. Communication at different potential cannot be performed during clocked serial communication with the slave select function.

3.6 Analog Characteristics

3.6.1 Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter

(1) Analog input in differential input mode

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, d_{OFR} = 0 mV, V_{COM} = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Full-scale differential input voltage range	V_{ID}	V_{ID} = (PGAxP - PGAxN) (x = 0 to 3)		± 800 /G_{TOTAL}		mV
Input voltage range	V_I	Each of PGAxP and PGAxN pins (x = 0 to 3)	0.2		1.8	V
Common mode input voltage	V_{COM}	d_{OFR} = 0 mV	0.2+(|V_{ID}|x G_{SET1})/2		1.8-(|V_{ID}|x G_{SET1})/2	V
Input bias current	I_{IN}	V_I = 1.0 V			± 50	nA
Input offset current	I_{INOFR}	V_I = 1.0 V			± 20	nA

(2) Analog input in single-ended input mode

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, d_{OFR} = 0 mV, V_{COM} = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	V_I	Each of PGAxP and PGAxN pins (x = 0 to 3) G_{SET1} = 1, G_{SET2} = 1	0.2		1.8	V
Input bias current	I_{IN}	V_I = 1.0 V			± 50	nA

(3) Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, d_{OFR} = 0 mV, V_{COM} = 1.0 V, external clock input used, in differential input mode) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				24	bit
Sampling frequency	f_{S1}	Normal mode		1		MHz
	f_{S2}	Low power mode		0.125		MHz
Output data rate	f_{DATA1}	Normal mode	0.48828		15.625	ksps
	f_{DATA2}	Low power mode	61.03615		1953.125	sps
Gain setting range	G_{TOTAL}	G_{TOTAL} = G_{SET1} × G_{SET2}	1		64	V/V
1st gain setting range	G_{SET1}	In differential input mode only		1, 2, 3, 4, 8		V/V
2nd gain setting range	G_{SET2}	In differential input mode only		1, 2, 4, 8		V/V
Offset adjustment bit range	d_{OFFB}			5		bit
Offset adjustment range	d_{OFR}	Referred to input	-164/G_{SET1}		+164/G_{SET1}	mV
Offset adjustment steps	d_{OFS}	Referred to input		11/G_{SET1}		mV

3.6.4 A/D converter characteristics

(1) When positive reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = AV_{DD}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V		1.2	±6.5	LSB
			2.7 V ≤ AV_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ AV_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ AV_{DD} ≤ 5.5 V	3.1875		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
			2.7 V ≤ AV_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI9		AV_{SS}		AV_{DD}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The number of pins depends on the product. For details, see a list of pin functions.

(2) When positive reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = V_{BGR}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±1.0	LSB
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ AV_{DD} ≤ 5.5 V		V_{BGR} Note 3			V
Analog input voltage	V_{AIN}	ANI0 to ANI9		0		V_{BGR}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. See the Internal reference voltage characteristics.

3.6.5 12-bit D/A converter

(1) When positive reference voltage (+) = AV_{DD} (DACVRF = 0)

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = AV_{DD})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES				(12)	bit
Output voltage range	DAOUT	12-bit resolution	0.35		AV_{DD}-0.47	V
Integral non-linearity error	DAILE	12-bit resolution			±4.0	LSB
Differential non-linearity error	DADLE	12-bit resolution			±1.0	LSB
Offset error	DAErr	12-bit resolution			±30	mV
Gain error	DAEG	12-bit resolution			±20	mV
Settling time	DAtset	12-bit resolution, C_L = 50 pF, R_L = 10 kΩ			(60)	µs

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.
Remark 2. The 12-bit D/A converter characteristics are the values obtained with the configurable amplifier connected.

(2) When positive reference voltage (+) = internal reference voltage (DACVRF = 1)

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = VREFDA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES				(8)	bit
Internal reference voltage	VREFDA	8-bit resolution	1.34	1.45	1.54	V
Output voltage range	DAOUT	8-bit resolution	0.35		VREFDA	V
Integral non-linearity error	DAILE	8-bit resolution			±1.0	LSB
Differential non-linearity error	DADLE	8-bit resolution			±1.0	LSB
Offset error	DAErr	8-bit resolution			±30	mV
Gain error	DAEG	8-bit resolution			±20	mV
Settling time	DAtset	8-bit resolution, C_L = 50 pF, R_L = 10 kΩ			(60)	µs

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.
Remark 2. The 12-bit D/A converter characteristics are the values obtained with the configurable amplifier connected.
Remark 3. Offset error and gain error do not include error in the internal reference voltage.

3.6.8 LVD characteristics

(1) LVD detection voltage in reset mode and interrupt mode

(T_A = -40 to +125°C, $V_{PDR} \le AV_{DD} = V_{DD} \le$ 5.5 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD0}	Rising edge	4.62	4.74	4.94	V
			Falling edge	4.52	4.64	4.84	V
		V_{LVD1}	Rising edge	4.50	4.62	4.82	V
			Falling edge	4.40	4.52	4.71	V
		V_{LVD2}	Rising edge	4.30	4.42	4.61	V
			Falling edge	4.21	4.32	4.51	V
		V_{LVD3}	Rising edge	3.13	3.22	3.39	V
			Falling edge	3.07	3.15	3.31	V
		V_{LVD4}	Rising edge	2.95	3.02	3.17	V
			Falling edge	2.89	2.96	3.09	V
		V_{LVD5}	Rising edge	2.74	2.81	2.95	V
			Falling edge	2.68	2.75	2.88	V
		V_{LVD6}	Rising edge	2.55	2.61	2.74	V
			Falling edge	2.49	2.55	2.67	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

(2) LVD detection voltage in interrupt & reset mode

(T_A = -40 to +125°C, $V_{PDR} \le AV_{DD} = V_{DD} \le$ 5.5 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	V_{LVDD6}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage		2.49	2.55	2.67	V
	V_{LVDD4}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.17	V
			Falling interrupt voltage	2.89	2.96	3.09	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.13	3.22	3.39	V
			Falling interrupt voltage	3.07	3.15	3.31	V
	V_{LVDD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage		2.68	2.75	2.88	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.61	V
			Falling interrupt voltage	4.21	4.32	4.51	V
	V_{LVDD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage		2.68	2.75	2.88	V
	V_{LVDD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.82	V
			Falling interrupt voltage	4.40	4.52	4.71	V
	V_{LVDD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage		2.68	2.75	2.88	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.39	V
			Falling interrupt voltage	3.07	3.15	3.31	V
	V_{LVDD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.94	V
			Falling interrupt voltage	4.52	4.64	4.84	V

3.9 Dedicated Flash Memory Programmer Communication (UART)

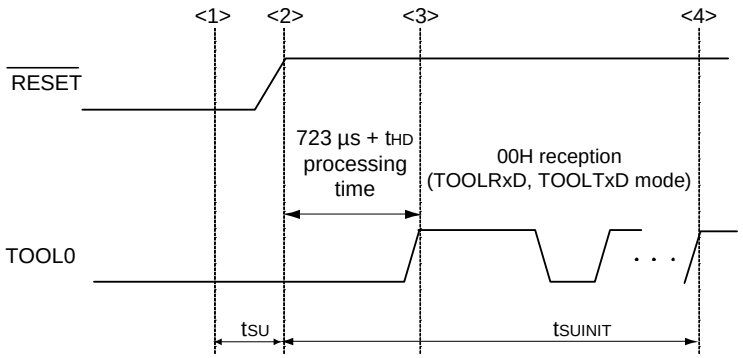
(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing for Switching Flash Memory Programming Modes

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)