Renesas Electronics America Inc - R5F11CBCMNA#U0 Datasheet

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What is "Embedded - Microcontrollers"?

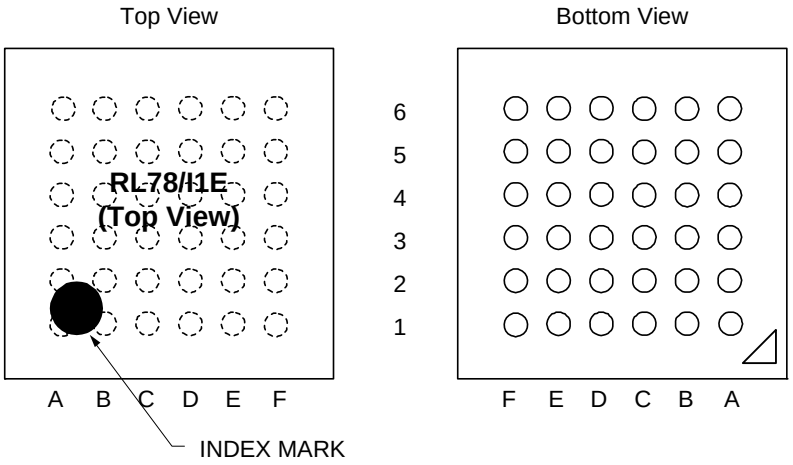
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	10
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b, 3x24b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11cbcmna-u0

1.3.2 36-pin products

<R> • 36-pin plastic TFBGA (4 × 4 mm, 0.5 mm pitch)



	A	B	C	D	E	F	
6	PGA2P	PGA1N	PGA1P	PGA0P	PGA3P	AVSS	6
5	PGA2N	P40/TOOL0	PGA0N	PGA3N	REGA	SBIAS	5
4	$\overline{\text{RESET}}$	P137/$\overline{\text{SSI00}}$/INTP0	P11/SI01/RXD1/SDA01/TI03/TO03/INTP2/TRGCLKA/TRJIO0	P12/SCK01/SCL01/TI11/TO11/INTP3/PCLBUZ0/TRGIOB/TRJO0	ANI0	AVDD	4
3	P122/EXCLK/X2	P15/SCK00/SCL00/TI10/TO10/INTP6/TRGCLKB	P10/SO01/TXD1/TI01/TO01/INTP1/TRGIOA	ANI3/AMP0P/ANX1	ANI2/AMP0N/ANX0	ANI1/AMP0O	3
2	P121/X1	REGC	P14/SI00/RXD0/SDA00/TI02/TO02/INTP5/TOOLRXD	P41/ANI6/AMP1P/ANX3	P42/ANI5/AMP1N/ANX2	ANI4/AMP1O	2
1	VDD	VSS	P13/SO00/TXD0/TI00/TO00/INTP4/TOOLTXD/RTC1HZ	P16/INTP7/ANI9/AMP2P/ANX5	P17/ANI8/AMP2N/ANX4	ANI7/AMP2O	1
	A	B	C	D	E	F	

Caution 1. Connect the REGC pin to the VSS pin via a capacitor (0.47 to 1 μF).
Caution 2. Connect the REGA pin to the AVSS pin via a capacitor (0.22 μF).
Caution 3. Make the AVSS pin the same potential as the VSS pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect the SBIAS pin to the AVSS pin via a capacitor (0.22 μF).

• AFE functions

(T_A = -40 to +105°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

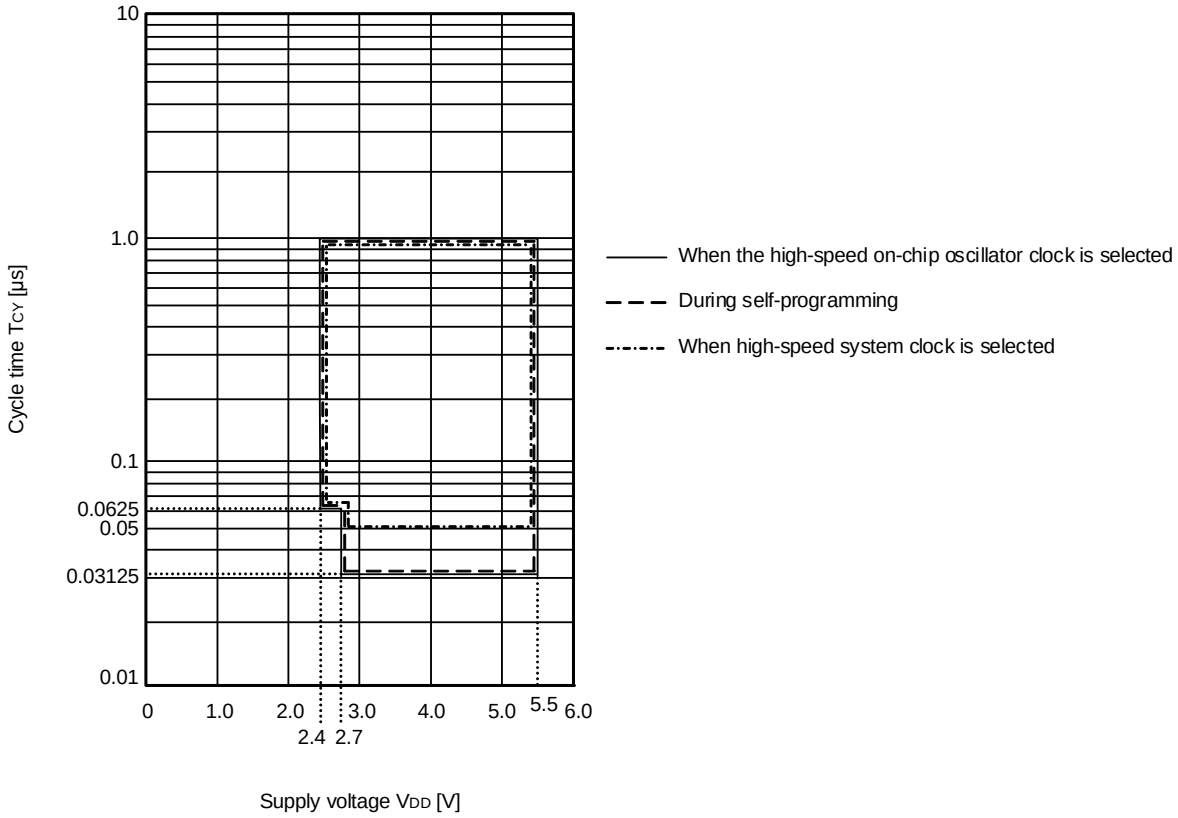
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
24-bit ΔΣ A/D converter operating current	I_{DSAD}	Normal mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA, 24-bit ΔΣ A/D converter, and digital filter Differential input mode OSR = 256 SBIAS I_{OUT} = 0 mA		0.94	1.46	mA
		Low power mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA, 24-bit ΔΣ A/D converter, and digital filter Differential input mode OSR = 256 SBIAS I_{OUT} = 0 mA		0.60	0.91	mA
10-bit A/D converter operating current	I_{ADC}	During conversion at the highest speed Notes 1, 2 AV_{DD} = 5.0 V		1.30	1.70	mA
Configurable amplifier operating current	I_{AMP}	Normal mode Notes 1, 2 Circuits that operate: ABGR and configurable amplifier I_L = 0 mA Per channel		0.13	0.24	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR and configurable amplifier I_L = 0 mA Per channel		0.30	0.45	mA
12-bit D/A converter operating current	I_{DAC}	When AV_{DD} is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR and internal reference voltage (VREFDA)		0.61	0.97	mA

Note 1. Current flowing to AV_{DD}

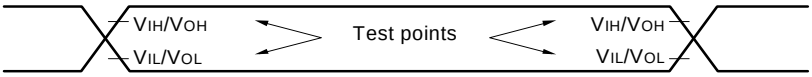
Note 2. Current flowing only to the circuits that operate shown in the Conditions column.

Minimum Instruction Execution Time During Main System Clock Operation

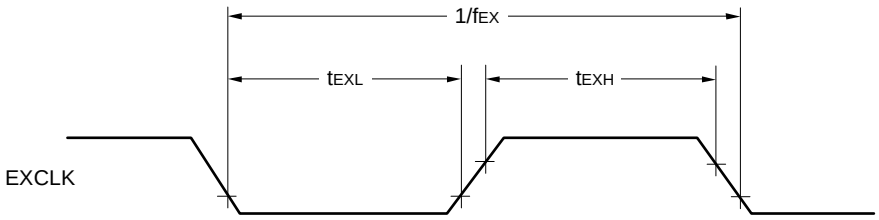
TCY vs VDD



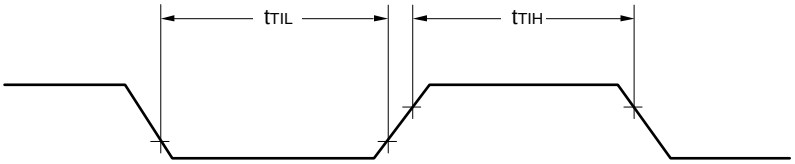
AC Timing Test Points

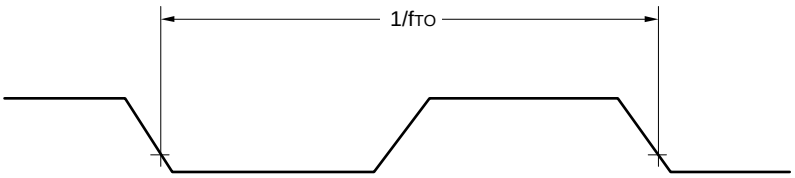


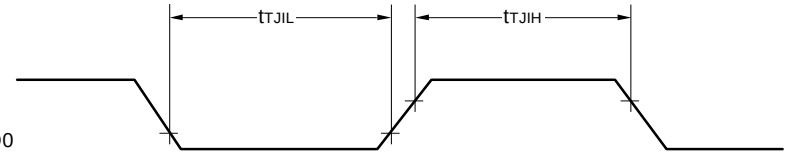
External System Clock Timing

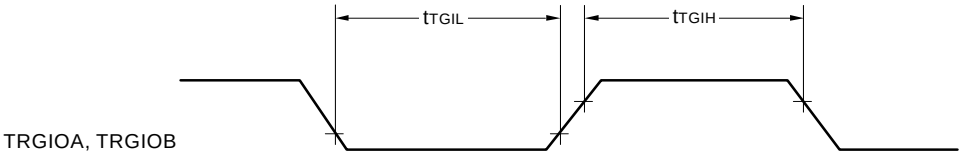


TI/TO Timing

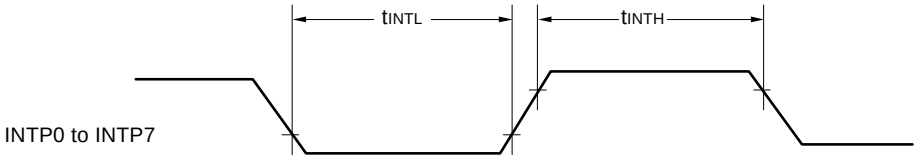




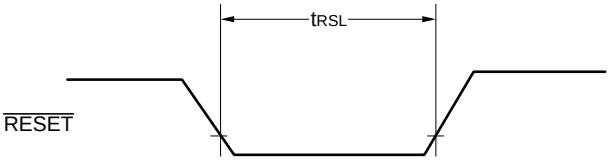




Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220 Note 2		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.6	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.6	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

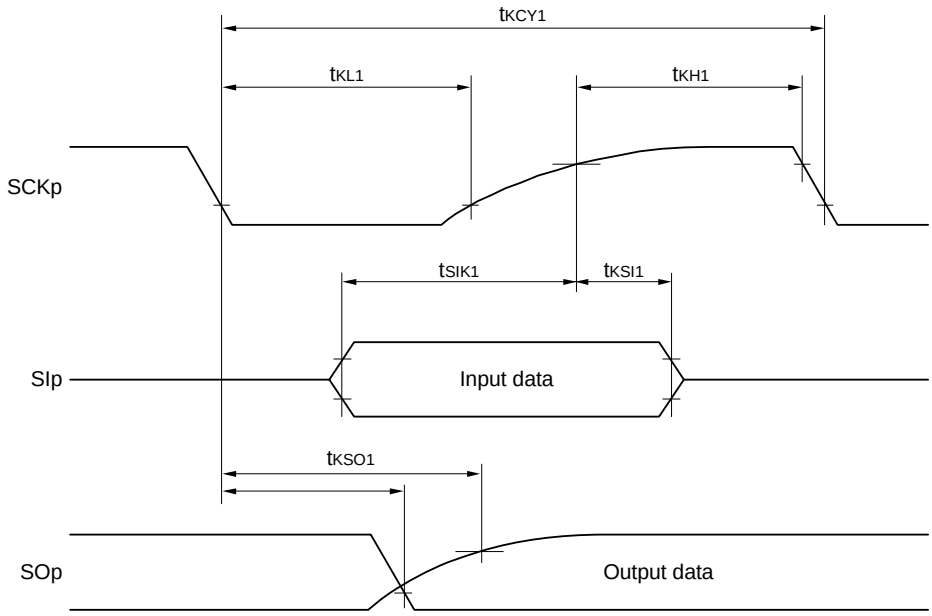
Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark 1. V_b [V]: Communication line voltage

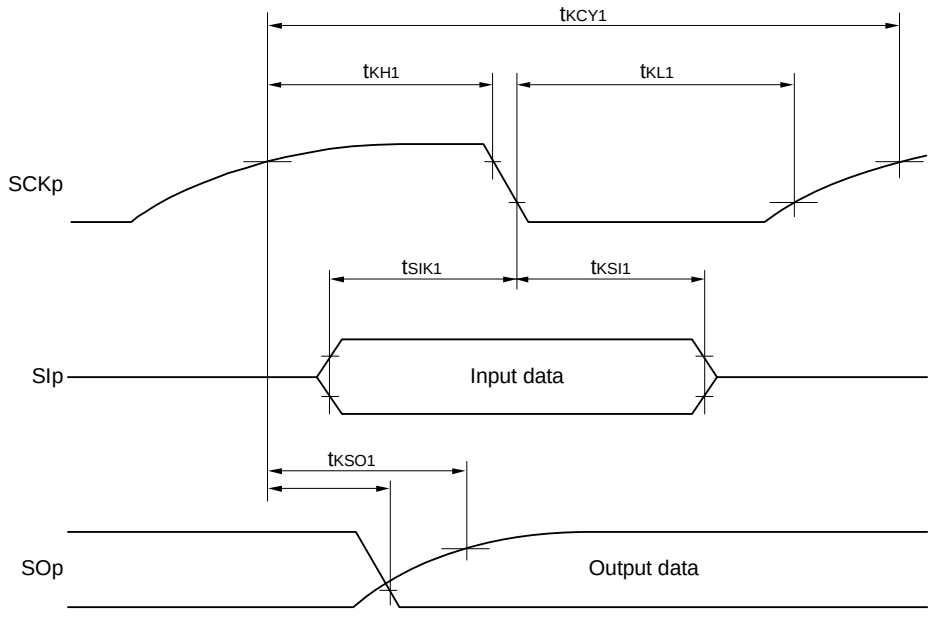
Remark 2. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

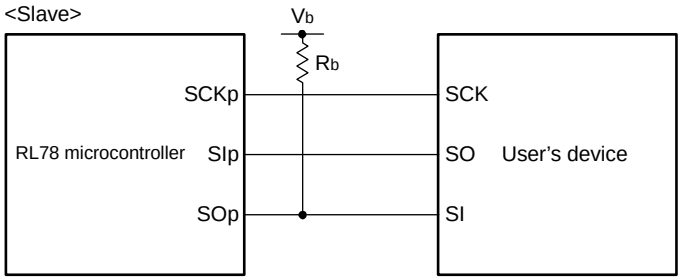
Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0 , 1), g: PIM or POM number (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

Remark 4. Communication at different potential cannot be performed during clocked serial communication with the slave select function.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/2)**

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			-0.5 to +6.5	V
	AV_{DD}	$AV_{DD} = V_{DD}$		-0.5 to +6.5	V
	AV_{SS}	$AV_{SS} = V_{SS}$		-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC		-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
REGA pin input voltage	V_{IREGA}	REGA		-0.3 to +2.8 and -0.3 to AV_{DD} + 0.3 Note 2	V
Input voltage	V_{I1}	P10 to P15, P40, P121, P122, P137, EXCLK, $\overline{\text{RESET}}$		-0.3 to V_{DD} +0.3 Note 3	V
Alternate-function pin input voltage	V_{I2}	P16, P17, P41, P42 (36-pin products only)	Digital input voltage	-0.3 to V_{DD} + 0.3 Note 3	V
			Analog input voltage	-0.3 to AV_{DD} + 0.3 Note 3	V
Analog input voltage	V_{IA}	PGA0P to PGA3P, PGA0N to PGA3N, ANI0 to ANI9, ANX0 to ANX5		-0.3 to AV_{DD} + 0.3 Note 3	V
Output voltage	V_{O1}	P10 to P15, P40		-0.3 to V_{DD} + 0.3 Note 3	V
Alternate-function pin output voltage	V_{O2}	P16, P17, P41, P42 (36-pin products only)	Digital output voltage	-0.3 to V_{DD} + 0.3 Note 3	V
			Analog output voltage	-0.3 to AV_{DD} + 0.3 Note 3	V
Analog output voltage	V_{OA}	SBIAS, AMP0O to AMP2O, ANX0 to ANX5		-0.3 to AV_{DD} + 0.3 Note 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Connect the REGA pin to AV_{SS} via a capacitor (0.22 μF). This value regulates the absolute maximum rating of the REGA pin. Do not use this pin with voltage applied to it.

Note 3. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. V_{SS} is used as the reference voltage.

3.2.3 PLL characteristics

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
PLL output frequency Notes 1, 2, 3	f_{PLL}	f_{MX} = 8 MHz	DSFRDIV = 0	DSCM = 0		48		MHz
			DSFRDIV = 1	DSCM = 0		24		MHz
				DSCM = 1		32		MHz
		f_{MX} = 4 MHz	DSFRDIV = 0	DSCM = 0		24		MHz
				DSCM = 1		32		MHz
Lockup wait time		Time from when PLL output is enabled to when the phase is locked			40			µs
Interval wait time		Time from when the PLL stops operating to when the setting to start PLL operation is specified			4			µs
Setup wait time		Time required from when the PLL input clock stabilizes and the PLL setting is determined to when the PLL is activated			1			µs

Note 1. When using a PLL, input a clock of 4 MHz or 8 MHz to the PLL.

Note 2. Be sure to specify one of these settings when using a PLL.

Note 3. When using the PLL output as the CPU clock, f_{IH} is divided by 2, 4, or 8 according to the setting of the RDIV1 and RDIV0 bits.

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	333		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	666		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 24		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 36		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 30 pF Note 3			66.6	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

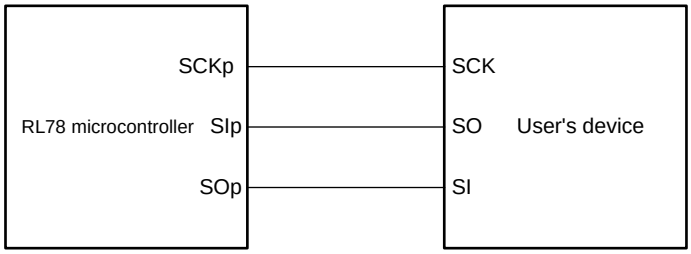
Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

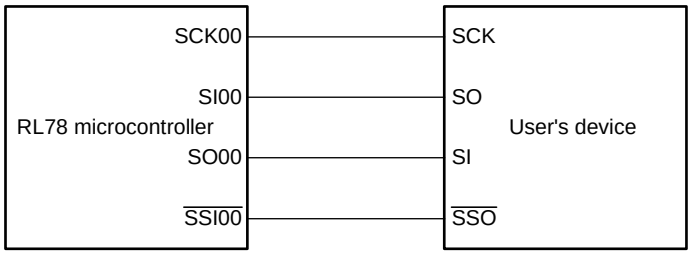
Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at same potential)

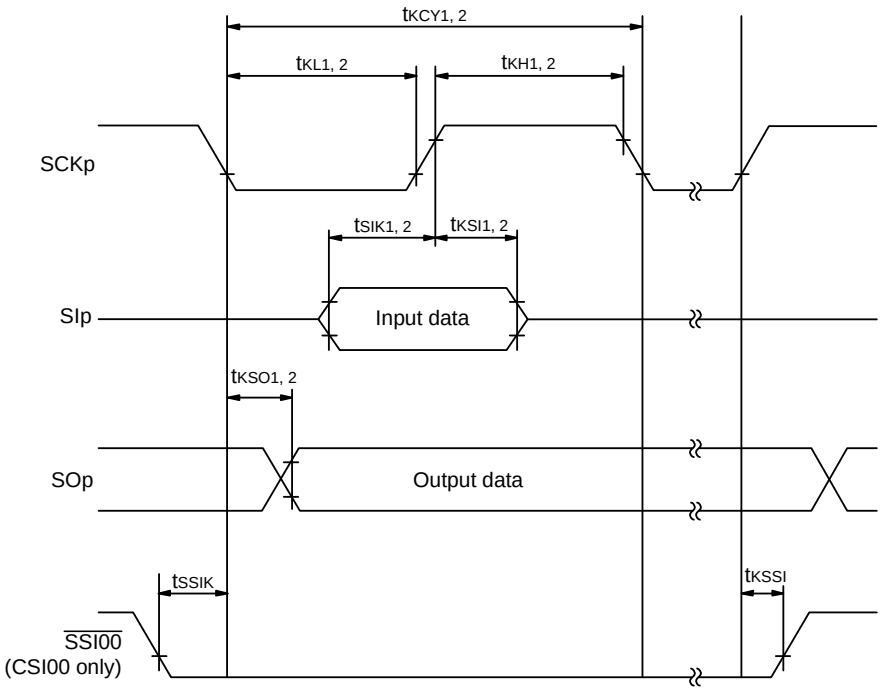


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

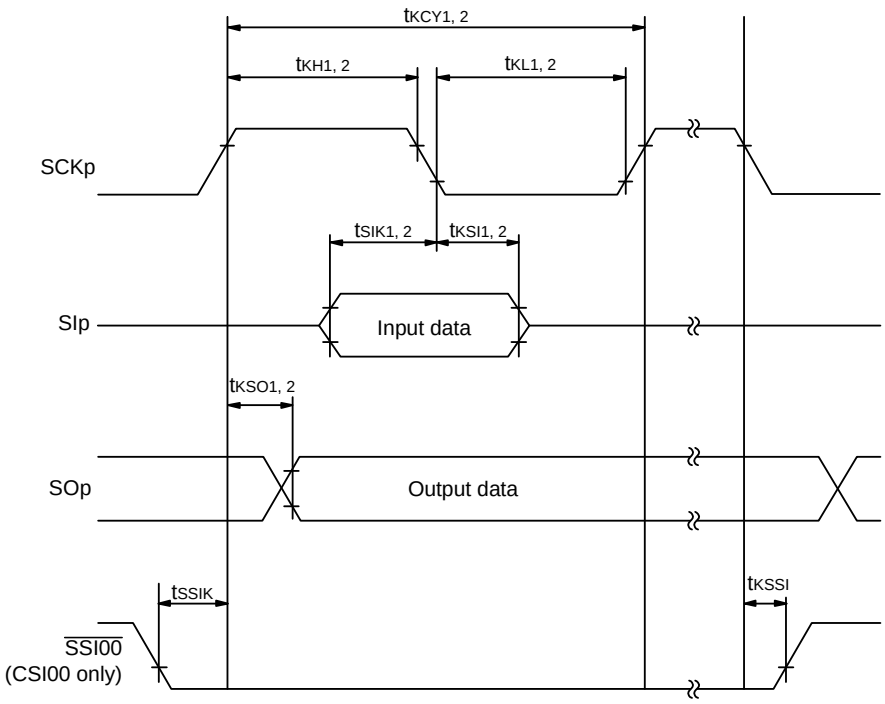


Remark 1. p: CSI number (p = 00, 01)
Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01)
Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		Note 1	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.0 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		Note 3	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		Note 5	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 6	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (3/3)

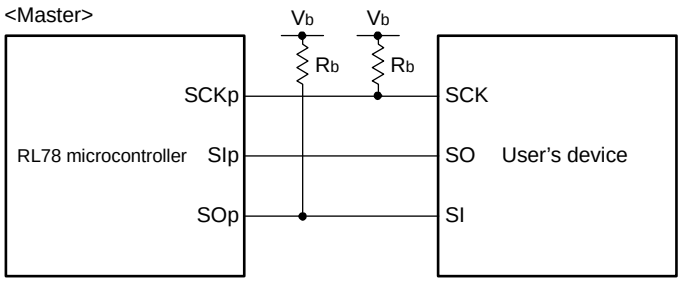
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↓) Note	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	88		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	220		ns
SIp hold time (from SCKp↓) Note	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output Note	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		50	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		50	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential

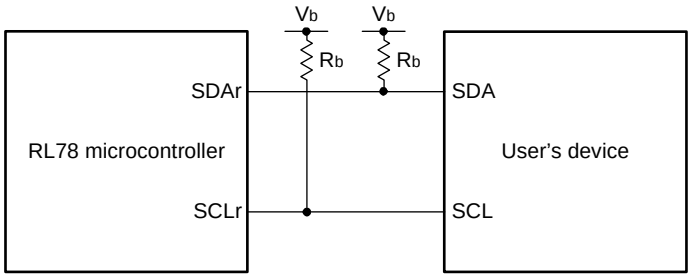


Remark 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

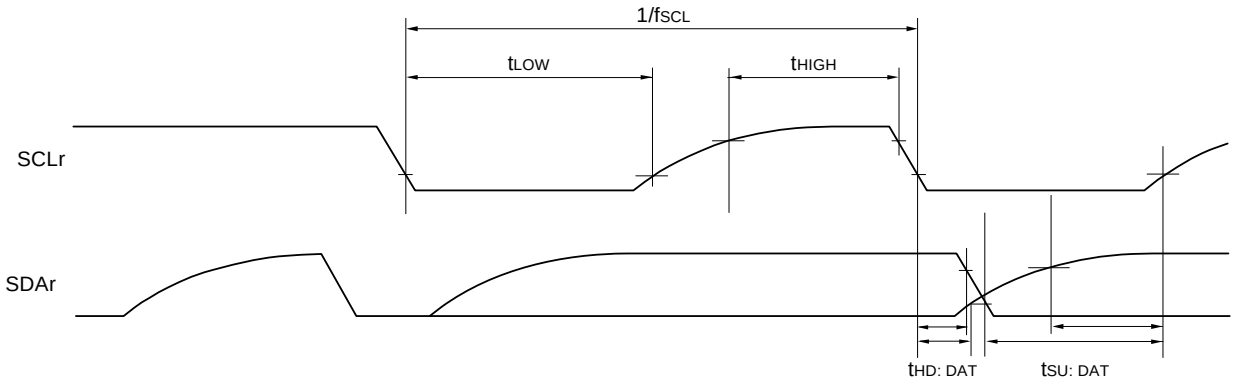
Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. Rb [Ω]: Communication line (SDAr, SCLr) pull-up resistance, Cb [F]: Communication line (SDAr, SCLr) load capacitance, Vb [V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01), g: PIM, POM number (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0), mn = 00, 01)

3.6.4 A/D converter characteristics

(1) When positive reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = AV_{DD}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V		1.2	±6.5	LSB
			2.7 V ≤ AV_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ AV_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ AV_{DD} ≤ 5.5 V	3.1875		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
			2.7 V ≤ AV_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI9		AV_{SS}		AV_{DD}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The number of pins depends on the product. For details, see a list of pin functions.

(2) When positive reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = V_{BGR}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.7 V ≤ AV_{DD} ≤ 5.5 V			±1.0	LSB
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ AV_{DD} ≤ 5.5 V		V_{BGR} Note 3			V
Analog input voltage	V_{AIN}	ANI0 to ANI9		0		V_{BGR}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. See the Internal reference voltage characteristics.