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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 10x10b, 4x24b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	36-TFBGA
Supplier Device Package	36-TFBGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11cccgbg-u0

1.6 Outline of Functions

[32-pin, 36-pin products]

(1/2)

Item		32-pin	36-pin
		R5F11CBC	R5F11CCC
Code flash memory		32 KB	
Data flash memory		4 KB	
RAM		8 KB	
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 16 MHz: V_{DD} = 2.4 to 2.7 V	
	High-speed on-chip oscillator clock (f_{IH})	1 to 32 MHz (V_{DD} = 2.7 to 5.5 V)Note 1 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V)	
	PLL clock (f_{PLL} divided by 2, 4, or 8)	3 to 32 MHz (V_{DD} = 2.7 to 5.5 V)Note 2 3 to 16 MHz (V_{DD} = 2.4 to 5.5 V)	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (high-speed on-chip oscillator clock: f_{IH} = 32 MHz operation)Note 3	
		0.03125 μs (PLL clock: f_{PLL} = 64 MHz, f_{IH} = 32 MHz operation)Note 4	
		0.05 μs (high-speed system clock: f_{MX} = 20 MHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	10	14
	CMOS I/O	7	11
	CMOS input	3	3
Timer	16-bit timer	8 channels (TAU: 6 channels, Timer RJ: 1 channel, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	Interval timer	1 channel	
	Timer output	Timer outputs: 10 channels PWM outputs: 9 channels	
	RTC output	1	
Clock output/buzzer output		1	
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)	
8/10-bit A/D converter		8 channels	10 channels
Serial interface		CSI: 2 channels/UART: 2 channels (UART supporting LIN-bus: 1 channel)/simplified I^2C: 2 channels	

Note 1. 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V) for M products (industrial applications, T_A = –40 to +125°C)

Note 2. 3 to 24 MHz (V_{DD} = 2.7 to 5.5 V) for M products (industrial applications, T_A = –40 to +125°C)

Note 3. 0.04167 μs (high-speed on-chip oscillator clock: f_{IH} = 24 MHz operation) for M products (industrial applications, T_A = –40 to +125°C)

Note 4. 0.04167 μs (PLL clock: f_{PLL} = 64 MHz, f_{IH} = 24 MHz operation) for M products (industrial applications, T_A = –40 to +125°C

2. ELECTRICAL SPECIFICATIONS (G: T_A = -40 to +105°C)

This chapter describes the electrical specifications for the products “G: Industrial applications (T_A = -40 to +105°C)”.

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product.

Caution 3. Please contact Renesas Electronics sales office for derating of operation under T_A = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products “M: Industrial applications”. For details, refer to **2.1** to **2.10**.

2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		32	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		-40 to +105°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/3)**

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P10 to P17 and P40 to P42 Note 2	-40°C < T_A ≤ +85°C			-10.0 Note 3	mA
			85°C < T_A ≤ 105°C			-3.0 Note 3	mA
		Total of P10 to P17, P41, and P42 Note 2 (When duty ≤ 70% Note 4)	4.0 V ≤ V_{DD} ≤ 5.5 V -40°C < T_A ≤ +85°C			-80.0	mA
			4.0 V ≤ V_{DD} ≤ 5.5 V 85°C < T_A ≤ 105°C			-30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-19.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			-10.0	mA
Output current, low Note 1	I_{OL1}	Per pin for P10 to P17 and P40 to P42 Note 2	-40°C < T_A ≤ +85°C			20.0 Note 3	mA
			85°C < T_A ≤ 105°C			8.5 Note 3	mA
		Total of P10 to P17, P41, and P42 Note 2 (When duty ≤ 70% Note 4)	4.0 V ≤ V_{DD} ≤ 5.5 V -40°C < T_A ≤ +85°C			80.0	mA
			4.0 V ≤ V_{DD} ≤ 5.5 V 85°C < T_A ≤ 105°C			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			20.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. This indicates the total current value when P16, P17, P41, and P42 are used as digital I/O ports. When using these pins as analog function (AFE) pins, refer to **2.1 Absolute Maximum Ratings**.

Note 3. Do not exceed the total current value.

Note 4. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

  Example: n = 80% when I_{OH} = -10.0 mA
  Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution **P10 to P15 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode Note 2	f_{HOCO} = 32 MHz, f_{MAIN} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		mA
					V_{DD} = 3.0 V		2.1		
			f_{HOCO} = 32 MHz, f_{MAIN} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.8	8.7	mA
					V_{DD} = 3.0 V		4.8	8.7	
			f_{HOCO} = 24 MHz, f_{MAIN} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.8	6.7	
					V_{DD} = 3.0 V		3.8	6.7	
			f_{HOCO} = 16 MHz, f_{MAIN} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	4.9	
					V_{DD} = 3.0 V		2.8	4.9	
			f_{MX} = 20 MHz, f_{MAIN} = 20 MHz Note 4, V_{DD} = 5.0 V	Normal operation	Square wave input		3.3	5.7	mA
					Resonator connection		3.5	5.8	
			f_{MX} = 20 MHz, f_{MAIN} = 20 MHz Note 4, V_{DD} = 3.0 V	Normal operation	Square wave input		3.3	5.7	
					Resonator connection		3.5	5.8	
			f_{MX} = 10 MHz, f_{MAIN} = 10 MHz Note 4, V_{DD} = 5.0 V	Normal operation	Square wave input		2.0	3.4	
					Resonator connection		2.1	3.5	
			f_{MX} = 10 MHz, f_{MAIN} = 10 MHz Note 4, V_{DD} = 3.0 V	Normal operation	Square wave input		2.0	3.4	
					Resonator connection		2.1	3.5	
			f_{MX} = 8 MHz, f_{MAIN} = 32 MHz Note 5, V_{DD} = 5.0 V	Normal operation	Square wave input		5.2	9.2	mA
					Resonator connection		5.3	9.3	
			f_{MX} = 8 MHz, f_{MAIN} = 32 MHz Note 5, V_{DD} = 3.0 V	Normal operation	Square wave input		5.2	9.2	
					Resonator connection		5.3	9.3	
			f_{MX} = 8 MHz, f_{MAIN} = 24 MHz Note 5, V_{DD} = 5.0 V	Normal operation	Square wave input		5.1	9.1	
					Resonator connection		5.2	9.2	
			f_{MX} = 8 MHz, f_{MAIN} = 24 MHz Note 5, V_{DD} = 3.0 V	Normal operation	Square wave input		5.1	9.1	
					Resonator connection		5.2	9.2	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the RTC, interval timer, watchdog timer, LVD circuit, AFE, I/O ports, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. The relationship between the operation voltage range and the CPU operating frequency is as below.
2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz

Note 3. When the high-speed system clock is stopped

Note 4. When the high-speed on-chip oscillator and the PLL are stopped

Note 5. When the high-speed on-chip oscillator is stopped and the PLL is operating

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

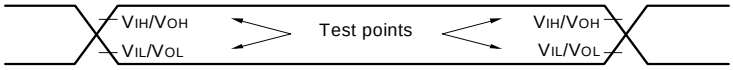
Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency

Remark 3. f_{MAIN}: Main system clock frequency

Remark 4. The temperature condition for the TYP. value is T_A = 25°C

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

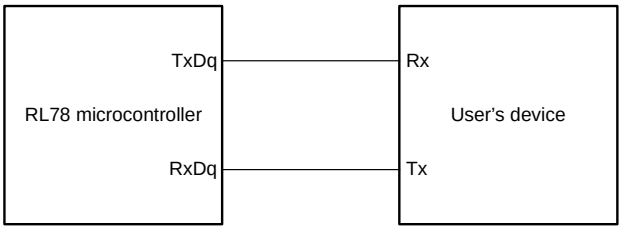
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1				f_{MCK}/12	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

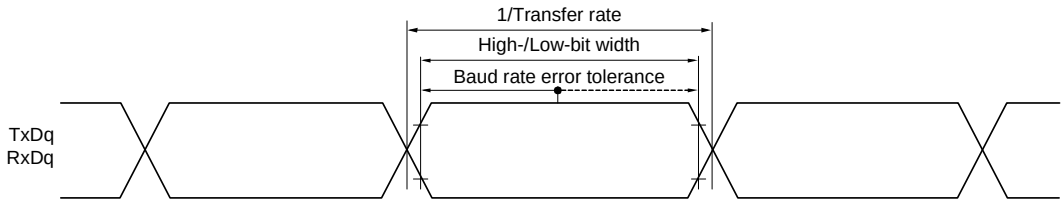
Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

Note 5. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 6. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/3)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) Note	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output Note	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

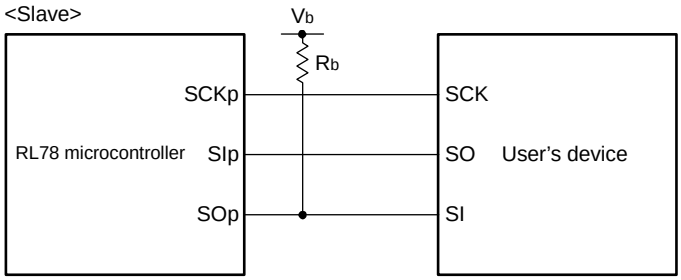
Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



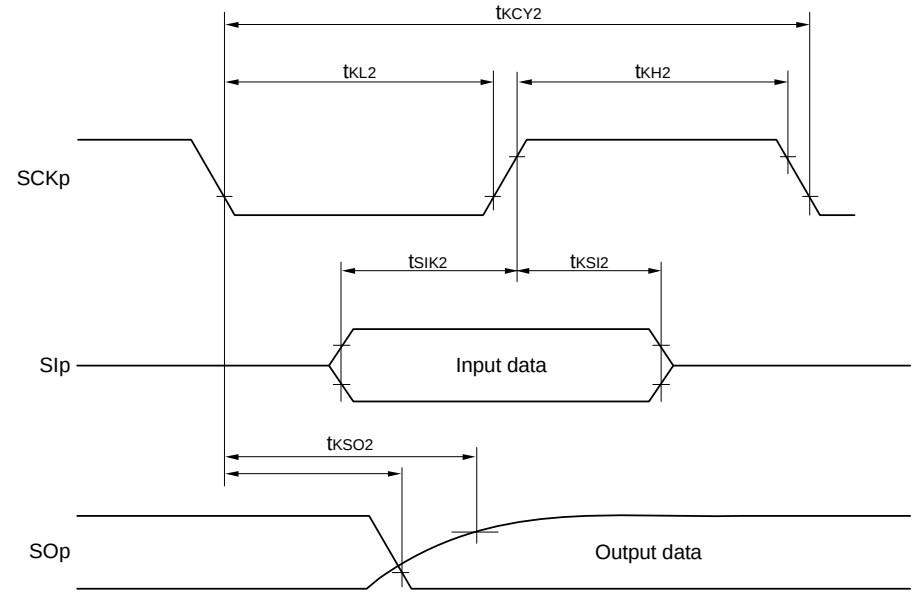
Remark 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0 , 1), g: PIM or POM number (g = 1)

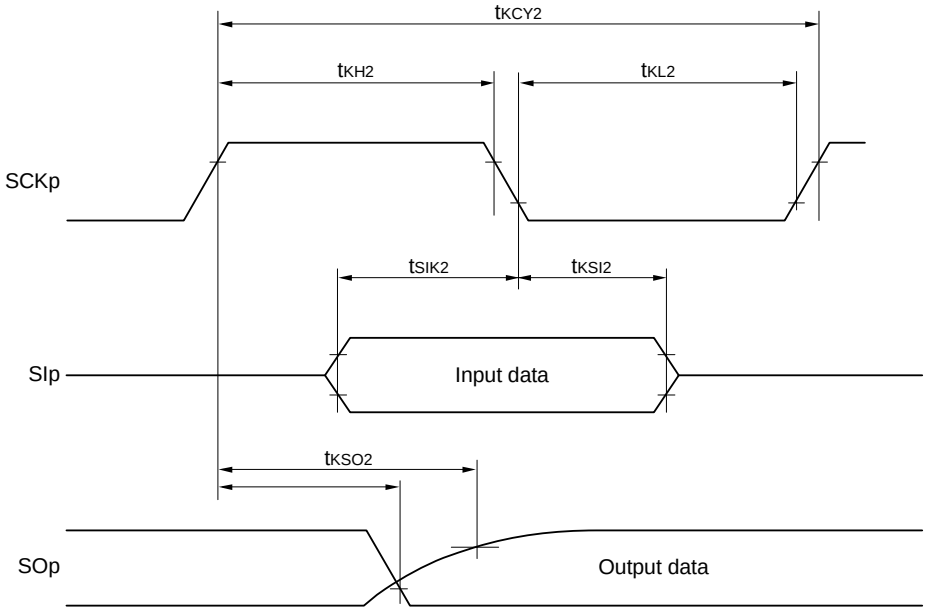
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

Remark 4. Communication at different potential cannot be performed during clocked serial communication with the slave select function.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

Remark 2. Communication at different potential cannot be performed during clocked serial communication with the slave select function.

2.6.8 LVD characteristics

(1) LVD detection voltage in reset mode and interrupt mode

(T_A = -40 to +105°C, $V_{PDR} \le AV_{DD} = V_{DD} \le$ 5.5 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD0}	Rising edge	4.62	4.74	4.84	V
			Falling edge	4.52	4.64	4.74	V
		V_{LVD1}	Rising edge	4.50	4.62	4.72	V
			Falling edge	4.40	4.52	4.62	V
		V_{LVD2}	Rising edge	4.30	4.42	4.51	V
			Falling edge	4.21	4.32	4.41	V
		V_{LVD3}	Rising edge	3.13	3.22	3.29	V
			Falling edge	3.07	3.15	3.22	V
		V_{LVD4}	Rising edge	2.95	3.02	3.09	V
			Falling edge	2.89	2.96	3.02	V
		V_{LVD5}	Rising edge	2.74	2.81	2.87	V
			Falling edge	2.68	2.75	2.81	V
		V_{LVD6}	Rising edge	2.55	2.61	2.67	V
			Falling edge	2.49	2.55	2.61	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

(2) LVD detection voltage in interrupt & reset mode

(T_A = -40 to +105°C, $V_{PDR} \le AV_{DD} = V_{DD} \le$ 5.5 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	V_{LVDD6}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage		2.49	2.55	2.61	V
	V_{LVDD4}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.09	V
			Falling interrupt voltage	2.89	2.96	3.02	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.13	3.22	3.29	V
			Falling interrupt voltage	3.07	3.15	3.22	V
	V_{LVDD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage		2.68	2.75	2.81	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.51	V
			Falling interrupt voltage	4.21	4.32	4.41	V
	V_{LVDD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage		2.68	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.72	V
			Falling interrupt voltage	4.40	4.52	4.62	V
	V_{LVDD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage		2.68	2.75	2.81	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.29	V
			Falling interrupt voltage	3.07	3.15	3.22	V
	V_{LVDD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.84	V
			Falling interrupt voltage	4.52	4.64	4.74	V

2.6.9 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				50	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

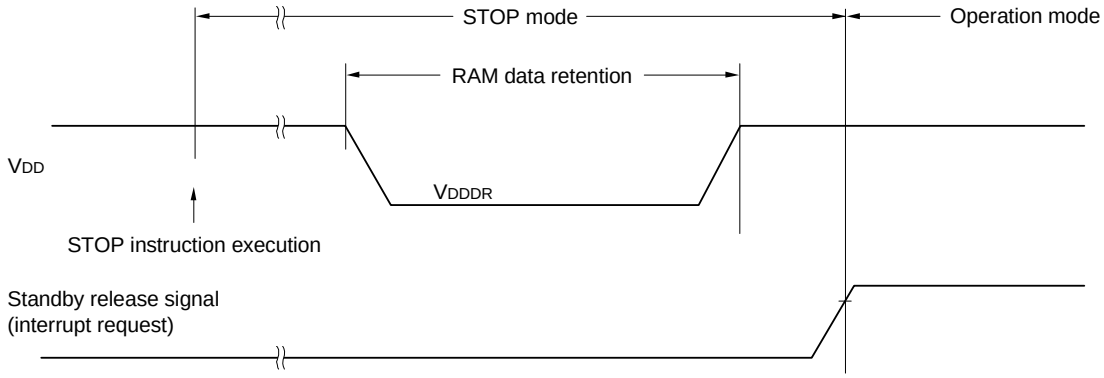
<R> 2.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 Notes 1, 2		5.5	V

Note 1. The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Note 2. Enter STOP mode before the supply voltage falls below the recommended operating voltage.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 5.5 V	1		32	MHz
<R> Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C Note 4	1,000			Times
<R> Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T_A = 25°C Note 4		1,000,000		
		Retained for 5 years T_A = 85°C Note 4	100,000			
		Retained for 20 years T_A = 85°C Note 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> **Note 4.** This temperature is the average value at which data are retained.

3.2 Oscillator Characteristics

3.2.1 X1 characteristics

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/I1E User's Manual..

3.2.2 On-chip oscillator characteristics

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V	1		24	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		-40 to +105°C	-2.0		+2.0	%
<R>		+105 to +125°C	-3.0		+3.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(3/3)**

Item	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P10 to P17, and P40 to P42	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121, P122 (X1, X2, EXCLK)	$V_I = V_{DD}$	In input port mode or when using external clock input			1	μA
				When a resonator is connected			10	μA
Input leakage current, low	I_{LIL1}	P10 to P17, and P40 to P42	$V_I = V_{SS}$				-1	μA
	I_{LIL2}	P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				-1	μA
	I_{LIL3}	P121, P122 (X1, X2, EXCLK)	$V_I = V_{SS}$	In input port mode or when using external clock input			-1	μA
				When a resonator is connected			-10	μA
On-chip pull-up resistance	R_U	P10 to P15, P40	$V_I = V_{SS}$, in input port mode		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.4 AC Characteristics

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	µs
			2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
		In the self-programming mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	µs
			2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1.0		8.0	MHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V		24			ns
		2.4 V ≤ V_{DD} < 2.7 V		60			ns
TI00 to TI03, TI10, TI11 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK} + 10			ns
Timer RJ input cycle	f_C	TRJIO0	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
			2.4 V ≤ V_{DD} < 2.7 V	300			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO0	2.7 V ≤ V_{DD} ≤ 5.5 V	40			ns
			2.4 V ≤ V_{DD} < 2.7 V	120			ns
Timer RG input high-level width, low-level width	t_{TGIH}, t_{TGIL}	TRGIOA, TRGIOB		2.5/f_{CLK}			ns
TO00 to TO03, TO10, TO11, TRJIO0, TRJO0, TRGIOA, TRGIOB output frequency	f_{TO}		4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
			2.7 V ≤ V_{DD} ≤ 4.0 V			6	MHz
			2.4 V ≤ V_{DD} < 2.7 V			3	MHz
PCLBUZ0 output frequency	f_{PCL}		4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
			2.7 V ≤ V_{DD} ≤ 4.0 V			6	MHz
			2.4 V ≤ V_{DD} < 2.7 V			3	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP1 to INTP7		1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +125°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		12/f_{MCK} and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 66	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 113	ns
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	400		ns

Note 1. The maximum transfer rate in the SNOOZE mode is 1 Mbps.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

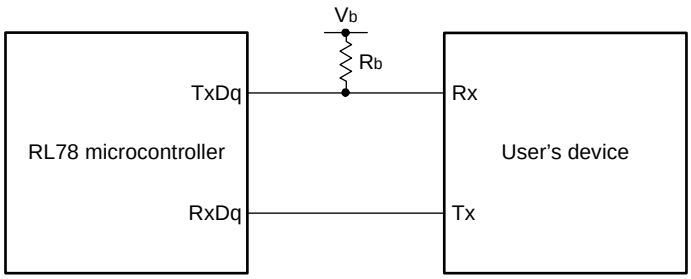
Note 4. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

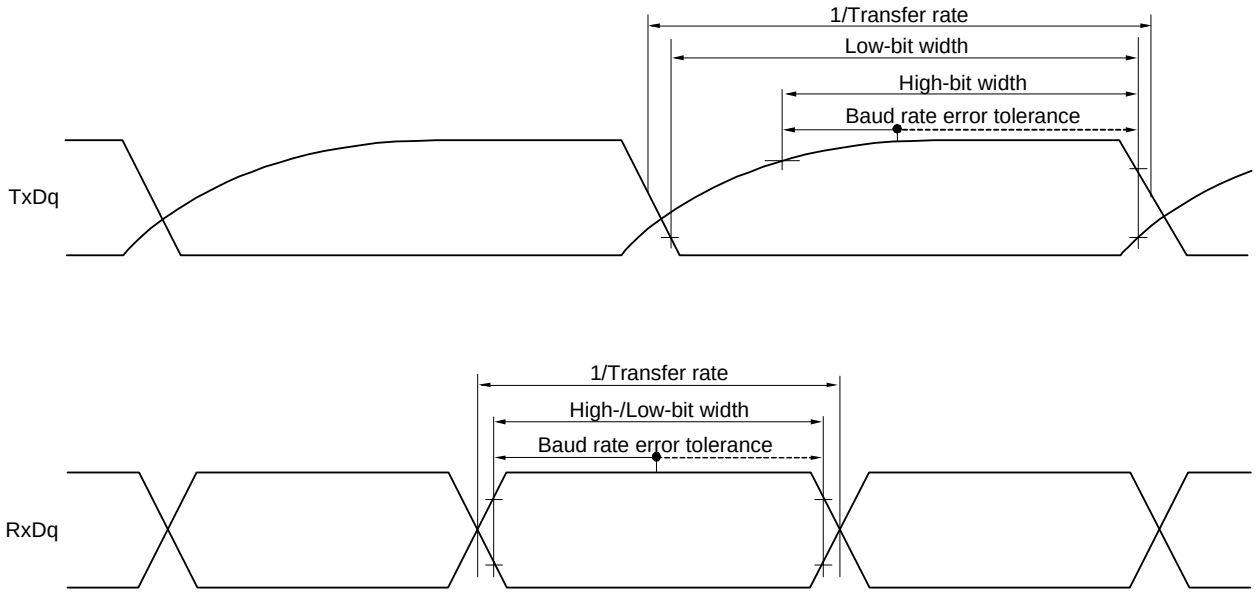
Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. Rb [Ω]: Communication line (TxDq) pull-up resistance,
Cb [F]: Communication line (TxDq) load capacitance, Vb [V]: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

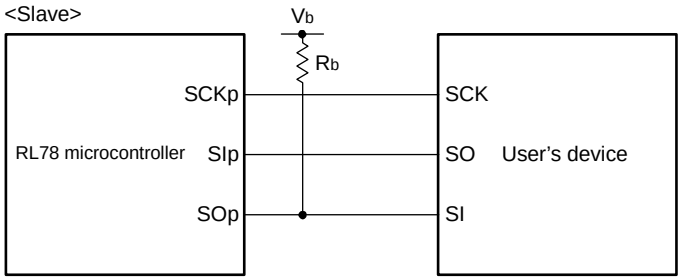
Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0 , 1), g: PIM or POM number (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

Remark 4. Communication at different potential cannot be performed during clocked serial communication with the slave select function.

3.6.6 Configurable amplifier

(T_A = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, V_{COM} = 1/2 AV_{DD}, internally connected voltage follower)

AMP0 configuration SW setting: Positive (+) pin = ANX1, negative (-) pin = ANX0

AMP1 configuration SW setting: Positive (+) pin = ANX3, negative (-) pin = ANX2

AMP2 configuration SW setting: Positive (+) pin = ANX5, negative (-) pin = ANX4

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	V_{IN}		AV_{SS}		AV_{DD}	V
Output voltage	V_{OL}	I_L= -1 mA, AV_{DD} = 2.7 to 5.5 V		AV_{SS} +0.02	AV_{SS} +0.07	V
	V_{OH}	I_L= 1 mA, AV_{DD} = 2.7 to 5.5 V	AV_{DD} -0.15	AV_{DD} -0.02		V
Maximum output current	I_{OUT}	4.5 V ≤ AV_{DD} ≤ 5.5 V	±10			mA
		2.7 V ≤ AV_{DD} ≤ 5.5 V	±5			mA
Input-referred offset voltage	V_{OFF}	T_A = 25°C without trimming I_L = 0 mA, V_{COM} = 1.0 V		±1	±4	mV
		T_A = 25°C with trimming I_L = 0 mA, V_{COM} = 1.0 V			±0.35	mV
Temperature coefficient for inputreferred offset voltage	V_{OTC}	I_L = 0 mA		(±2)	(±8)	µV/°C
Slew rate	SR1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(0.1)		V/µs
	SR2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(0.8)		V/µs
Gain bandwidth	GBW1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(350)		kHz
	GBW2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(1.8)		MHz
Phase margin	θM1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(70)		deg
	θM2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(60)		deg
Settling time	tset1	Normal mode C_L = 50 pF, R_L = 10 kΩ		(20)		µs
	tset2	High-speed mode C_L = 50 pF, R_L = 10 kΩ		(10)		µs
Peak-to-peak voltage noise	Enb	0.1 to 10 Hz Normal mode C_L = 50 pF, R_L = 10 kΩ		(2.0)		µVrms
Input-referred noise	En	f = 1 kHz Normal mode C_L = 50 pF, R_L = 10 kΩ		(70)		nV/√Hz
Common mode rejection ratio	CMRR	f = 1 KHz, C_L = 50 pF, R_L = 10 kΩ		(70)		dB
Power supply rejection ratio	PSRR	2.7 V ≤ AV_{DD} ≤ 5.5 V C_L = 50 pF, R_L = 10 kΩ		(62)		dB

(Remarks are listed on the next page.)

3.9 Dedicated Flash Memory Programmer Communication (UART)

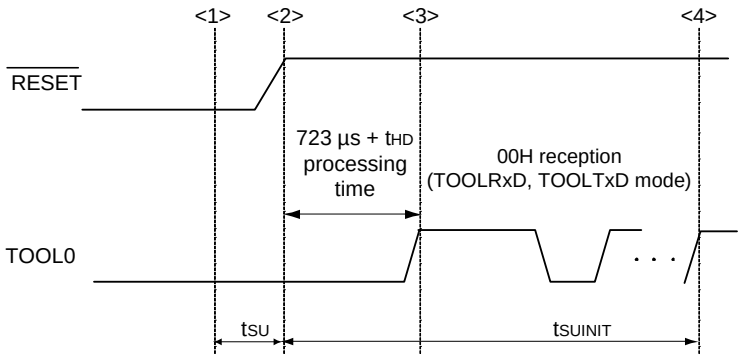
(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing for Switching Flash Memory Programming Modes

(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)