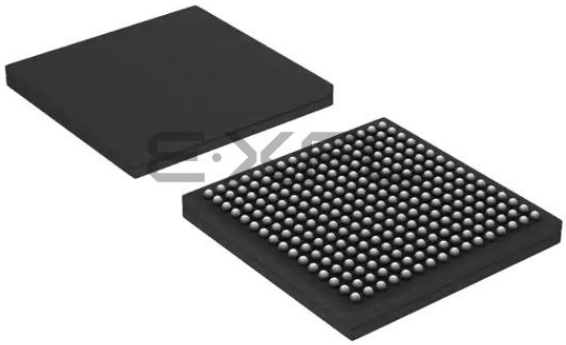

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc9328mx1dvm20

- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

2 Signals and Connections

Table 2 identifies and describes the i.MX1 processor signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

Table 2. i.MX1 Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip-Select (EIM)	
A[24:0]	Address bus signals
D[31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24].
$\overline{EB1}$	Byte Strobe—Active low external enable byte signal that controls D [23:16].
$\overline{EB2}$	Byte Strobe—Active low external enable byte signal that controls D [15:8].
$\overline{EB3}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0].
$\overline{OE}$	Memory Output Enable—Active low output enables external data bus.
$\overline{CS}$ [5:0]	Chip-Select—The chip-select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default $\overline{CSD}$ [1:0] is selected.
$\overline{ECB}$	Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
$\overline{LBA}$	Active low signal sent by a flash device causing the external burst device to latch the starting burst address.
BCLK (burst clock)	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
$\overline{RW}$	$\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a $\overline{WE}$ input signal by external DRAM.
$\overline{DTACK}$	$\overline{DTACK}$ signal—The external input data acknowledge signal. When using the external DTACK signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external DTACK signal after 1022 clock counts have elapsed.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode of the i.MX1 processor upon system reset is determined by the settings of these pins.
SDRAM Controller	
SDBA [4:0]	SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles.

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SIM_TX	Transmit Data
SIM_PD	Presence Detect Schmitt trigger input
SIM_SVEN	SIM Vdd Enable
SPI 1 and SPI 2	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_$\overline{SS}$	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_$\overline{SPI_RDY}$	Serial Data Ready
SPI2_TXD	SPI2 Master TxData Output—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_RXD	SPI2 Master RxData Input—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_$\overline{SS}$	SPI2 Slave Select—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_SCLK	SPI2 Serial Clock—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
$\overline{USBD\_ROE}$	USB $\overline{OE}$
USBD_AFE	USB Analog Front End Enable
Secure Digital Interface	
SD_CMD	SD Command—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added.

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_CLK	MMC Output Clock
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2\_RTS}}$	Request to Send
$\overline{\text{UART2\_CTS}}$	Clear to Send
$\overline{\text{UART2\_DSR}}$	Data Set Ready
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
UART3_RXD	Receive Data
UART3_TXD	Transmit Data
$\overline{\text{UART3\_RTS}}$	Request to Send
$\overline{\text{UART3\_CTS}}$	Clear to Send
$\overline{\text{UART3\_DSR}}$	Data Set Ready
$\overline{\text{UART3\_RI}}$	Ring Indicator
$\overline{\text{UART3\_DCD}}$	Data Carrier Detect
$\overline{\text{UART3\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	G5	D21	I/O	69K								Pull-H	
NVDD1	H1	A13	O									L	
NVDD1	H4	D20	I/O	69K								Pull-H	
	T1	VSS	Static										
QVDD1	H9	QVDD1	Static										
	H8	VSS	Static										
NVDD1	J5	NVDD1	Static										
NVDD1	J1	A12	O									L	
NVDD1	J4	D19	I/O	69K								Pull-H	
NVDD1	J2	A11	O									L	
NVDD1	J3	D18	I/O	69K								Pull-H	
NVDD1	K1	A10	O									L	
NVDD1	K4	D17	I/O	69K								Pull-H	
NVDD1	K3	A9	O									L	
NVDD1	K2	D16	I/O	69K								Pull-H	
NVDD1	L1	A8	O									L	
NVDD1	L4	D15	I/O	69K								Pull-H	
NVDD1	L2	A7	O									L	
NVDD1	L5	D14	I/O	69K								Pull-H	
	K6	VSS	Static										
NVDD1	K5	NVDD1	Static										
NVDD1	M4	A6	O									L	
NVDD1	L3	D13	I/O	69K								Pull-H	
NVDD1	M1	A5	O									L	
NVDD1	M2	D12	I/O	69K								Pull-H	

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD2	R14	$\overline{TDO}$	O									Hiz[5]	
NVDD2	N15	TMS	I	69K								Pull-H	
NVDD2	L9	TCK	I	69K								Pull-H	
NVDD2	N16	TDI	I	69K								Pull-H	
NVDD2	P14	I2C_SCL	O				PA16	69K				Pull-H	PA16
NVDD2	P15	I2C_SDA	I/O				PA15	69K				Pull-H	PA15
NVDD2	N13	CSI_PIXCLK	I				PA14	69K				Pull-H	PA14
NVDD2	M13	CSI_HSYNC	I				PA13	69K				Pull-H	PA13
NVDD2	M14	CSI_VSYNC	I				PA12	69K				Pull-H	PA12
NVDD2	N14	CSI_D7	I				PA11	69K				Pull-H	PA11
NVDD2	M15	CSI_D6	I				PA10	69K				Pull-H	PA10
NVDD2	M16	CSI_D5	I				PA9	69K				Pull-H	PA9
NVDD2	J10	VSS	Static										
NVDD2	M12	CSI_D4	I				PA8	69K				Pull-H	PA8
NVDD2	L16	CSI_D3	I				PA7	69K				Pull-H	PA7
NVDD2	L15	CSI_D2	I				PA6	69K				Pull-H	PA6
NVDD2	L14	CSI_D1	I				PA5	69K				Pull-H	PA5
NVDD2	L13	CSI_D0	I				PA4	69K				Pull-H	PA4
NVDD2	L12	CSI_MCLK	O				PA3	69K				Pull-H	PA3
NVDD2	L11	PWMO	O				PA2	69K				Pull-H	PA2
NVDD2	L10	TIN	I				PA1	69K			SPI2_RxD	Pull-H	PA1
NVDD2	K15	TMR2OUT	O				PD31	69K	SPI2_TxD			Pull-H	PD31
NVDD2	K16	LD15	O				PD30	69K				Pull-H	PD30
NVDD2	K14	LD14	O				PD29	69K				Pull-H	PD29
NVDD2	K13	LD13	O				PD28	69K				Pull-H	PD28

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD4	F6	SIM_RST	O		SSI_TXFS	I/O	PB18	69K				Pull-H	PB18
NVDD4	G6	SIM_RX	I		SSI_TXDAT	O	PB17	69K				Pull-H	PB17
NVDD4	B4	SIM_TX	I/O		SSI_RXDAT	I	PB16	69K				Pull-H	PB16
NVDD4	C4	SIM_PD	I		SSI_RXCLK	I/O	PB15	69K				Pull-H	PB15
NVDD4	D4	SIM_SVEN	O		SSI_RXFS	I/O	PB14	69K				Pull-H	PB14
NVDD4	B3	SD_CMD	I/O		MS_BS	O	PB13	69K				Pull-H	PB13
NVDD4	A3	SD_CLK	O		MS_SCLKO	O	PB12	69K				Pull-H	PB12
NVDD4	A2	SD_DAT3	I/O		MS_SDIO	I/O	PB11	69K (pull down)				Pull-L	PB11
NVDD4	E5	SD_DAT2	I/O		MS_SCLKI	I	PB10	69K				Pull-H	PB10
NVDD4	B2	SD_DAT1	I/O		MS_PI1	I	PB9	69K				Pull-H	PB9
NVDD4	C3	SD_DAT0	I/O		MS_PI0	I	PB8	69K				Pull-H	PB8

1 After reset, $\overline{CS0}$ goes H/L depends on BOOT[3:0].

2 Need external circuitry to drive the signal.

3 Need external pull-up.

4 External resistor is needed.

5 Need external pull-up or pull-down.

6 ASP signals are clamped by AVDD2 to prevent ESD (electrostatic discharge) damage. AVDD2 must be greater than QVDD to keep diodes reverse-biased.

3 Electrical Characteristics

This section contains the electrical specifications and timing diagrams for the i.MX1 processor.

3.1 Maximum Ratings

Table 4 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 5 on page 23 or the DC Characteristics table.

Table 4. Maximum Ratings

Symbol	Rating	Minimum	Maximum	Unit
NV_{DD}	DC I/O Supply Voltage	-0.3	3.3	V
QV_{DD}	DC Internal (core = 150 MHz) Supply Voltage	-0.3	1.9	V
QV_{DD}	DC Internal (core = 200 MHz) Supply Voltage	-0.3	2.0	V
AV_{DD}	DC Analog Supply Voltage	-0.3	3.3	V
$BTRFV_{DD}$	DC Bluetooth Supply Voltage	-0.3	3.3	V
VESD_HBM	ESD immunity with HBM (human body model)	–	2000	V
VESD_MM	ESD immunity with MM (machine model)	–	100	V
ILatchup	Latch-up immunity	–	200	mA
Test	Storage temperature	-55	150	°C
Pmax	Power Consumption	800[1]	1300[2]	mW

1 A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM® core-that is, 7x GPIO, 15x Data bus, and 8x Address bus.

2 A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core-that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at MHz, and where the whole image is running out of SDRAM. QVDD at V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 5 provides the recommended operating ranges for the supply voltages and temperatures. The i.MX1 processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

BTRFVDD is the supply voltage for the Bluetooth interface signals. It is quite sensitive to the data transmit/receive accuracy. Please refer to Bluetooth RF spec for special handling. If Bluetooth is not used

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns
4a	Output hold time	2.28	–	2	–	ns
4b	Output setup time	3.42	–	3	–	ns

4.2 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 10. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
DPLL input clock freq range	Vcc = 1.8V	5	–	100	MHz
Pre-divider output clock freq range	Vcc = 1.8V	5	–	30	MHz
DPLL output clock freq range	Vcc = 1.8V	80	–	220	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Pre-multiplier lock-in time	–	–	–	312.5	µsec
Freq lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	250	280 (56 µs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	250 (50 µs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	300	350 (70 µs)	400	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	270	320 (64 µs)	370	T_{ref}
Freq jitter (p-p)	–	–	0.005 (0.01%)	0.01	$2 \bullet T_{dck}$

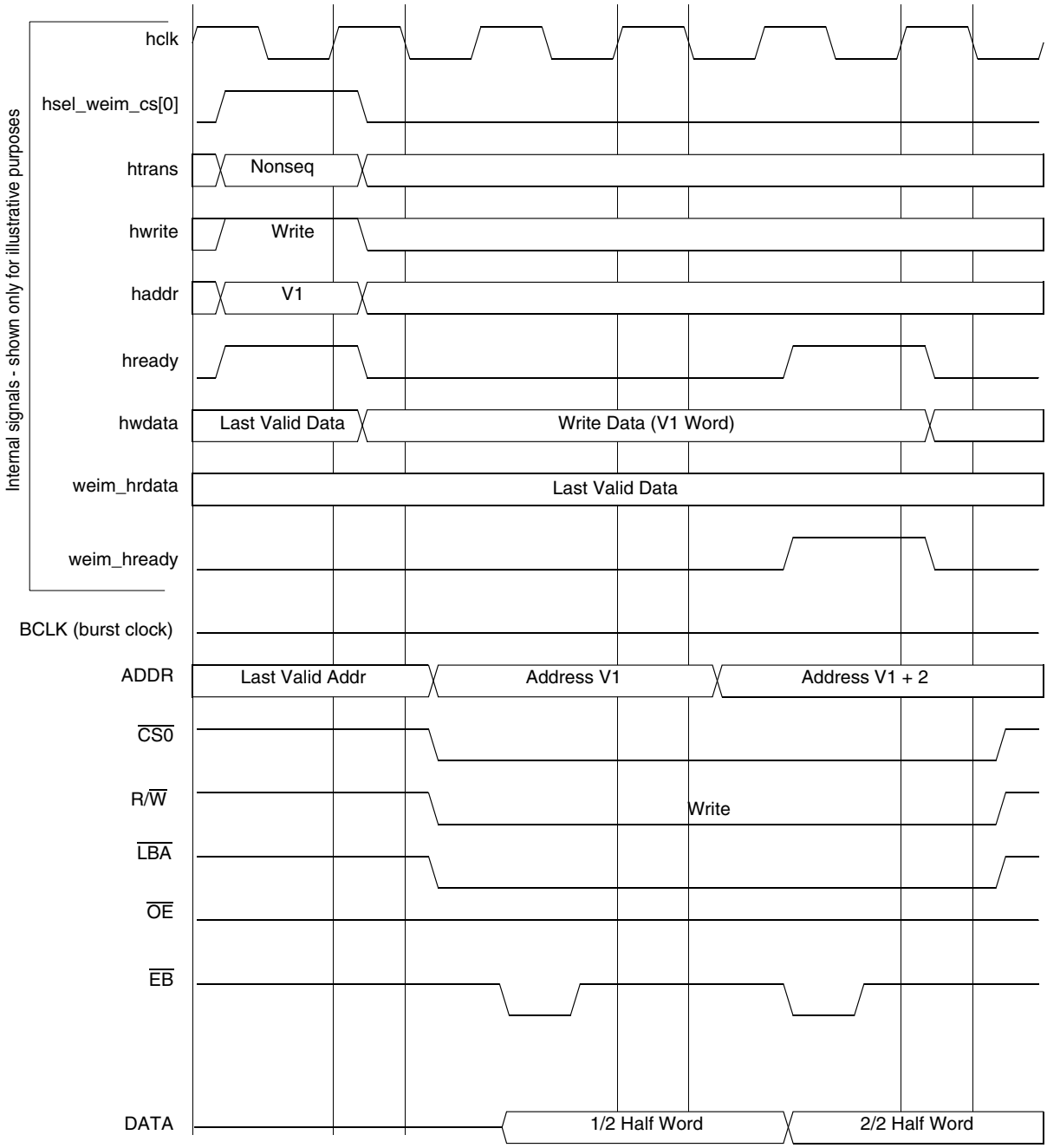
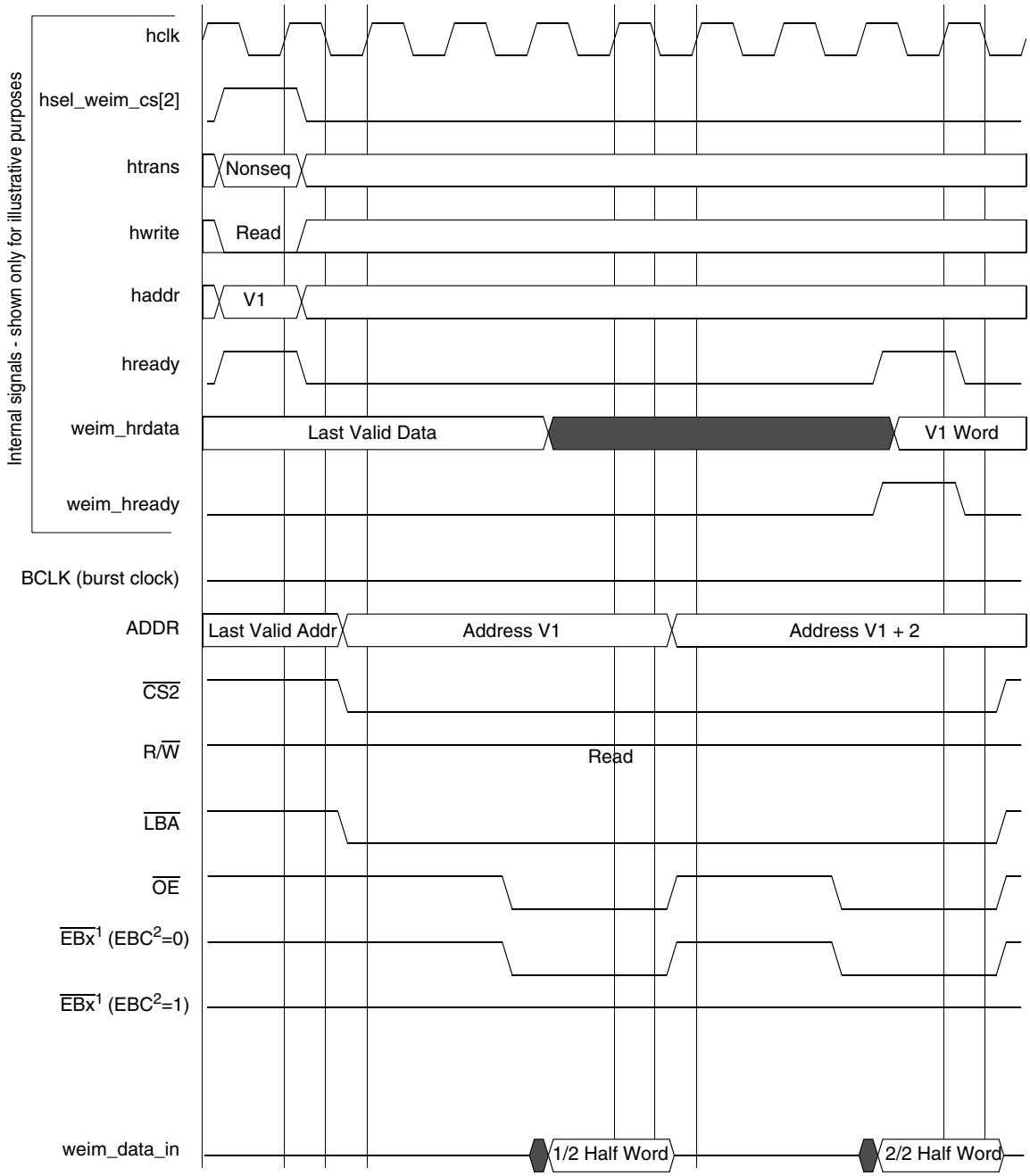


Figure 13. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 16. WSC = 3, OEA = 4, A.WORD/E.HALF

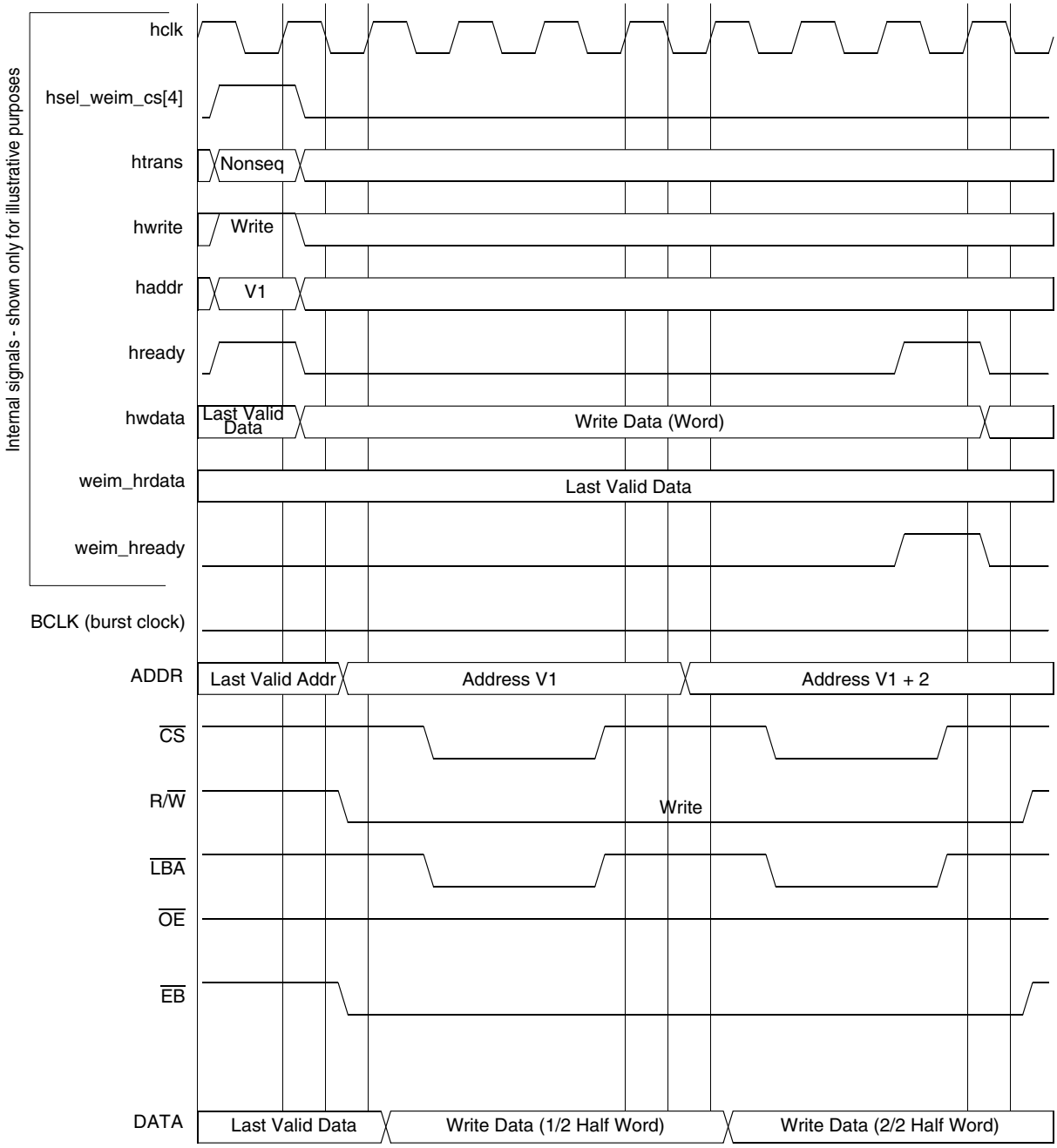
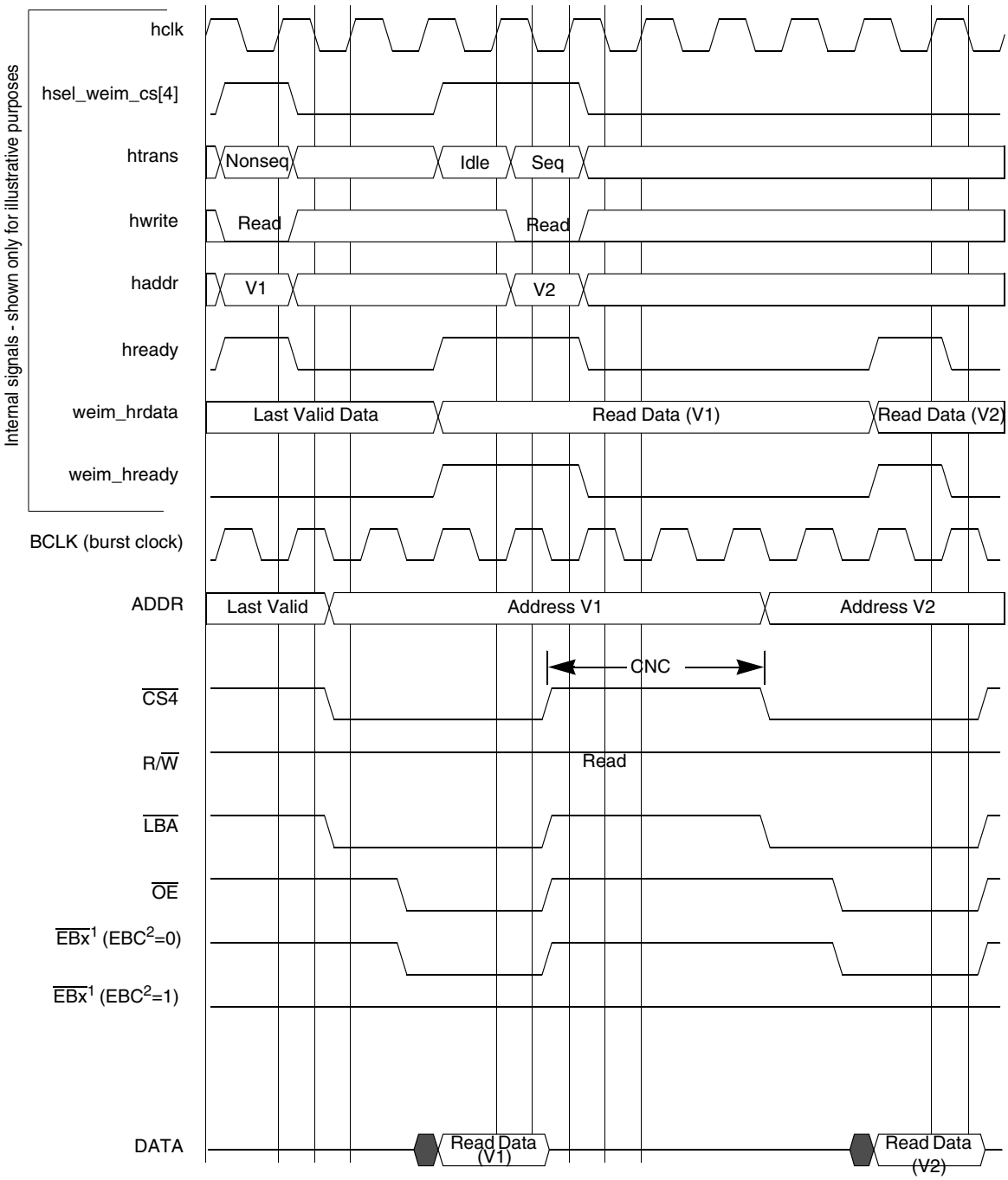
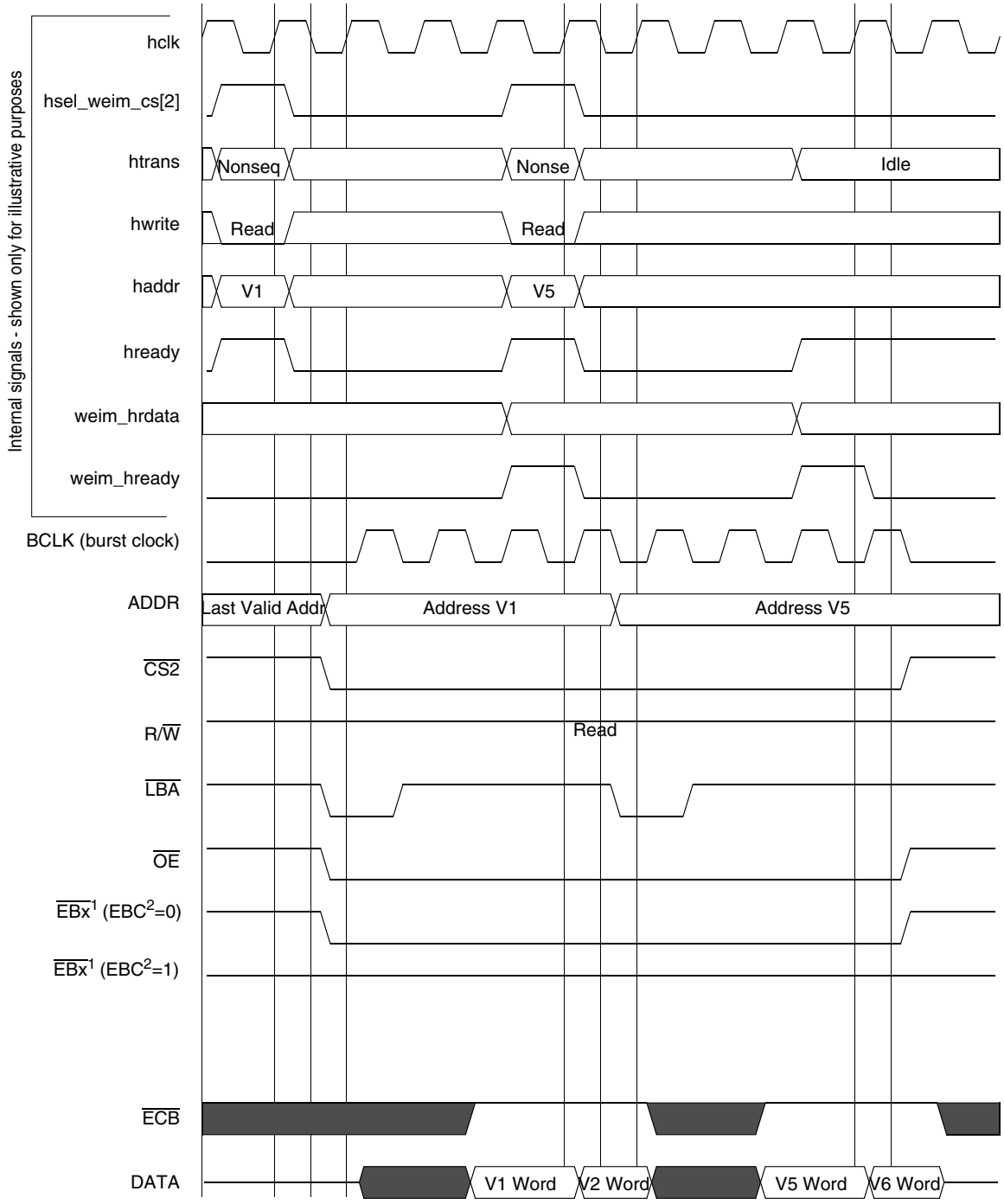


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



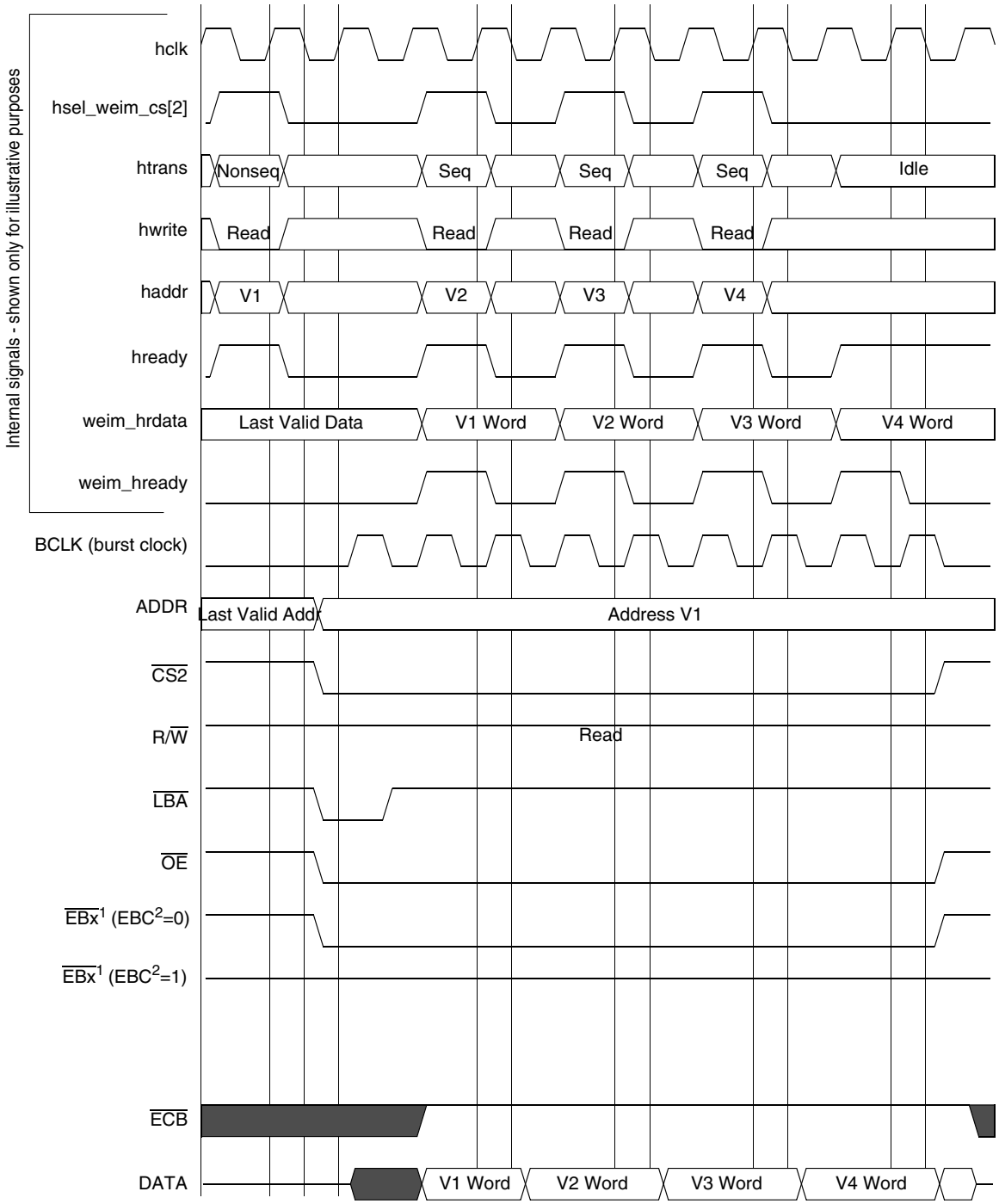
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 28. WSC = 3, SYNC = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 29. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

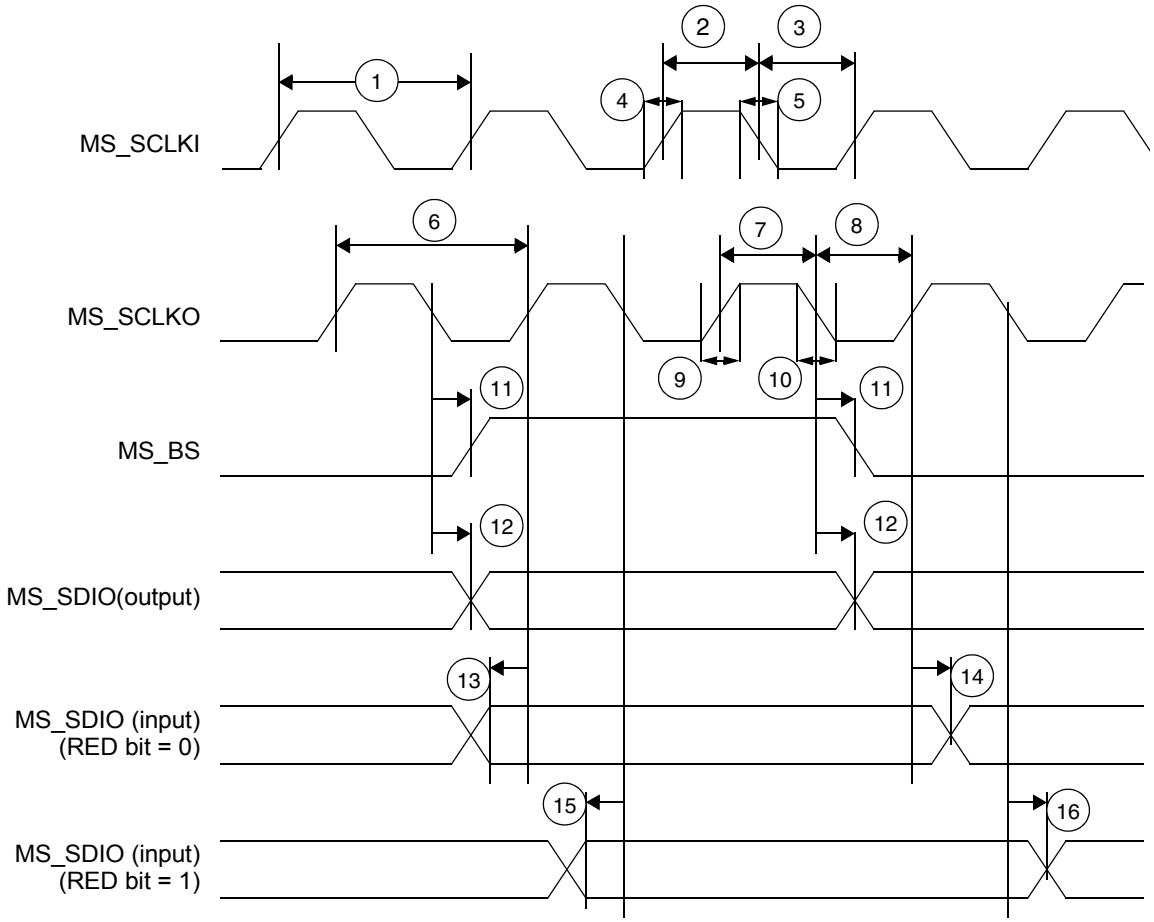


Figure 55. MSHC Signal Timing Diagram

Table 31. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	–	25	MHz
2	MS_SCLKI high pulse width	20	–	ns
3	MS_SCLKI low pulse width	20	–	ns
4	MS_SCLKI rise time	–	3	ns
5	MS_SCLKI fall time	–	3	ns
6	MS_SCLKO frequency[1]	–	25	MHz
7	MS_SCLKO high pulse width[1]	20	–	ns
8	MS_SCLKO low pulse width[1]	15	–	ns
9	MS_SCLKO rise time[1]	–	5	ns
10	MS_SCLKO fall time[1]	–	5	ns
11	MS_BS delay time[1]	–	3	ns

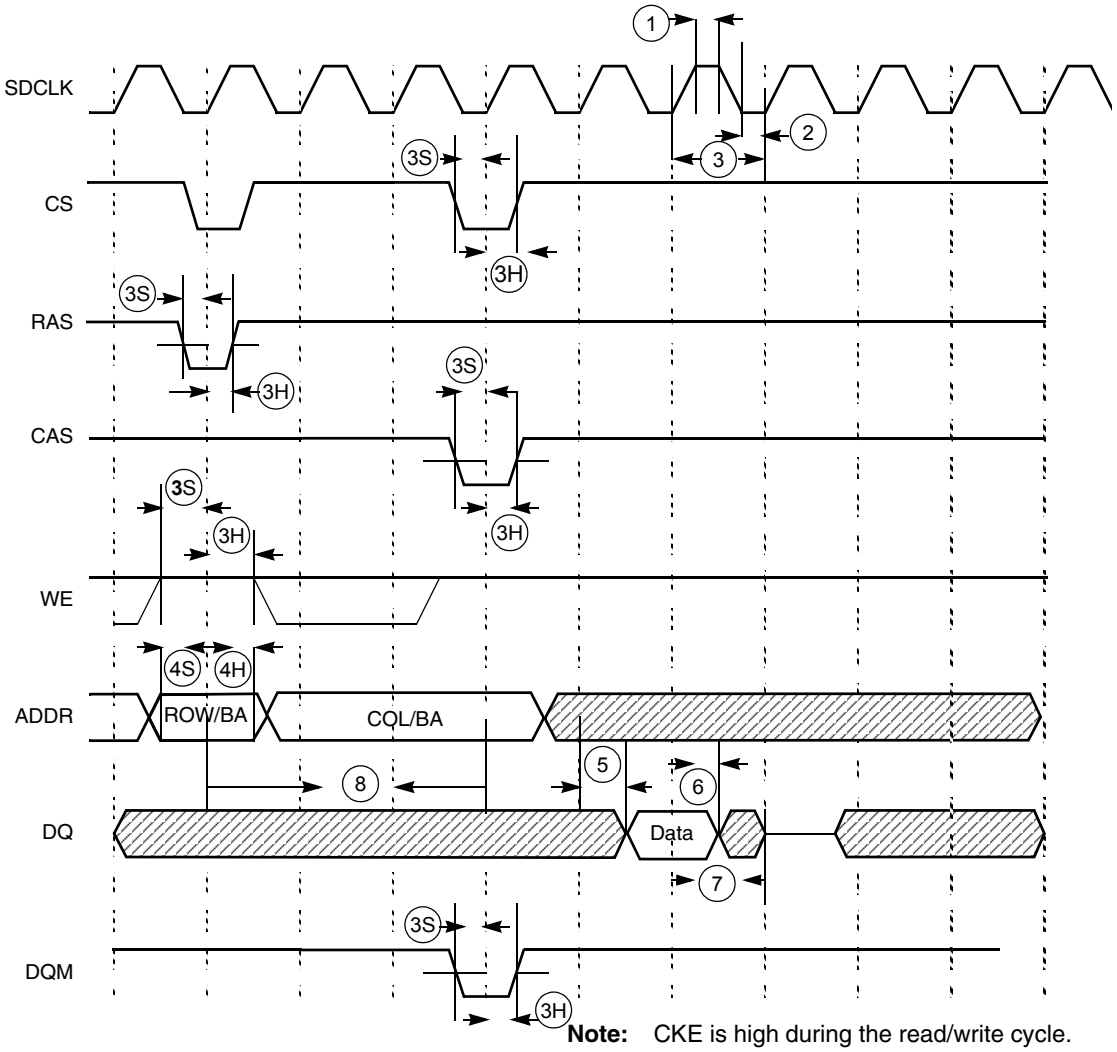
Table 32. PWM Output Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
3b	Clock rise time[1]	–	6.67	–	5/10	ns
4a	Output delay time[1]	5.7	–	5	–	ns
4b	Output setup time[1]	5.7	–	5	–	ns

[1] C_L of PWMO = 30 pF

4.13 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.



Note: CKE is high during the read/write cycle.

Figure 57. SDRAM Read Cycle Timing Diagram

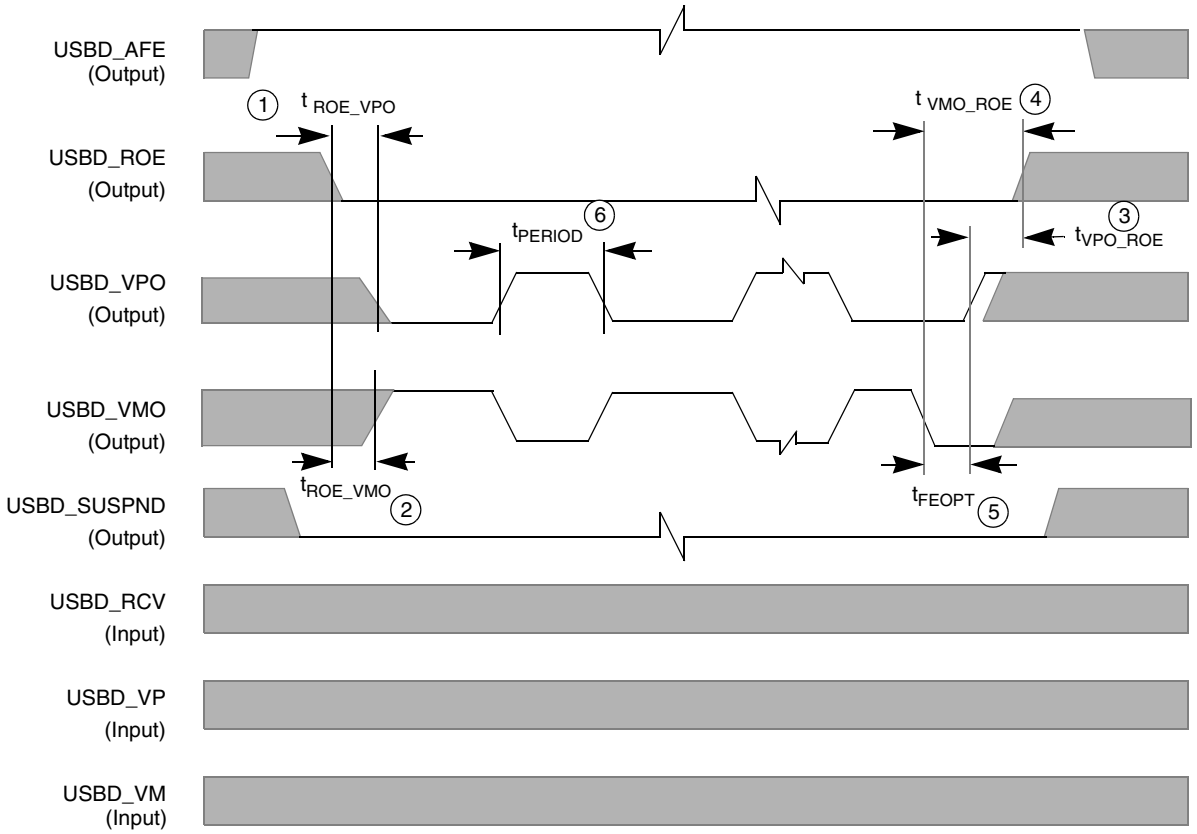


Figure 61. USB Device Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 36. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{ROE_VPO}; USBD_ROE active to USBD_VPO low	83.14	83.47	ns
2	t_{ROE_VMO}; USBD_ROE active to USBD_VMO high	81.55	81.98	ns
3	t_{VPO_ROE}; USBD_VPO high to USBD_ROE deactivated	83.54	83.80	ns
4	t_{VMO_ROE}; USBD_VMO low to USBD_ROE deactivated (includes SE0)	248.90	249.13	ns
5	t_{FEOPT}; SE0 interval of EOP	160.00	175.00	ns
6	t_{PERIOD}; Data transfer rate	11.97	12.03	Mb/s

Table 40. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port B Alternate Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port B Alternate Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns

NOTES

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