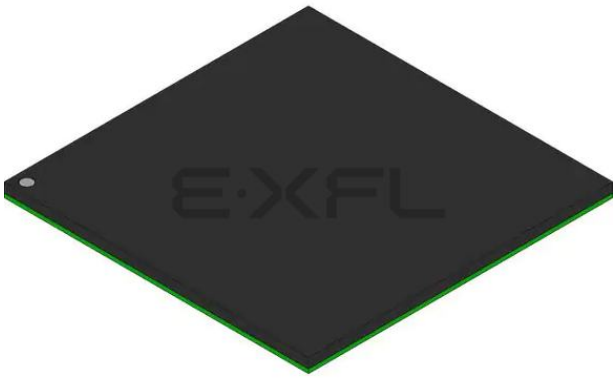

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx1cvm15

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_CLK	MMC Output Clock
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2\_RTS}}$	Request to Send
$\overline{\text{UART2\_CTS}}$	Clear to Send
$\overline{\text{UART2\_DSR}}$	Data Set Ready
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
UART3_RXD	Receive Data
UART3_TXD	Transmit Data
$\overline{\text{UART3\_RTS}}$	Request to Send
$\overline{\text{UART3\_CTS}}$	Clear to Send
$\overline{\text{UART3\_DSR}}$	Data Set Ready
$\overline{\text{UART3\_RI}}$	Ring Indicator
$\overline{\text{UART3\_DCD}}$	Data Carrier Detect
$\overline{\text{UART3\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	T6	$\overline{CS1}$	O									H	
NVDD1	T7	$\overline{CS0}$	O									H[1]	
NVDD1	R6	D5	I/O	69K								Pull-H	
NVDD1	P6	$\overline{ECB}$	I		ETMTRACEPKT7		PA20	69K				Pull-H	$\overline{ECB}$
NVDD1	N6	D4	I/O	69K								Pull-H	
NVDD1	R7	$\overline{LBA}$	O		ETMTRACEPKT6		PA19	69K				H	$\overline{LBA}$
NVDD1	P8	D3	I/O	69K								Pull-H	
NVDD1	R8	BCLK			ETMTRACEPKT5		PA18	69K				L	BCLK
NVDD1	P7	D2	I/O	69K								Pull-H	
	J7	VSS	Static										
NVDD1	L6	NVDD1	Static										
NVDD1	N7	DTACK	I		ETMTRACEPKT4		PA17	69K	SPI2_SS	A25		Pull-H	PA17
NVDD1	N8	D1	I/O	69K								Pull-H	
NVDD1	M7	$\overline{RW}$										H	
NVDD1	T8	MA11	O									L	
NVDD1	M8	MA10	O									L	
NVDD1	R9	D0	I/O	69K								Pull-H	
	K7	VSS	Static										
NVDD1	P9	DQM3	O									L	
NVDD1	T9	DQM2	O									L	
NVDD1	N9	DQM1	O									L	
NVDD1	R10	DQM0	O									L	
NVDD1	M9	$\overline{RAS}$	O									H	
NVDD1	L8	$\overline{CAS}$	O									H	
NVDD1	J8	NVDD1	Static										

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD2	R14	$\overline{TDO}$	O									Hiz[5]	
NVDD2	N15	TMS	I	69K								Pull-H	
NVDD2	L9	TCK	I	69K								Pull-H	
NVDD2	N16	TDI	I	69K								Pull-H	
NVDD2	P14	I2C_SCL	O				PA16	69K				Pull-H	PA16
NVDD2	P15	I2C_SDA	I/O				PA15	69K				Pull-H	PA15
NVDD2	N13	CSI_PIXCLK	I				PA14	69K				Pull-H	PA14
NVDD2	M13	CSI_HSYNC	I				PA13	69K				Pull-H	PA13
NVDD2	M14	CSI_VSYNC	I				PA12	69K				Pull-H	PA12
NVDD2	N14	CSI_D7	I				PA11	69K				Pull-H	PA11
NVDD2	M15	CSI_D6	I				PA10	69K				Pull-H	PA10
NVDD2	M16	CSI_D5	I				PA9	69K				Pull-H	PA9
NVDD2	J10	VSS	Static										
NVDD2	M12	CSI_D4	I				PA8	69K				Pull-H	PA8
NVDD2	L16	CSI_D3	I				PA7	69K				Pull-H	PA7
NVDD2	L15	CSI_D2	I				PA6	69K				Pull-H	PA6
NVDD2	L14	CSI_D1	I				PA5	69K				Pull-H	PA5
NVDD2	L13	CSI_D0	I				PA4	69K				Pull-H	PA4
NVDD2	L12	CSI_MCLK	O				PA3	69K				Pull-H	PA3
NVDD2	L11	PWMO	O				PA2	69K				Pull-H	PA2
NVDD2	L10	TIN	I				PA1	69K			SPI2_RxD	Pull-H	PA1
NVDD2	K15	TMR2OUT	O				PD31	69K	SPI2_TxD			Pull-H	PD31
NVDD2	K16	LD15	O				PD30	69K				Pull-H	PD30
NVDD2	K14	LD14	O				PD29	69K				Pull-H	PD29
NVDD2	K13	LD13	O				PD28	69K				Pull-H	PD28

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
QVDD[6]	D12	NC	O										
QVDD4	A13	QVDD4	Static										
	B13	VSS	Static										
BTRFVDD	C12	BTRFVDD	Static										
BTRFVDD	B12	BT1	I				PC31	69K			UART3_RX	Pull-H	PC31
BTRFVDD	F11	BT2	O				PC30	69K		UART3_TX		Hiz	PC30
BTRFVDD	A12	BT3	I				PC29	69K			UART3_RTS	Pull-H	PC29
BTRFVDD	E11	BT4	I				PC28	69K		UART3_CTS		Pull-H	PC28
BTRFVDD	A11	BT5	I/O				PC27	69K		UART3_DCD		Pull-H	PC27
BTRFVDD	D11	BT6	O				PC26	69K		SPI2_SS3	UART3_DTR	L	PC26
BTRFVDD	B11	BT7	O				PC25	69K		UART3_DSR		L	PC25
BTRFVDD	C11	BT8	O		SSI2_RXFS		PC24	69K		UART3_RI		Hiz	PC24
BTRFVDD	G10	BT9	O		SSI2_RX		PC23	69K				L	PC23
BTRFVDD	F10	BT10	O		SSI2_TX		PC22	69K				H	PC22
BTRFVDD	B10	BT11	O		SSI2_TXCLK		PC21	69K				H	PC21
BTRFVDD	E10	BT12	O		SSI2_TXFS		PC20	69K				Hiz	PC20
BTRFVDD	D10	BT13	O		SSI2_RXCLK		PC19	69K				L	PC19
	C10	BTRFGND	Static										
NVDD3	A10	NVDD3	Static										
NVDD3	G9	SPI1_MOSI	I/O				PC17	69K				Pull-H	PC17
NVDD3	F9	SPI1_MISO	I/O				PC16	69K				Pull-H	PC16
NVDD3	E9	SPI1_$\overline{SS}$	I/O				PC15	69K				Pull-H	PC15
NVDD3	B9	SPI1_SCLK	I/O				PC14	69K				Pull-H	PC14
NVDD3	D9	SPI1_$\overline{SPI_RDY}$	I				PC13	69K			$\overline{DMA\_Req}$	Pull-H	PC13
NVDD3	A9	UART1_RXD	I				PC12	69K				Pull-H	PC12

in the system, these Bluetooth pins can be used as general purpose I/O pins and BTRFVDD can be used as other NVDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 5. Recommended Operating Range

Symbol	Rating	Minimum	Maximum	Unit
T_A	Operating temperature range MC9328MX1VM20\MC9328MX1VM15	0	70	°C
T_A	Operating temperature range MC9328MX1DVM20\MC9328MX1DVM15	-30	70	°C
T_A	Operating temperature range MC9328MX1CVM15	-40	85	°C
NVDD	I/O supply voltage (if using MSHC, CSI, SPI, BTA, LCD, and USBd which are only 3 V interfaces)	2.70	3.30	V
NVDD	I/O supply voltage (if not using the peripherals listed above)	1.70	3.30	V
QVDD	Internal supply voltage (Core = 150 MHz)	1.70	1.90	V
QVDD	Internal supply voltage (Core = 200 MHz)	1.80	2.00	V
AVDD	Analog supply voltage	1.70	3.30	V

3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the “Power-Up Sequence” section of application note AN2537 on the i.MX applications processor website.

3.4 DC Electrical Characteristics

Table 6 contains both maximum and minimum DC characteristics of the i.MX1 processor.

Table 6. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Min	Typical	Max	Unit
Iop	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, MPEG4 decoding playback from external memory card to both external SSI audio decoder and driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	–	QVDD at 1.8V = 120mA; NVDD+AVDD at 3.0V = 30mA	–	mA
$Sidd_1$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 25°C)	–	25	–	µA
$Sidd_2$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 55°C)	–	45	–	µA
$Sidd_3$	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 25°C)	–	35	–	µA

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA

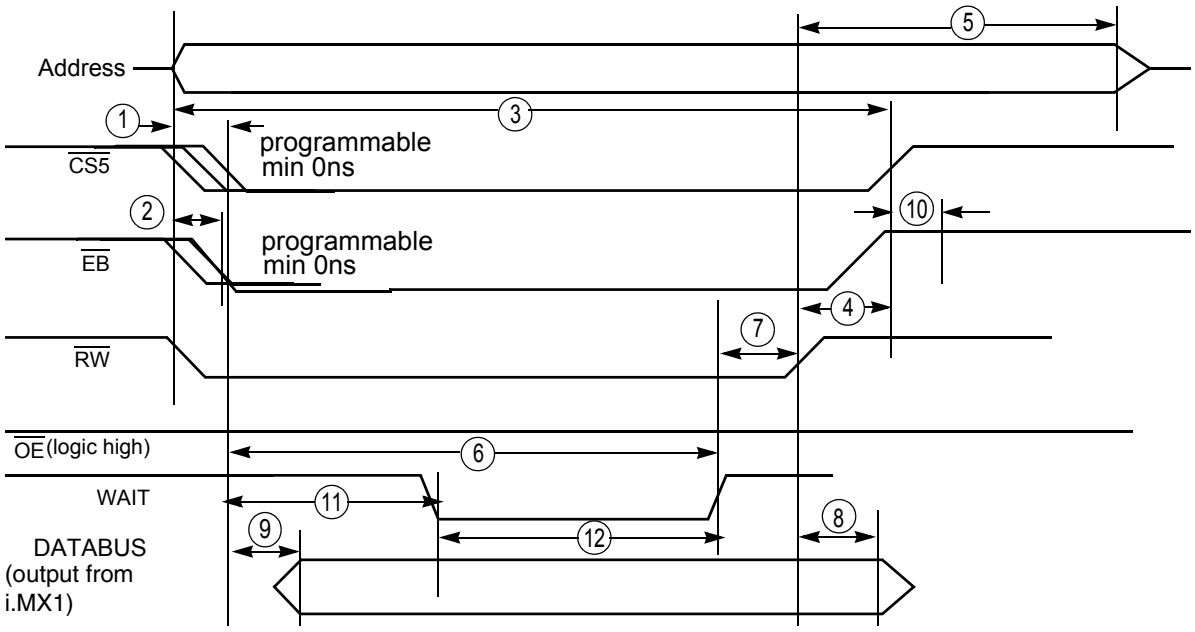


Figure 8. WAIT Write Cycle without DMA

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-0.29	2.5T+0.68	ns
5	$\overline{RW}$ negated to Address inactive	67.28	–	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns

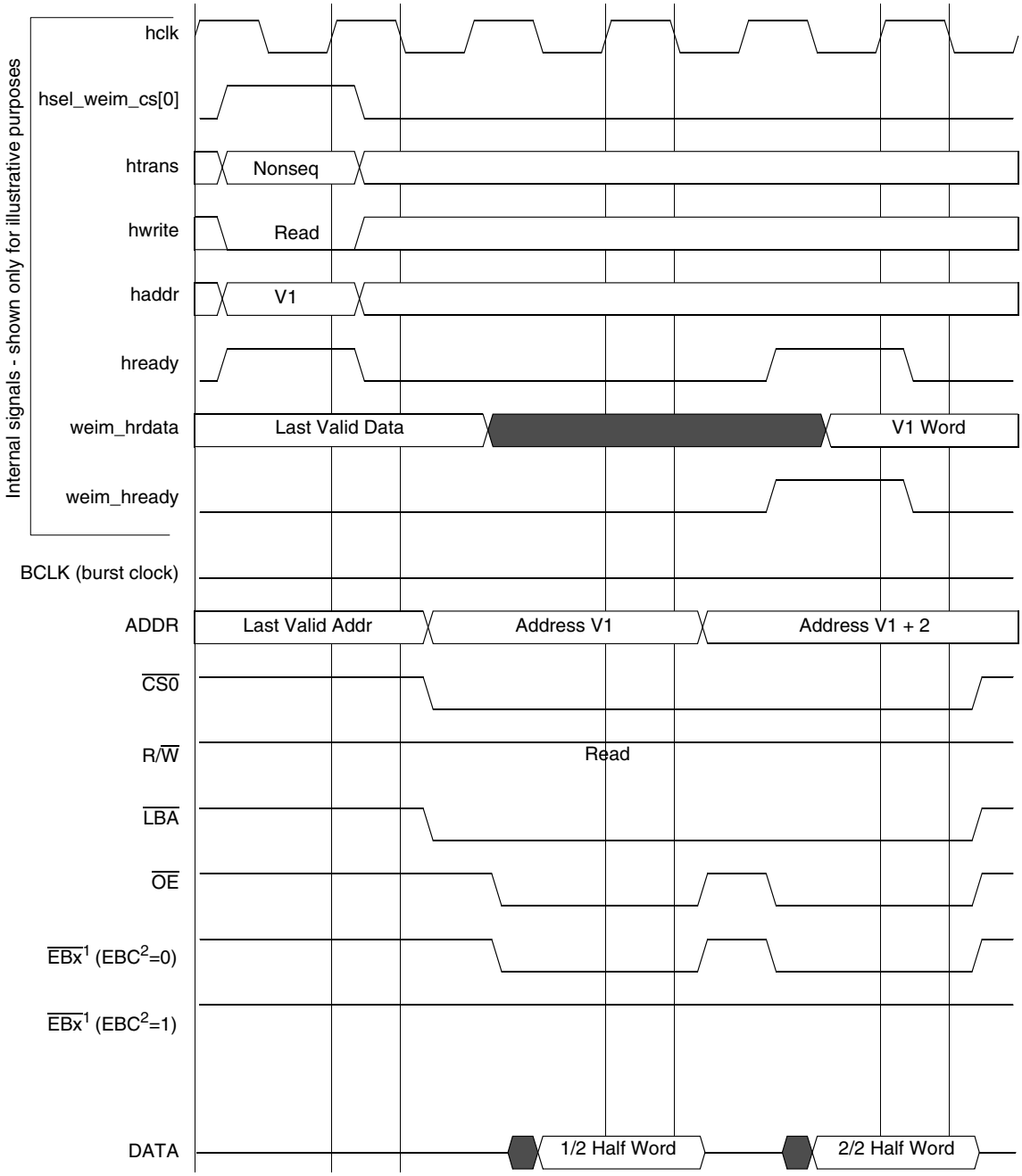
Table 16. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-0.29	2.5T+0.68	ns
5	Address inactived after $\overline{CS}$ negated	–	0.93	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
7	Wait asserted to $\overline{RW}$ negated	T+2.15	2T+7.34	ns
8	Data hold timing after $\overline{RW}$ negated	24.87	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
11	$\overline{EB}$ negate after $\overline{CS}$ negate	1.5T+0.74	1.5T+2.35	
12	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
13	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4.The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.3 EIM External Bus Timing

The External Interface Module (EIM) is the interface to devices external to the i.MX1, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 12. WSC = 1, OEA = 1, A.WORD/E.HALF

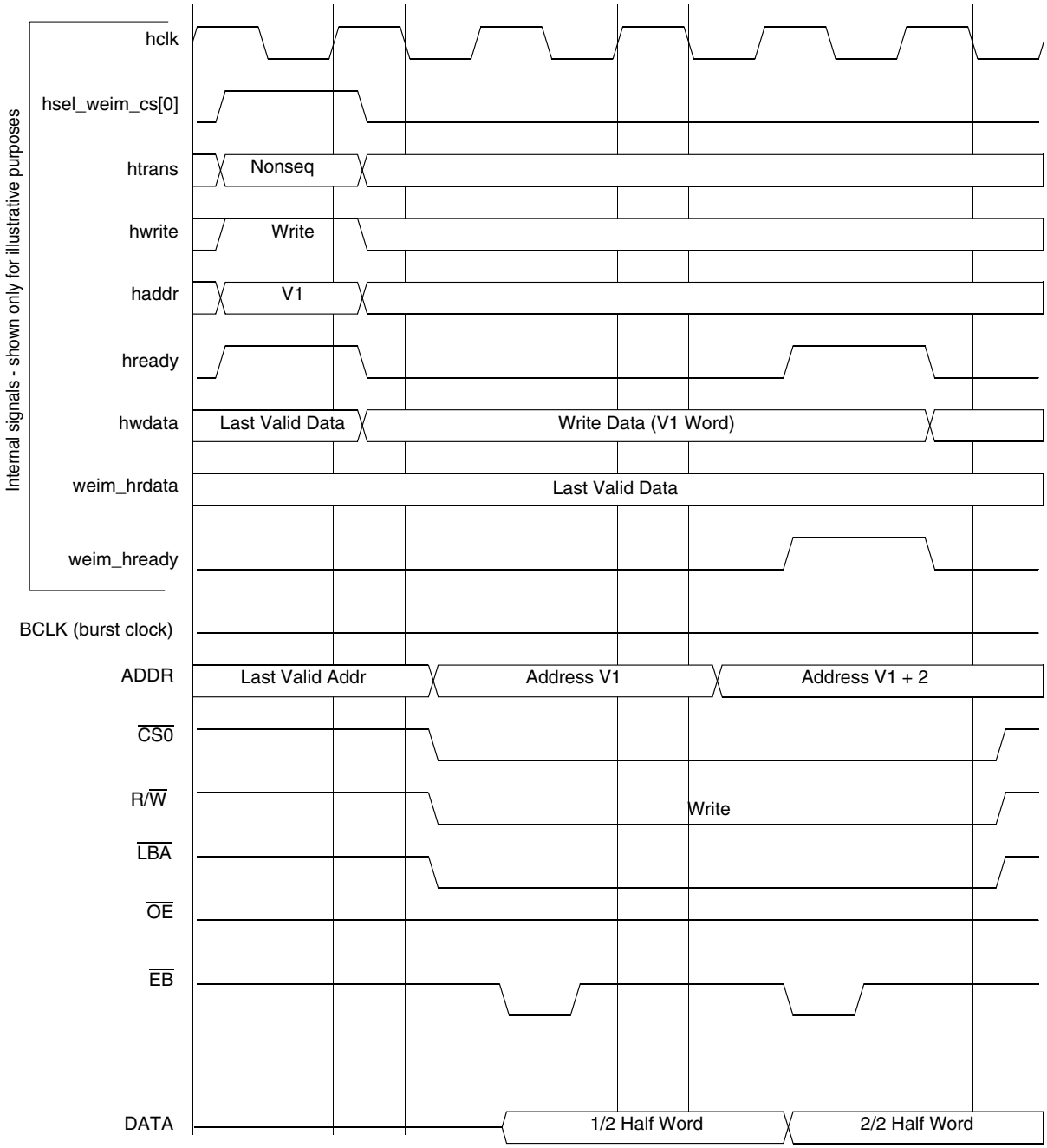


Figure 13. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

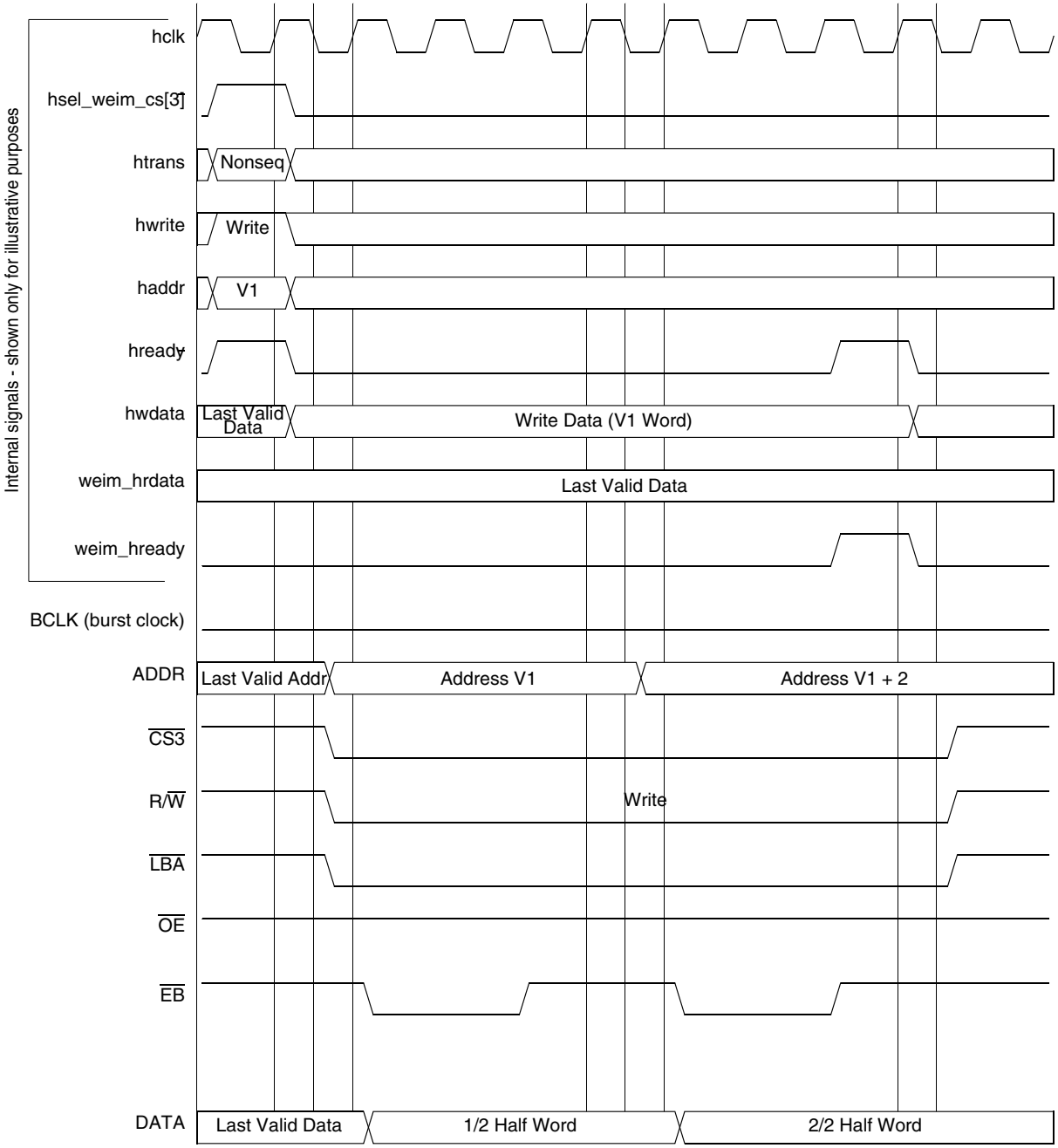


Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF

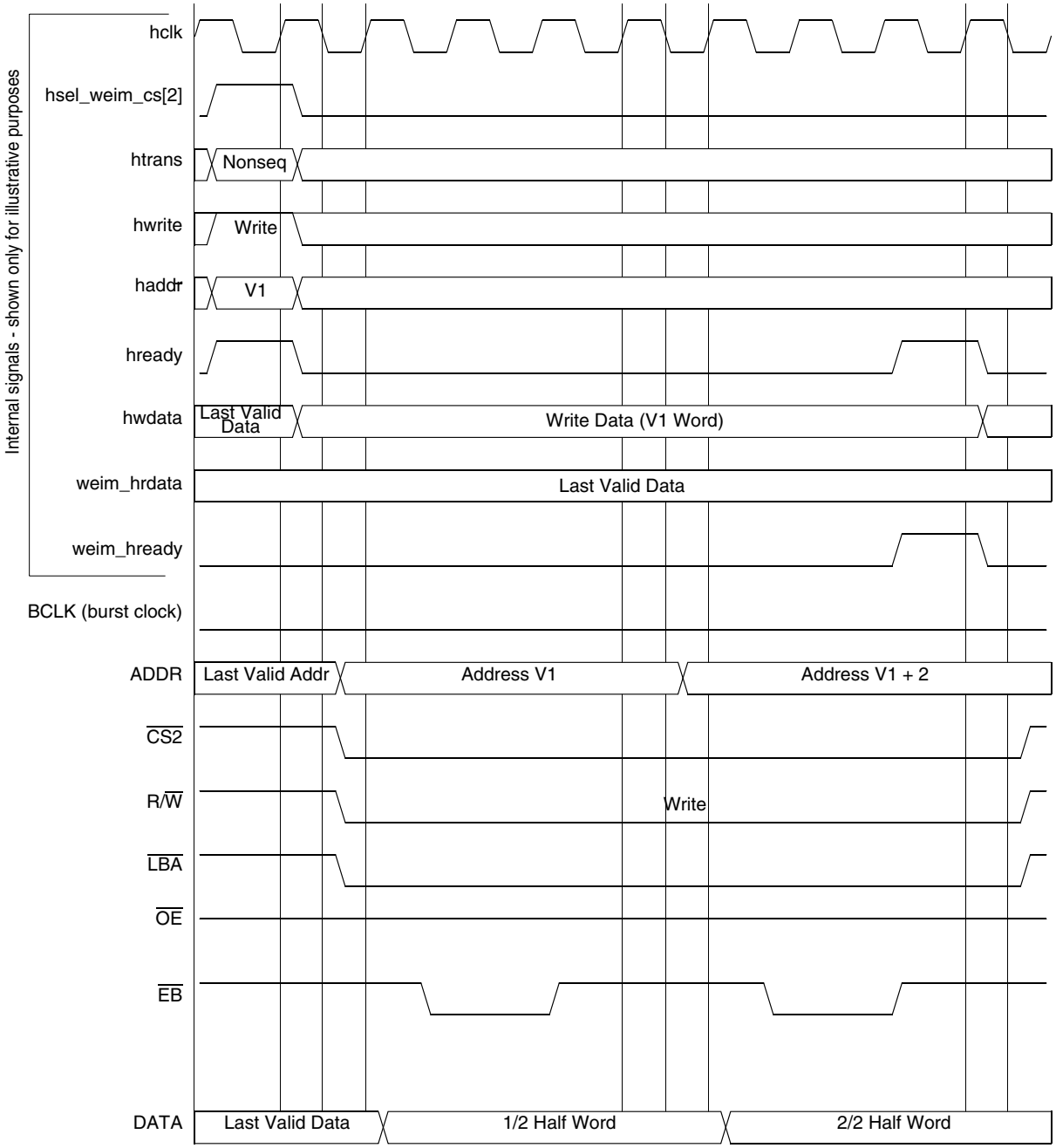
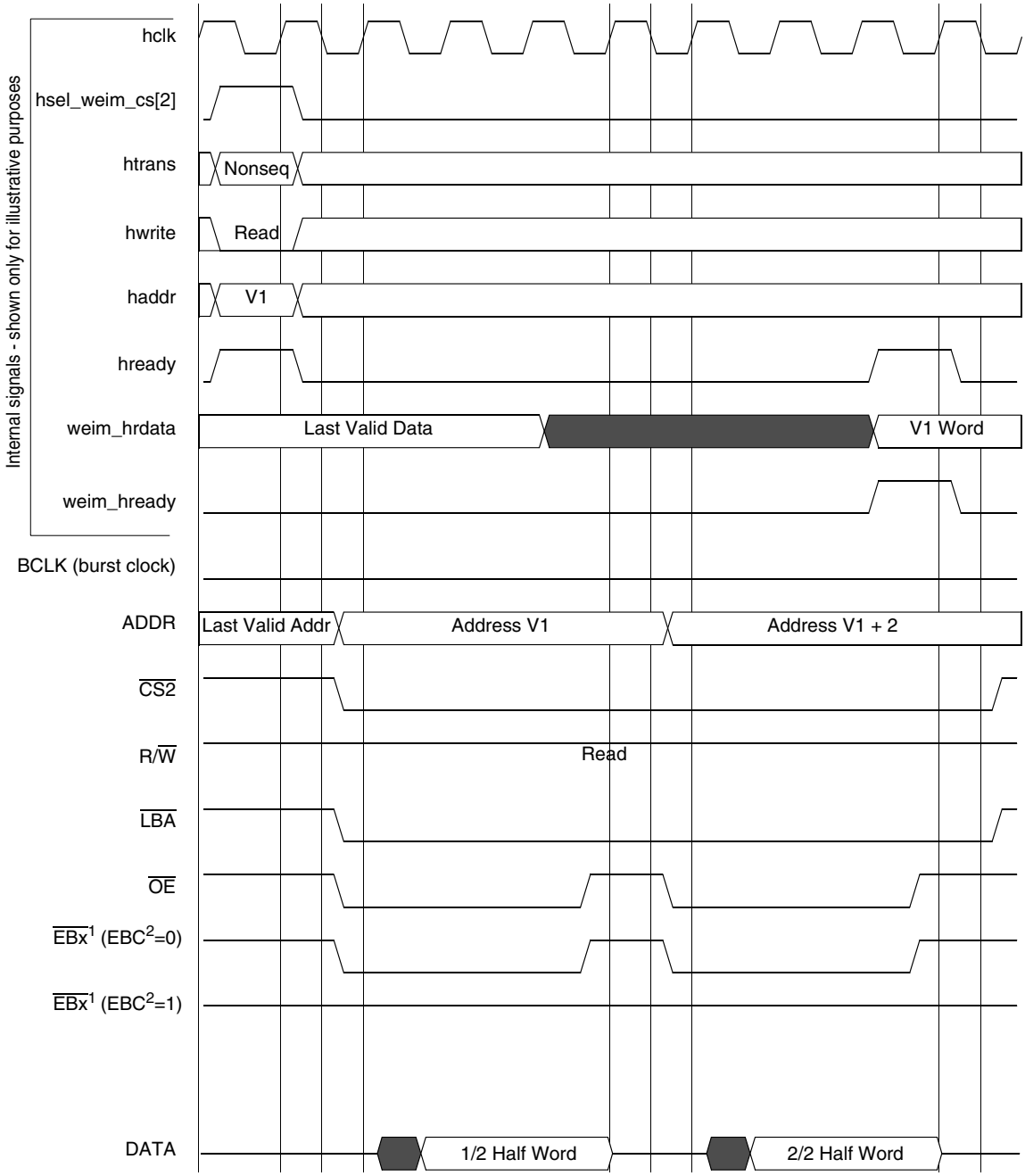


Figure 17. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF

Table 19. Pen ADC Test Conditions

Vp max	1800 mV	ip max	+7 µA
Vp min	GND	ip min	1.5 µA
Vn	GND	in	1.5 µA
Sample frequency		12 MHz	
Sample rate		1.2 KHz	
Input frequency		100 Hz	
Input range		0–1800 mV	
Note: Ru1 = Ru2 = 200K			

Table 20. Pen ADC Absolute Rating

ip max	+9.5 µA
ip min	-2.5 µA
in max	+9.5 µA
in min	-2.5 µA

4.6 ASP Touch Panel Controller

The following sections contain the electrical specifications of the ASP touch panel controller. The value of parameters and their corresponding measuring conditions are mentioned as well.

4.6.1 Electrical Specifications

Test conditions: Temperature = 25º C, QVDD = 1800mV.

Table 21. ASP Touch Panel Controller Electrical Spec

Parameter	Minimum	Typical	Maximum	Unit
Offset	–	32768	–	–
Offset Error	–	–	8199	–
Gain	–	13.65	–	mV^{-1}
Gain Error	–	–	33%	–
DNL	8	9	–	Bits
INL	–	0	–	Bits
Accuracy (without missing code)	8	9	–	Bits
Operating Voltage Range (Pen)	–	–	QVDD	mV
Operating Voltage Range (U)	Negative QVDD	–	QVDD	mV
On-resistance of switches SW[8:1]	–	10	–	Ohm

Note that QVDD should be 1800mV.

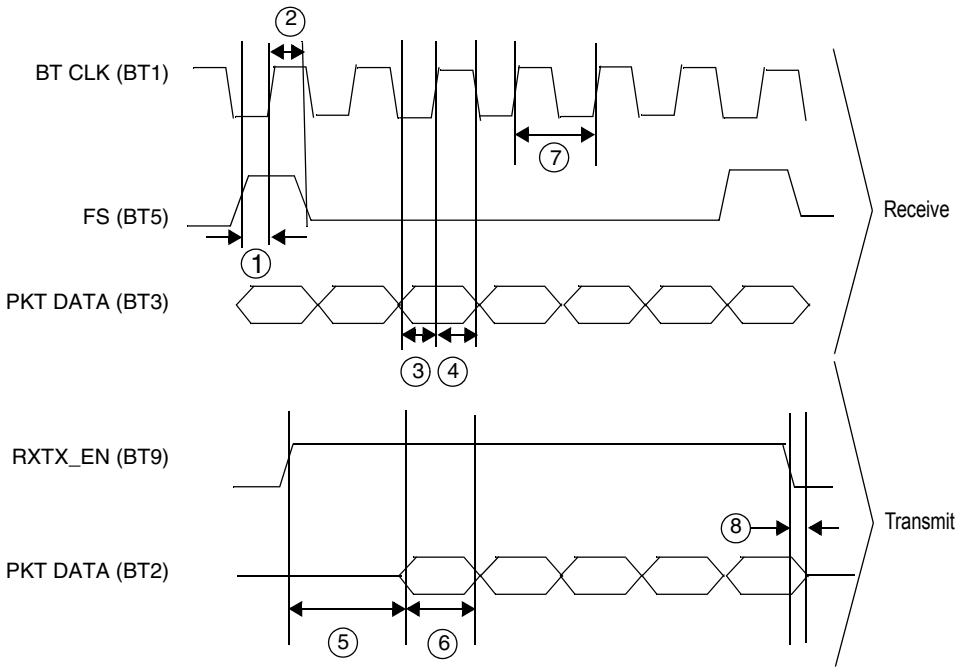


Figure 37. MC13180 Data Bus Timing Diagram

Table 22. MC13180 Data Bus Timing Parameter Table

Ref No.	Parameter	Minimum	Typical	Maximum	Unit
1	FrameSync setup time relative to BT CLK rising edge[1]	–	4	–	ns
2	FrameSync hold time relative to BT CLK rising edge[1]	–	12	–	ns
3	Receive Data setup time relative to BT CLK rising edge[1]	–	6	–	ns
4	Receive Data hold time relative to BT CLK rising edge[1]	–	13	–	ns
5	Transmit Data setup time relative to RXTX_EN rising edge[2]	172.5	–	192.5	µs
6	TX DATA period	1000 +/- 0.02			ns
7	BT CLK duty cycle	40	–	60	%
8	Transmit Data hold time relative to RXTX_EN falling edge	4	–	10	µs

1 Please refer to 2.4 GHz RF Transceiver Module (MC13180) Technical Data documentation.

2 The setup and hold times of RX_TX_EN can be adjusted by programming Time_A_B register (0x00216050) and RF_Status (0x0021605C) registers.

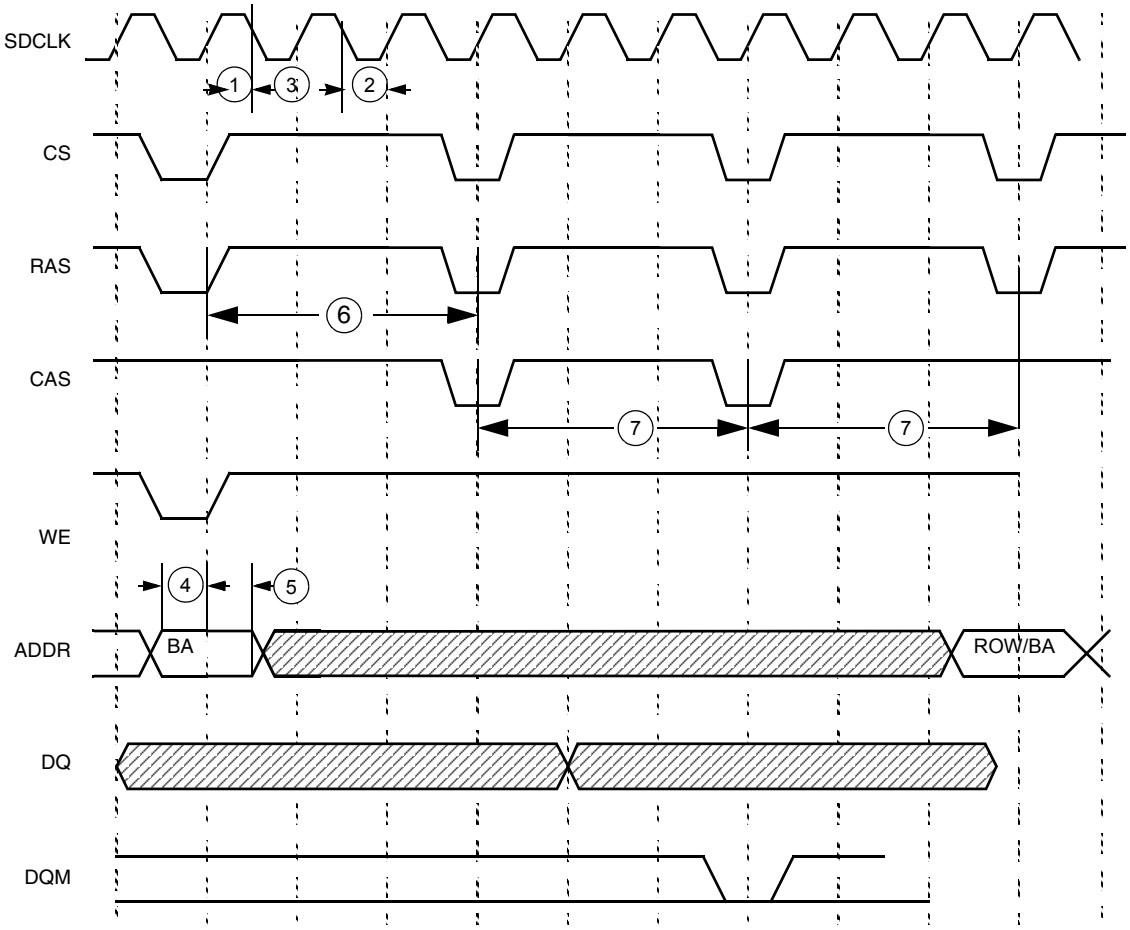


Figure 59. SDRAM Refresh Timing Diagram

Table 35. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP1}	–	ns
7	Auto precharge command period	t_{RC1}	–	t_{RC1}	–	ns

[1] t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *MC9328MX1 reference manual*.

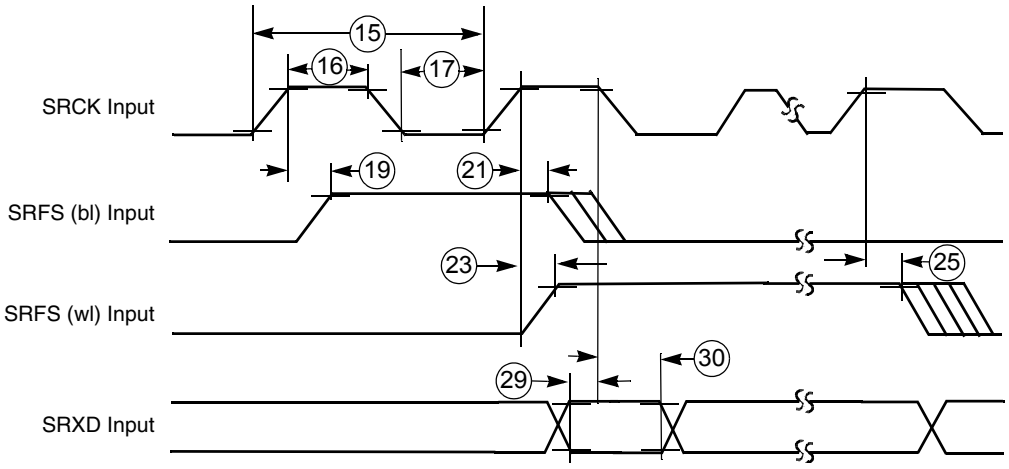


Figure 67. SSI Receiver External Clock Timing Diagram

Table 39. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Primary Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.5	4.5	1.3	3.9	ns
3	SRCK high to SRFS (bl) high[3]	-1.2	-1.7	-1.1	-1.5	ns
4	STCK high to STFS (bl) low[3]	2.5	4.3	2.2	3.8	ns
5	SRCK high to SRFS (bl) low[3]	0.1	-0.8	0.1	-0.8	ns
6	STCK high to STFS (wl) high[3]	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high[3]	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low[3]	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low[3]	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	–	18.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Primary Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns

Table 39. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function[2])						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port C Primary Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1 All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

2 There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

3 bl = bit length; wl = word length.

Table 40. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	STCK high to STXD high impedance	17.90	29.75	15.7	26.1	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hold time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port B Alternate Function[2])						
31	SRXD setup before STCK falling	18.81	–	16.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port B Alternate Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1 All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

2 There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

3 bl = bit length; wl = word length.

Table 41. SSI 2 (Port C Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8V +/- 0.10V		3.0V +/- 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Alternate Function)[2]						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns

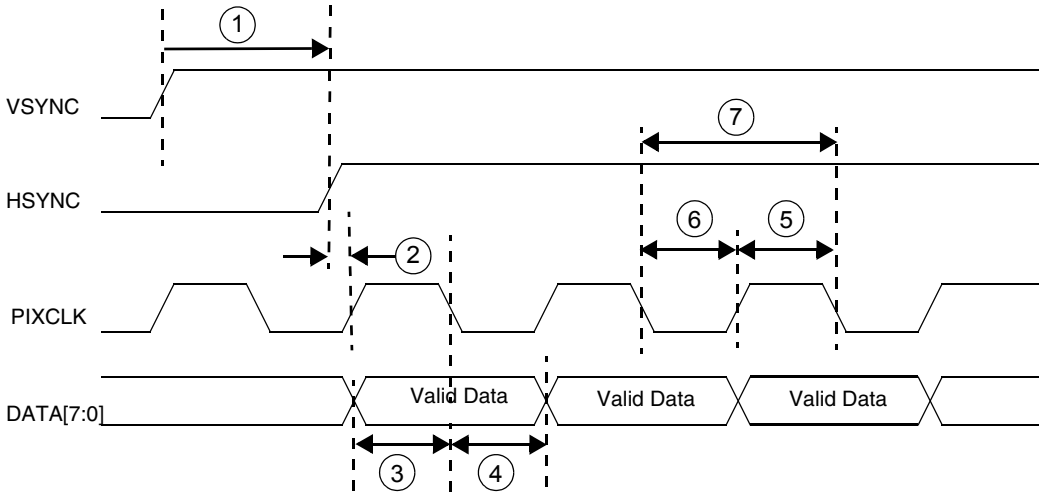


Figure 69. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge

Table 42. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

6 Product Documentation

6.1 Revision History

Table 45 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 45. i.MX1 Data Sheet Revision History Rev. 7

Location	Revision
Table 1 on page 3 Signal Names and Descriptions	• Added the DMA_REQ signal to table. • Corrected signal name from $\overline{\text{USBD\_OE}}$ to $\overline{\text{USBD\_ROE}}$ • Corrected signal names From: C10 BTRFGN, To: BTRFGND From: G6 SIM_RST, To: SIM_RX From: G7 UART2_TXD, To: SIM_CLK
Table 3 on page 11 Signal Multiplex Table i.MX1	Added Signal Multiplex table from Reference Manual with the following changes: • Changed I/O Supply Voltage, PB31–14, from NVDD3 to NVDD4 • Corrected footnotes 1–5. • Changed AVDD2 references to QVDD, except for C14. Added footnote regarding ESD. • Changed occurrence of SD_SCLK to SD_CLK. • Removed 69K pull-up resistor from EB1, EB2, and added to D9
Table 10 on page 26	Changed first and second parameters descriptions: From: Reference Clock freq range, To: DPLL input clock freq range From: Double clock freq range, To: DPLL output freq range
Table 3 on page 11	Added Signal Multiplex table.

6.2 Reference Documents

The following documents are required for a complete description of the MC9328MX1 and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MX1 Product Brief (order number MC9328MX1P)

MC9328MX1 Reference Manual (order number MC9328MX1RM)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.