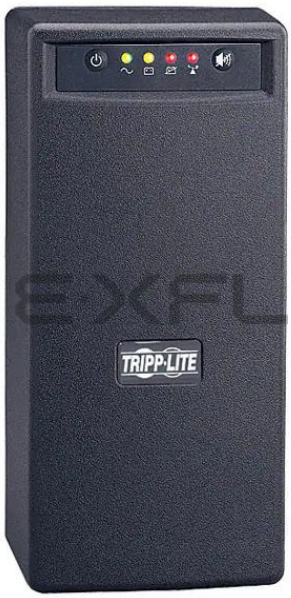

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx1cvm15r2

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SIM_TX	Transmit Data
SIM_PD	Presence Detect Schmitt trigger input
SIM_SVEN	SIM Vdd Enable
SPI 1 and SPI 2	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_$\overline{SS}$	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_$\overline{SPI_RDY}$	Serial Data Ready
SPI2_TXD	SPI2 Master TxData Output—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_RXD	SPI2 Master RxData Input—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_$\overline{SS}$	SPI2 Slave Select—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_SCLK	SPI2 Serial Clock—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
$\overline{USBD\_ROE}$	USB $\overline{OE}$
USBD_AFE	USB Analog Front End Enable
Secure Digital Interface	
SD_CMD	SD Command—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added.

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_CLK	MMC Output Clock
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2\_RTS}}$	Request to Send
$\overline{\text{UART2\_CTS}}$	Clear to Send
$\overline{\text{UART2\_DSR}}$	Data Set Ready
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
UART3_RXD	Receive Data
UART3_TXD	Transmit Data
$\overline{\text{UART3\_RTS}}$	Request to Send
$\overline{\text{UART3\_CTS}}$	Clear to Send
$\overline{\text{UART3\_DSR}}$	Data Set Ready
$\overline{\text{UART3\_RI}}$	Ring Indicator
$\overline{\text{UART3\_DCD}}$	Data Carrier Detect
$\overline{\text{UART3\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD4	F6	SIM_RST	O		SSI_TXFS	I/O	PB18	69K				Pull-H	PB18
NVDD4	G6	SIM_RX	I		SSI_TXDAT	O	PB17	69K				Pull-H	PB17
NVDD4	B4	SIM_TX	I/O		SSI_RXDAT	I	PB16	69K				Pull-H	PB16
NVDD4	C4	SIM_PD	I		SSI_RXCLK	I/O	PB15	69K				Pull-H	PB15
NVDD4	D4	SIM_SVEN	O		SSI_RXFS	I/O	PB14	69K				Pull-H	PB14
NVDD4	B3	SD_CMD	I/O		MS_BS	O	PB13	69K				Pull-H	PB13
NVDD4	A3	SD_CLK	O		MS_SCLKO	O	PB12	69K				Pull-H	PB12
NVDD4	A2	SD_DAT3	I/O		MS_SDIO	I/O	PB11	69K (pull down)				Pull-L	PB11
NVDD4	E5	SD_DAT2	I/O		MS_SCLKI	I	PB10	69K				Pull-H	PB10
NVDD4	B2	SD_DAT1	I/O		MS_PI1	I	PB9	69K				Pull-H	PB9
NVDD4	C3	SD_DAT0	I/O		MS_PI0	I	PB8	69K				Pull-H	PB8

1 After reset, $\overline{CS0}$ goes H/L depends on BOOT[3:0].

2 Need external circuitry to drive the signal.

3 Need external pull-up.

4 External resistor is needed.

5 Need external pull-up or pull-down.

6 ASP signals are clamped by AVDD2 to prevent ESD (electrostatic discharge) damage. AVDD2 must be greater than QVDD to keep diodes reverse-biased.

Table 6. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Min	Typical	Max	Unit
$Sidd_4$	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 55°C)	–	60	–	µA
V_{IH}	Input high voltage	$0.7V_{DD}$	–	Vdd+0.2	V
V_{IL}	Input low voltage	–	–	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	–	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	–	–	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	–	–	±1	µA
I_{IH}	Input high leakage current (V_{IN} = V_{DD}, no pull-up or pull-down)	–	–	±1	µA
I_{OH}	Output high current (V_{OH} = $0.8V_{DD}$, V_{DD} = 1.8V)	4.0	–	–	mA
I_{OL}	Output low current (V_{OL} = 0.4V, V_{DD} = 1.8V)	-4.0	–	–	mA
I_{OZ}	Output leakage current (V_{out} = V_{DD}, output is high impedance)	–	–	±5	µA
C_i	Input capacitance	–	–	5	pF
C_o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 8. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms

Table 8. 32k/16M Oscillator Signal Timing (Continued)

Parameter	Minimum	RMS	Maximum	Unit
EXTAL16M input jitter (peak to peak) [1]	–	TBD	TBD	–
EXTAL16M startup time [1]	TBD	–	–	–

[1] The 16 MHz oscillator is not recommended for use in new designs.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MX1.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

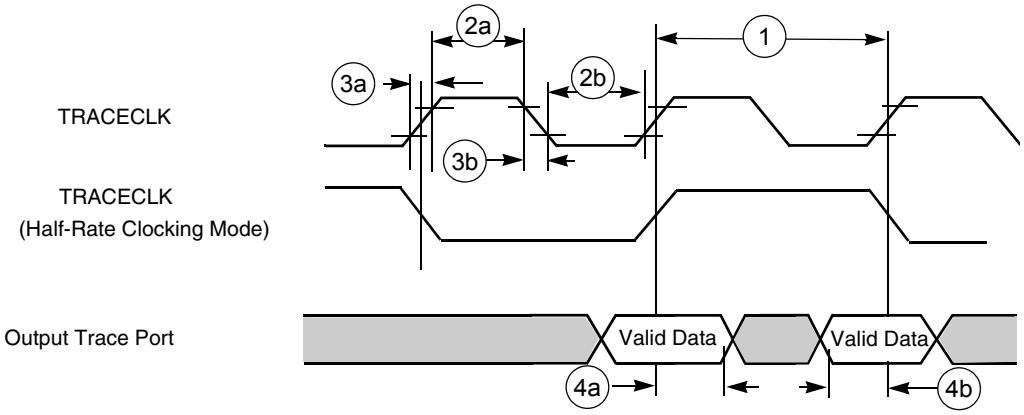


Figure 2. Trace Port Timing Diagram

Table 10. DPLL Specifications (Continued)

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.8V	–	1.0 (10%)	1.5	ns
Power supply voltage	–	1.7	–	2.5	V
Power dissipation	FOL mode, integer MF, f_{dck} = MHz, Vcc = 1.8V	–	–	4	mW

4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4.

NOTE

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

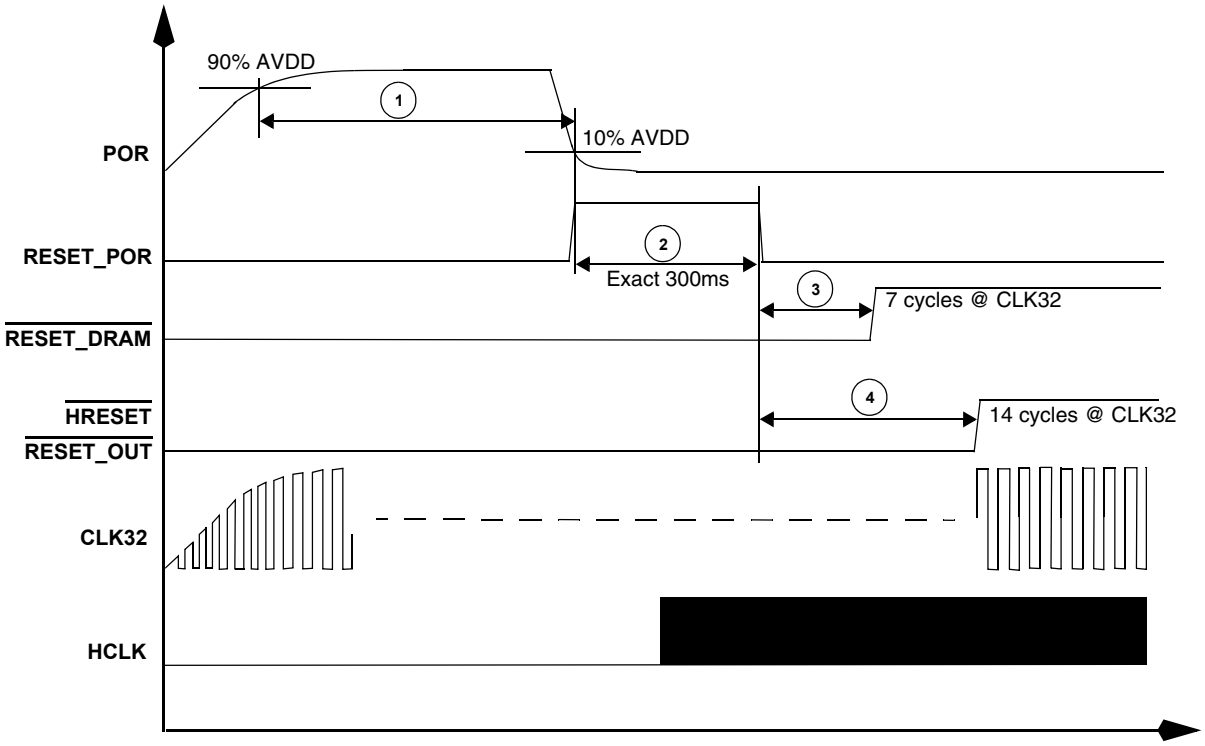
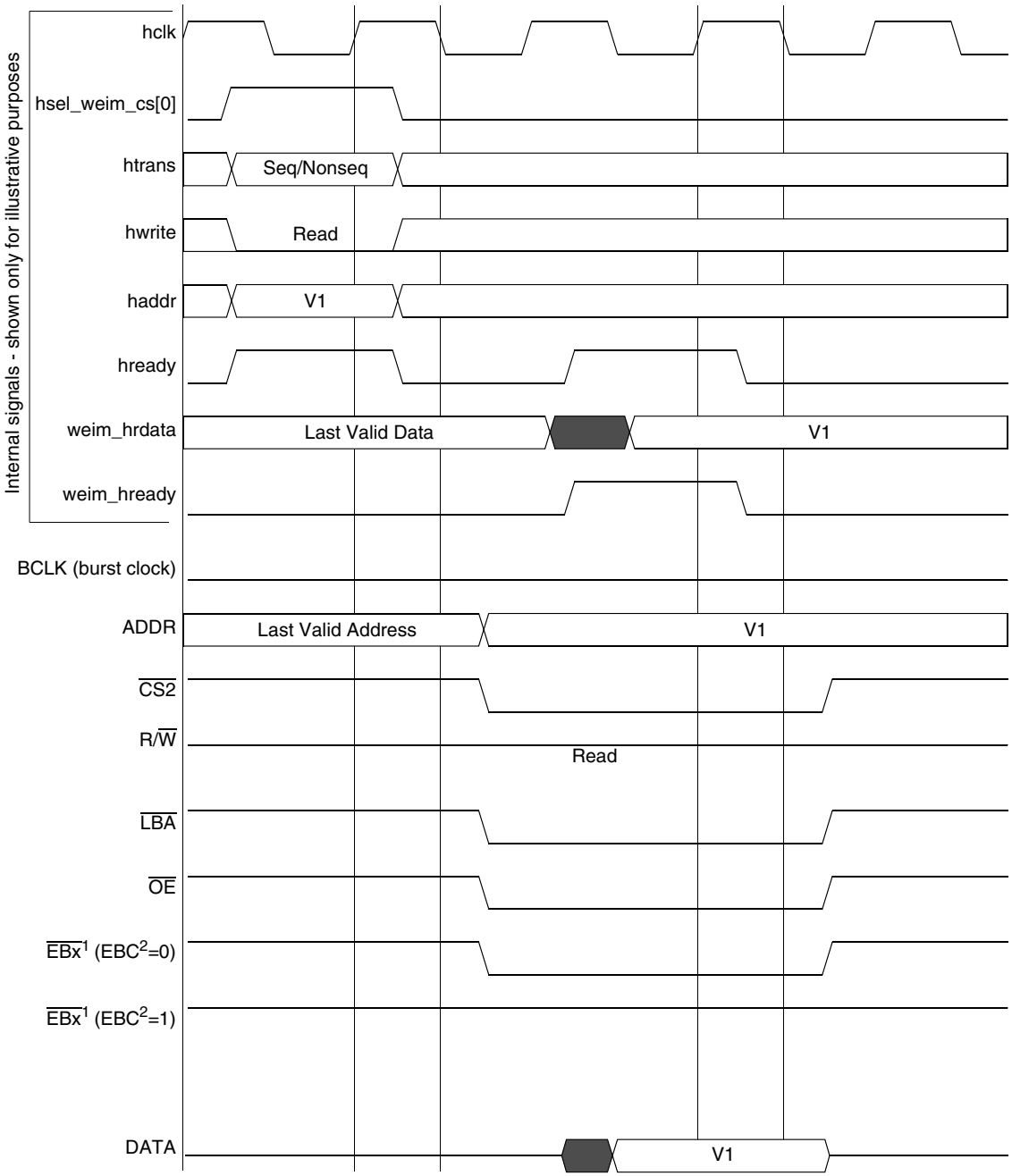
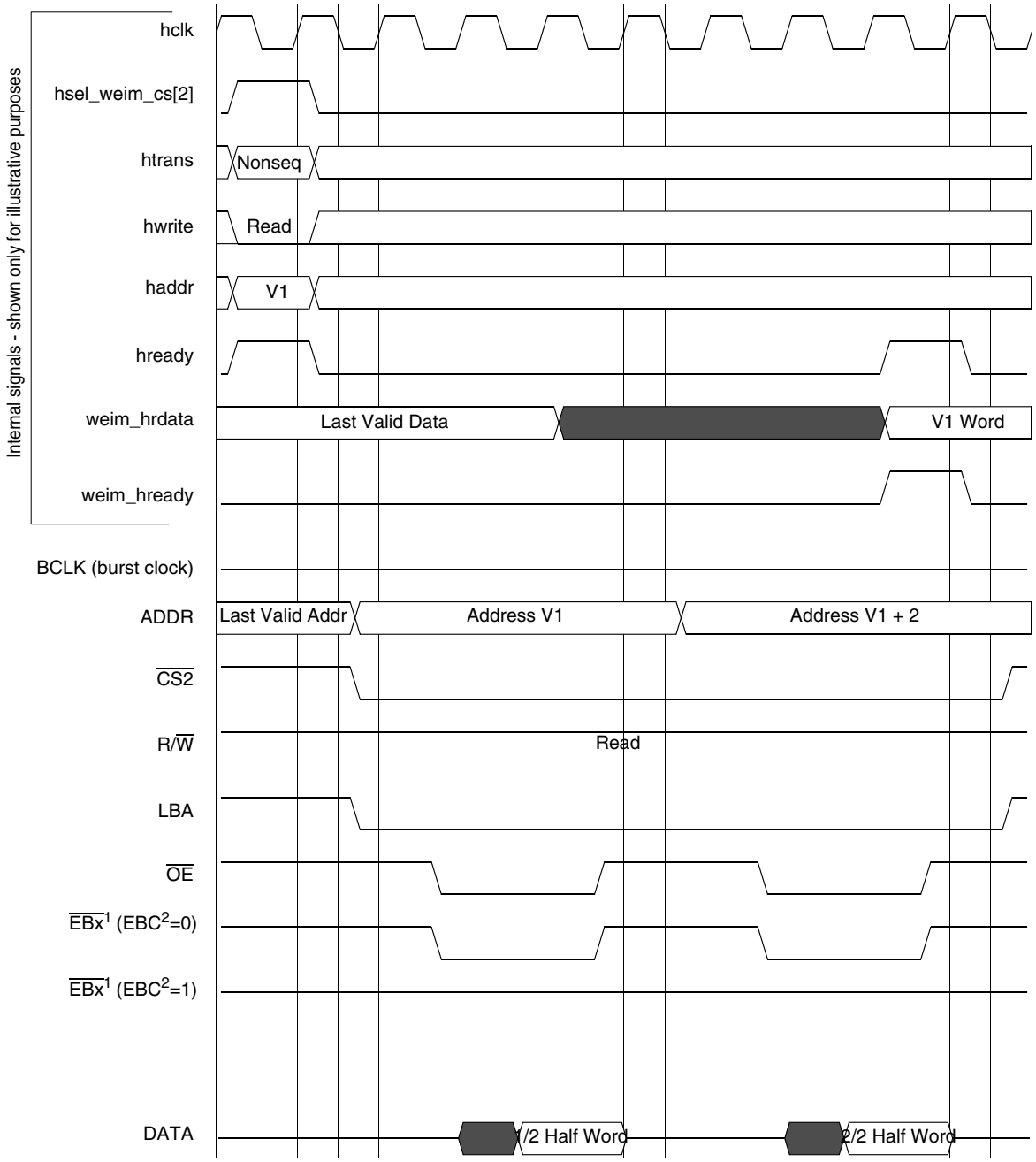


Figure 3. Timing Relationship with POR



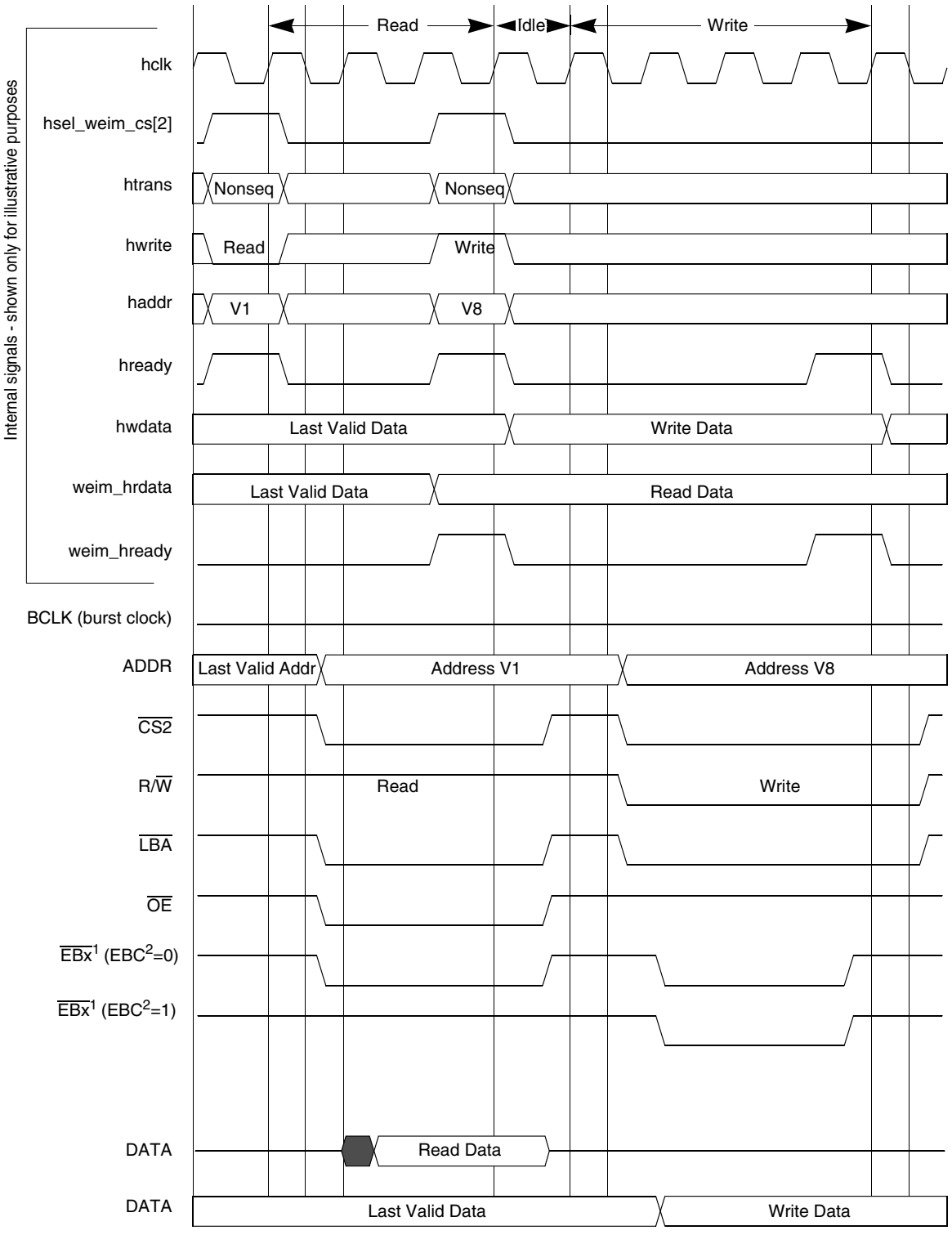
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 10. WSC = 1, A.HALF/E.HALF



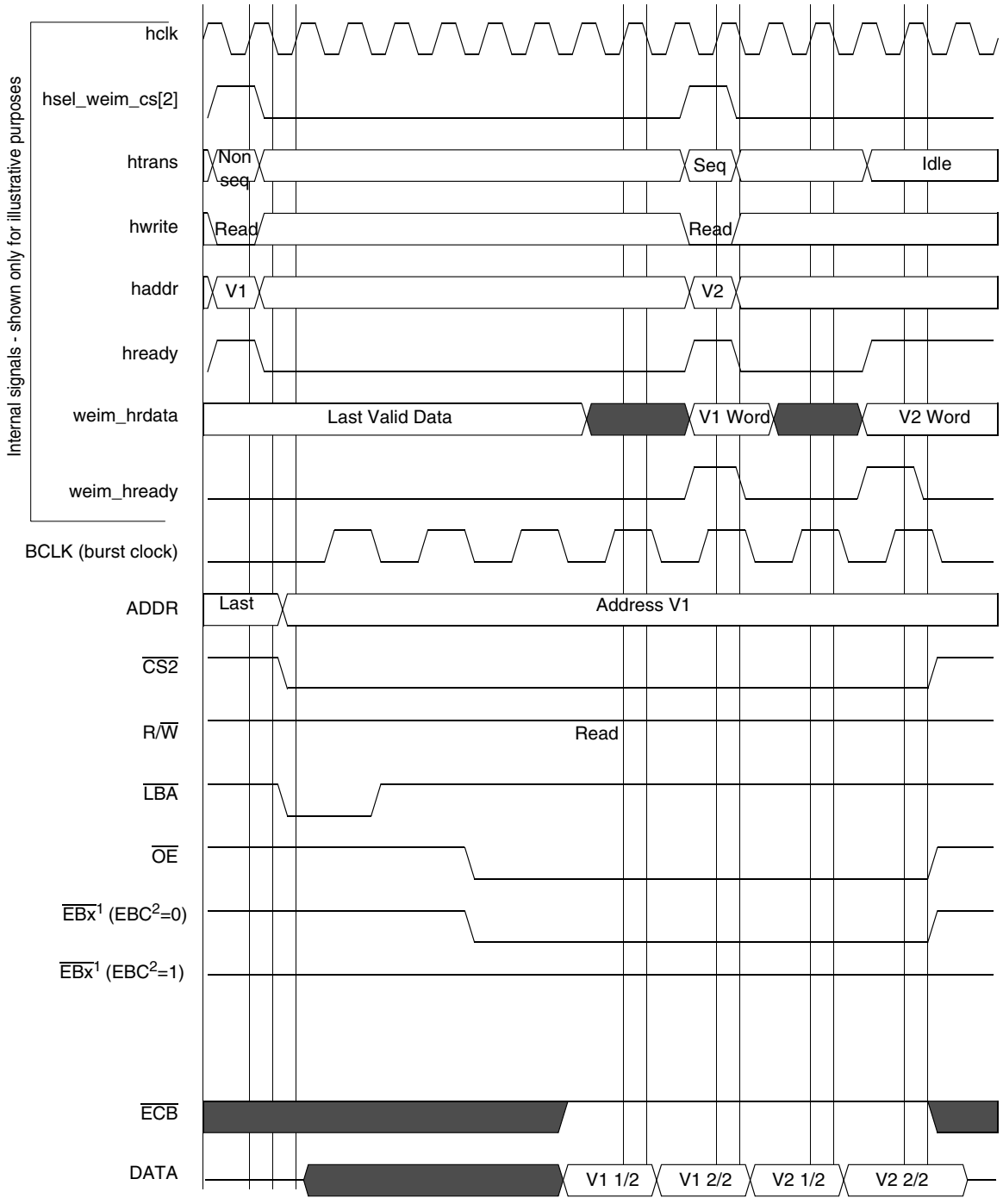
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 23. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

4.6.4 Gain Error Calculations

Gain error calculations are made using the information in this section.

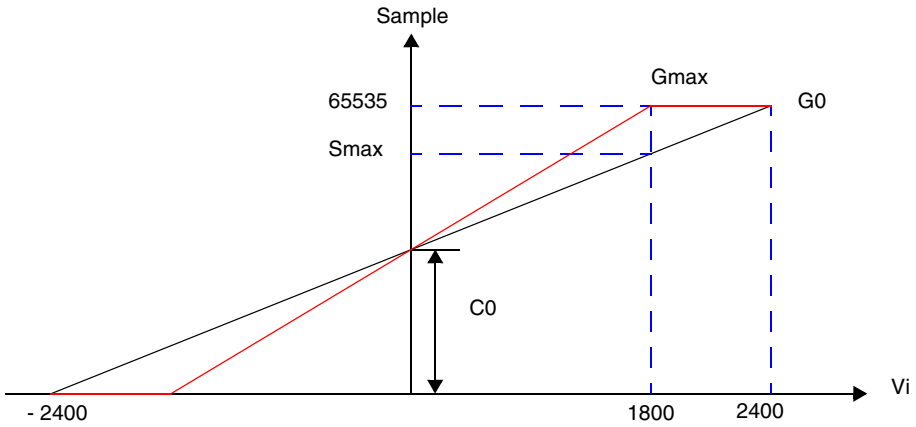


Figure 36. Gain Error Calculations

Assuming the offset remains unchanged, the mapping is rotated around y-intercept to determine the maximum gain allowed. This occurs when the sample at 1800mV has just reached the ceiling of the 16-bit range, 65535.

Maximum Offset $G_{max,}$

G_{max} $= (65535 - C_{0)} / 1800$
$= (65535 - 32767) / 1800$
$= 18.20$

Gain Error $G_{r,}$

G_r $= (G_{max} - G_0) / G_0 * 100\%$
$= (18.20 - 13.65) / 13.65 * 100\%$
$= 33\%$

4.7 Bluetooth Accelerator

CAUTION

On-chip accelerator hardware is not supported by software. An external Bluetooth chip interfaced to a UART is recommended.

The Bluetooth Accelerator (BTA) radio interface supports the Wireless RF Transceiver, MC13180 using an SPI interface. This section provides the data bus timing diagrams and SPI interface timing diagrams shown in Figure 37 and Figure 38, and the associated parameters shown in Table 22 and Table 23.

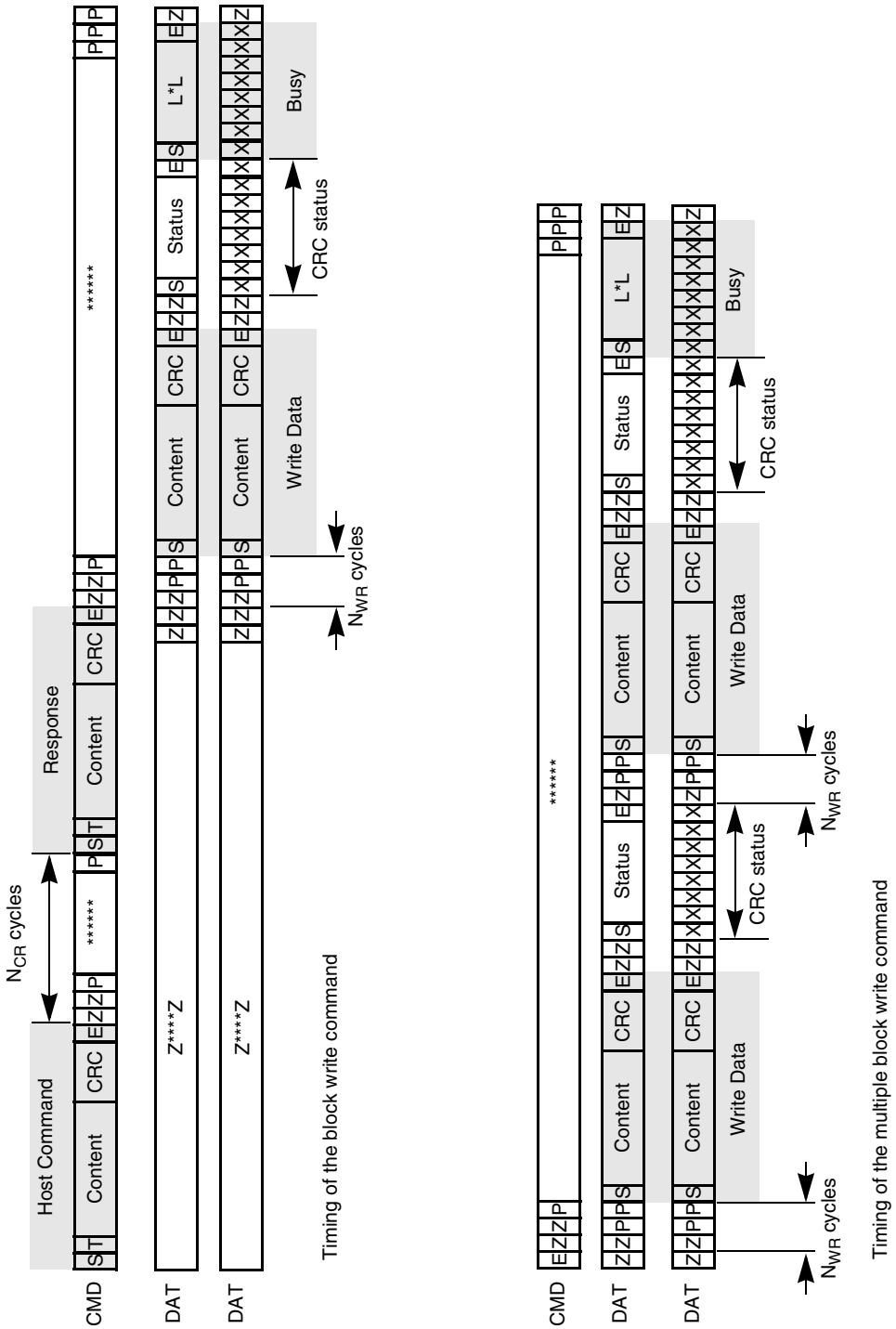


Figure 51. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 52 shows the different scenarios on the bus.

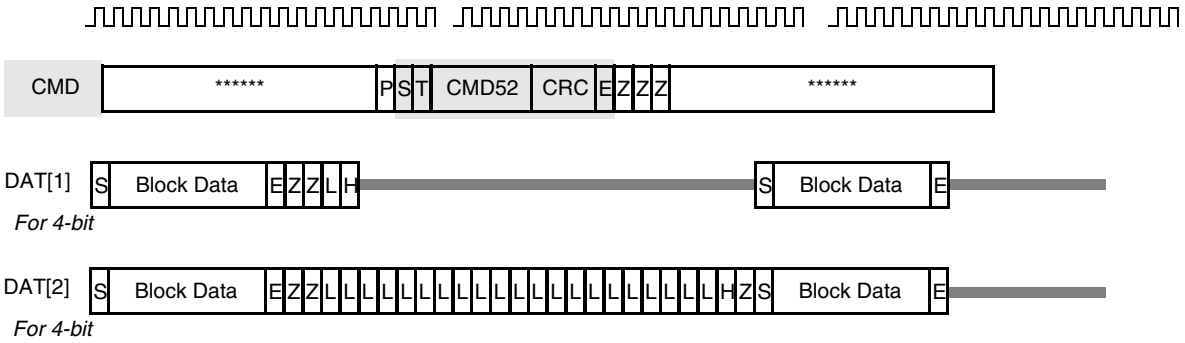


Figure 54. SDIO ReadWait Timing Diagram

4.11 Memory Stick Host Controller

The Memory Stick protocol requires three interface signal line connections for data transfers: MS_BS, MS_SDIO, and MS_SCLKO. Communication is always initiated by the MSHC and operates the bus in either four-state or two-state access mode.

The MS_BS signal classifies data on the SDIO into one of four states (BS0, BS1, BS2, or BS3) according to its attribute and transfer direction. BS0 is the INT transfer state, and during this state no packet transmissions occur. During the BS1, BS2, and BS3 states, packet communications are executed. The BS1, BS2, and BS3 states are regarded as one packet length and one communication transfer is always completed within one packet length (in four-state access mode).

The Memory Stick usually operates in four state access mode and in BS1, BS2, and BS3 bus states. When an error occurs during packet communication, the mode is shifted to two-state access mode, and the BS0 and BS1 bus states are automatically repeated to avoid a bus collision on the SDIO.

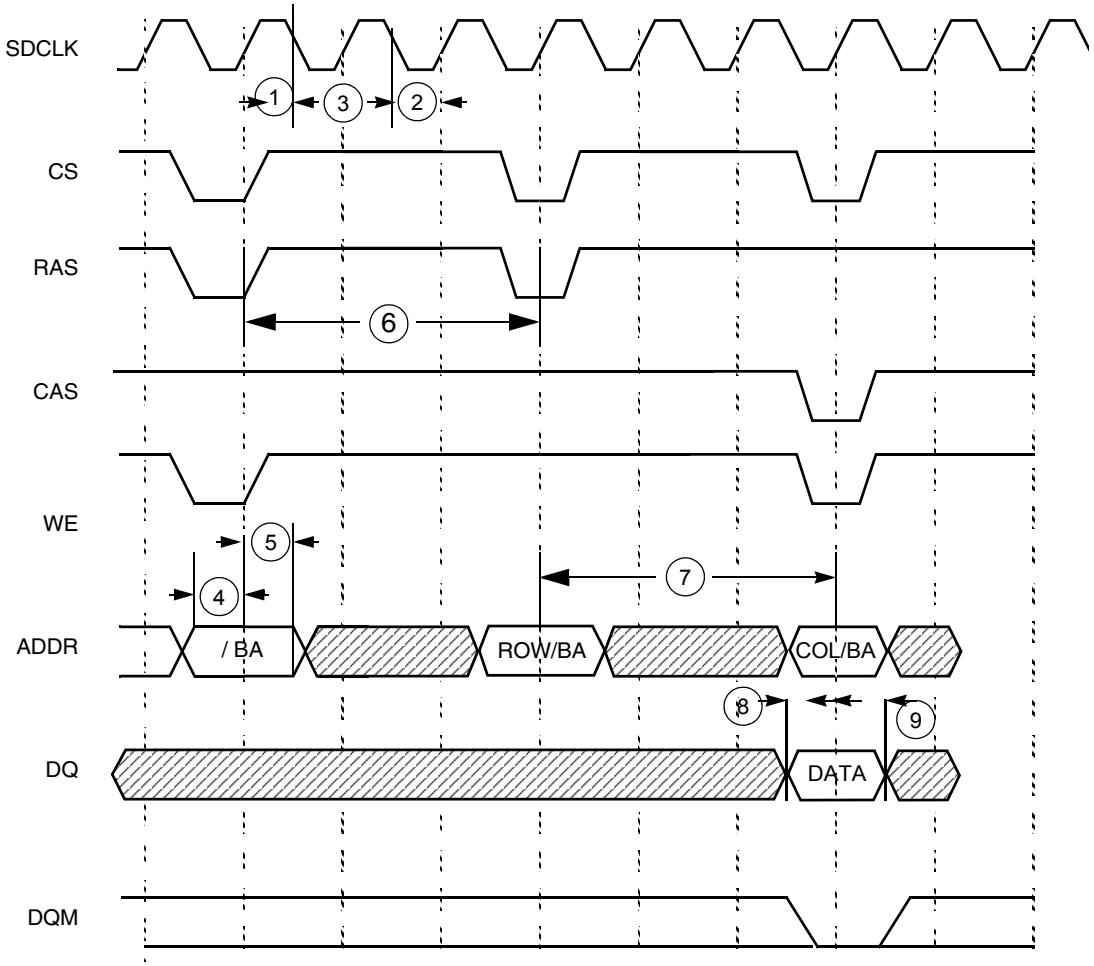


Figure 58. SDRAM Write Cycle Timing Diagram

Table 34. SDRAM Write Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period[1]	t_{RP}[2]	–	t_{RP2}	–	ns
7	Active to read/write command delay	t_{RCD2}	–	t_{RCD2}	–	ns
8	Data setup time	4.0	–	2	–	ns
9	Data hold time	2.28	–	2	–	ns

1 Precharge cycle timing is included in the write timing diagram.

2 t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the *MC9328MX1 reference manual*.

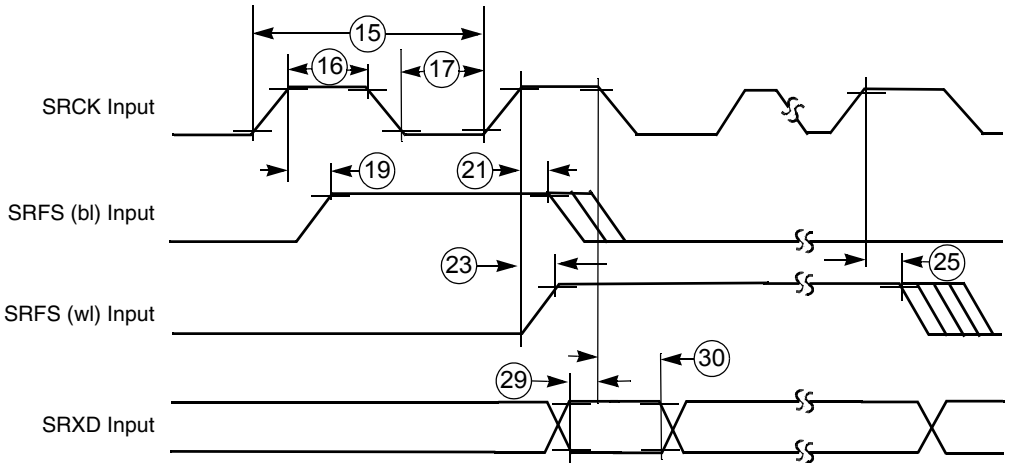


Figure 67. SSI Receiver External Clock Timing Diagram

Table 39. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Primary Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.5	4.5	1.3	3.9	ns
3	SRCK high to SRFS (bl) high[3]	-1.2	-1.7	-1.1	-1.5	ns
4	STCK high to STFS (bl) low[3]	2.5	4.3	2.2	3.8	ns
5	SRCK high to SRFS (bl) low[3]	0.1	-0.8	0.1	-0.8	ns
6	STCK high to STFS (wl) high[3]	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high[3]	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low[3]	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low[3]	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	–	18.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Primary Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns

Table 39. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function[2])						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port C Primary Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1 All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

2 There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

3 bl = bit length; wl = word length.

Table 40. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port B Alternate Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port B Alternate Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns

5 Pin-Out and Package Information

Table 44 illustrates the package pin assignments for the 256-pin MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 11.

Table 44. i.MX1 256 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NVSS	SD_DAT3	SD_CLK	NVSS	USBD_ AFE	NVDD4	NVSS	UART1_ RTS	UART1_ RXD	NVDD3	BT5	BT3	QVDD4	RVP	UIP	N.C.	A
B	A24	SD_DAT1	SD_CMD	SIM_TX	USBD_ ROE	USBD_VP	SSI_RXCLK	SSI_TXCLK	SPI1_ SCLK	BT11	BT7	BT1	QVSS	RVM	UIN	N.C.	B
C	A23	D31	SD_DAT0	SIM_PD	USBD_ RCV	UART2_ CTS	UART2_ RXD	SSI_ RXFS	UART1_ TXD	BTRFGND	BT8	BTRFVDD	N.C.	AVDD2[1]	VSS	R1B	C
D	A22	D30	D29	SIM_SVEN	USBD_ SUSPND	USBD_ VPO	USBD_ VMO	SSI_RXDAT	SPI1_ SPI_RDY	BT13	BT6	N.C.	N.C.	N.C.	R1A	R2B	D
E	A20	A21	D28	D26	SD_DAT2	USBD_VM	UART2_ RTS	SSI_TXDAT	SPI1_SS	BT12	BT4	N.C.	N.C.	PY2	PX2	R2A	E
F	A18	D27	D25	A19	A16	SIM_RST	UART2_ TXD	SSI_TXFS	SPI1_ MISO	BT10	BT2	REV	PY1	PX1	LSCLK	SPL_SPR	F
G	A15	A17	D24	D23	D21	SIM_RX	SIM_CLK	UART1_ CTS	SPI1_ MOSI	BT9	CLS	CONTRAST	ACD/OE	LP/ HSYNC	FLM/ VSYNC	LD1	G
H	A13	D22	A14	D20	NVDD1	NVDD1	NVSS	QVSS	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3	H
J	A12	A11	D18	D19	NVDD1	NVDD1	NVSS	NVDD1	NVSS	NVSS	LD6	LD7	LD8	LD11	QVDD3	QVSS	J
K	A10	D16	A9	D17	NVDD1	NVSS	NVSS	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TMR2OUT	LD15	K
L	A8	A7	D13	D15	D14	NVDD1	NVSS	CAS	TCK	TIN	PWMO	CSI_MCLK	CSI_D0	CSI_D1	CSI_D2	CSI_D3	L
M	A5	D12	D11	A6	SDCLK	NVSS	RW	MA10	RAS	RESET_IN	BIG_ ENDIAN	CSI_D4	CSI_ HSYNC	CSI_VSYNC	CSI_D6	CSI_D5	M
N	A4	EB1	D10	D7	A0	D4	PA17	D1	DQM1	RESET_SF[2]	RESET_ OUT	BOOT2	CSI_ PIXCLK	CSI_D7	TMS	TDI	N
P	A3	D9	EB0	CS3	D6	ECB	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	TRST	I2C_SCL	I2C_SDA	XTAL32K	P
R	EB2	EB3	A1	CS4	D8	D5	LBA	BCLK[3]	D0	DQM0	SDCKE0	POR	BOOT1	TDO	QVDD2	EXTAL32K	R
T	NVSS	A2	OE	CS5	CS2	CS1	CS0	MA11	DQM2	SDWE	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	QVSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

1 ASP signals are clamped by AVDD2 to prevent ESD (Electrostatic Discharge) damage. AVDD2 must be greater than QVDD to keep diodes reversed-biased.

2 This signal is not used and should be floated in an actual application.

3 burst clock

NOTES

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Document Number: MC9328MX1
Rev. 7
12/2006