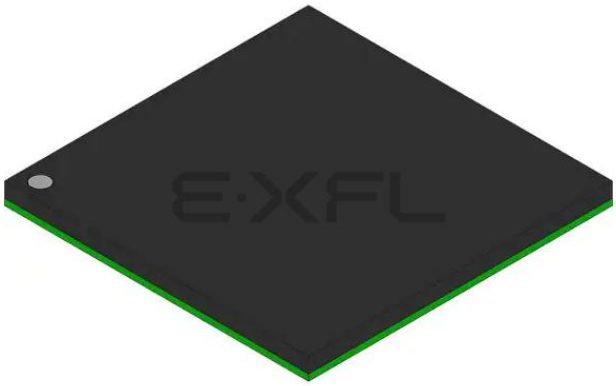

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx1dvh20

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
BT4	Input
BT5	Output
BT6	Output
BT7	Output
BT8	Output
BT9	Output
BT10	Output
BT11	Output
BT12	Output
BT13	Output
BTRF VDD	Power supply from external BT RFIC
BTRF GND	Ground from external BT RFIC
Test Function	
TRISTATE	Forces all I/O signals to high impedance for test purposes. For normal operation, terminate this input with a 1 k ohm resistor to ground. (TRI-STATE® is a registered trademark of National Semiconductor.)
Digital Supply Pins	
NVDD	Digital Supply for the I/O pins
NVSS	Digital Ground for the I/O pins
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Ground pins for silicon internal circuitry

2.1 I/O Pads Power Supply and Signal Multiplexing Scheme

This section describes detailed information about both the power supply for each I/O pin and its function multiplexing scheme. The user can reference information provided in Table 6 on page 23 to configure the power supply scheme for each device in the system (memory and external peripherals). The function multiplexing information also shown in Table 6 allows the user to select the function of each pin by configuring the appropriate GPIO registers when those pins are multiplexed to provide different functions.

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	N1	A4	O									L	
NVDD1	M3	D11	I/O	69K								Pull-H	
NVDD1	P3	$\overline{EB0}$	O									H	
NVDD1	N3	D10	I/O	69K								Pull-H	
NVDD1	P1	A3	O									L	
NVDD1	N2	$\overline{EB1}$	O									H	
NVDD1	P2	D9	I/O	69K								Pull-H	
NVDD1	R1	$\overline{EB2}$	O									H	
	M6	VSS	Static										
NVDD1	H6	NVDD1	Static										
NVDD1	T2	A2	O									L	
NVDD1	R2	$\overline{EB3}$	O									H	
NVDD1	R5	D8	I/O	69K								Pull-H	
NVDD1	T3	$\overline{OE}$	O									H	
NVDD1	R3	A1	O									L	
NVDD1	T4	$\overline{CS5}$	O				PA23	69K				Pull-H	PA23
NVDD1	N4	D7	I/O	69K								Pull-H	
NVDD1	R4	$\overline{CS4}$	O				PA22	69K				Pull-H	PA22
NVDD1	N5	A0	O				PA21	69K				L	A0
NVDD1	P4	$\overline{CS3}$	O		$\overline{CSD1}$							H	$\overline{CSD1}$
NVDD1	P5	D6	I/O	69K								Pull-H	
NVDD1	T5	$\overline{CS2}$	O		$\overline{CSD0}$							H	$\overline{CSD0}$
	H7	VSS	Static										
NVDD1	J6	NVDD1	Static										
NVDD1	M5	SDCLK	O									H	

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD3	C9	UART1_TXD	O				PC11	69K				Pull-H	PC11
NVDD3	A8	$\overline{\text{UART1\_RTS}}$	I				PC10	69K				Pull-H	PC10
NVDD3	G8	$\overline{\text{UART1\_CTS}}$	O				PC9	69K				Pull-H	PC9
NVDD3	B8	SSI_TXCLK	I/O				PC8	69K				Pull-H	PC8
NVDD3	F8	SSI_TXFS	I/O				PC7	69K				Pull-H	PC7
NVDD3	E8	SSI_TXDAT	O				PC6	69K				Pull-H	PC6
NVDD3	D8	SSI_RXDAT	I				PC5	69K				Pull-H	PC5
NVDD3	B7	SSI_RXCLK	I/O				PC4	69K				Pull-H	PC4
NVDD3	C8	SSI_RXFS	I/O				PC3	69K				Pull-H	PC3
	A7	VSS	Static										
NVDD4	C7	UART2_RXD	I				PB31	69K				Pull-H	PB31
NVDD4	F7	UART2_TXD	O				PB30	69K				Pull-H	PB30
NVDD4	E7	$\overline{\text{UART2\_RTS}}$	I				PB29	69K				Pull-H	PB29
NVDD4	C6	$\overline{\text{UART2\_CTS}}$	O				PB28	69K				Pull-H	PB28
NVDD4	D7	USBD_VMO	O				PB27	69K				Pull-H	PB27
NVDD4	D6	USBD_VPO	O				PB26	69K				Pull-H	PB26
NVDD4	E6	USBD_VM	I				PB25	69K				Pull-H	PB25
NVDD4	B6	USBD_VP	I				PB24	69K				Pull-H	PB24
NVDD4	D5	USBD_SUSPND	O				PB23	69K				Pull-H	PB23
NVDD4	C5	USBD_RCV	I/O				PB22	69K				Pull-H	PB22
NVDD4	B5	$\overline{\text{USBD\_ROE}}$	O				PB21	69K				Pull-H	PB21
NVDD4	A5	USBD_AFE	O				PB20	69K				Pull-H	PB20
	A4	VSS	Static										
NVDD4	A6	NVDD4	Static										
NVDD4	G7	SIM_CLK	O		SSI_TXCLK	I/O	PB19	69K				Pull-H	PB19

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD4	F6	SIM_RST	O		SSI_TXFS	I/O	PB18	69K				Pull-H	PB18
NVDD4	G6	SIM_RX	I		SSI_TXDAT	O	PB17	69K				Pull-H	PB17
NVDD4	B4	SIM_TX	I/O		SSI_RXDAT	I	PB16	69K				Pull-H	PB16
NVDD4	C4	SIM_PD	I		SSI_RXCLK	I/O	PB15	69K				Pull-H	PB15
NVDD4	D4	SIM_SVEN	O		SSI_RXFS	I/O	PB14	69K				Pull-H	PB14
NVDD4	B3	SD_CMD	I/O		MS_BS	O	PB13	69K				Pull-H	PB13
NVDD4	A3	SD_CLK	O		MS_SCLKO	O	PB12	69K				Pull-H	PB12
NVDD4	A2	SD_DAT3	I/O		MS_SDIO	I/O	PB11	69K (pull down)				Pull-L	PB11
NVDD4	E5	SD_DAT2	I/O		MS_SCLKI	I	PB10	69K				Pull-H	PB10
NVDD4	B2	SD_DAT1	I/O		MS_PI1	I	PB9	69K				Pull-H	PB9
NVDD4	C3	SD_DAT0	I/O		MS_PI0	I	PB8	69K				Pull-H	PB8

1 After reset, $\overline{CS0}$ goes H/L depends on BOOT[3:0].

2 Need external circuitry to drive the signal.

3 Need external pull-up.

4 External resistor is needed.

5 Need external pull-up or pull-down.

6 ASP signals are clamped by AVDD2 to prevent ESD (electrostatic discharge) damage. AVDD2 must be greater than QVDD to keep diodes reverse-biased.

Table 6. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Min	Typical	Max	Unit
$Sidd_4$	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 55°C)	–	60	–	µA
V_{IH}	Input high voltage	$0.7V_{DD}$	–	Vdd+0.2	V
V_{IL}	Input low voltage	–	–	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	–	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	–	–	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	–	–	±1	µA
I_{IH}	Input high leakage current (V_{IN} = V_{DD}, no pull-up or pull-down)	–	–	±1	µA
I_{OH}	Output high current (V_{OH} = $0.8V_{DD}$, V_{DD} = 1.8V)	4.0	–	–	mA
I_{OL}	Output low current (V_{OL} = 0.4V, V_{DD} = 1.8V)	-4.0	–	–	mA
I_{OZ}	Output leakage current (V_{out} = V_{DD}, output is high impedance)	–	–	±5	µA
C_i	Input capacitance	–	–	5	pF
C_o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 8. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms

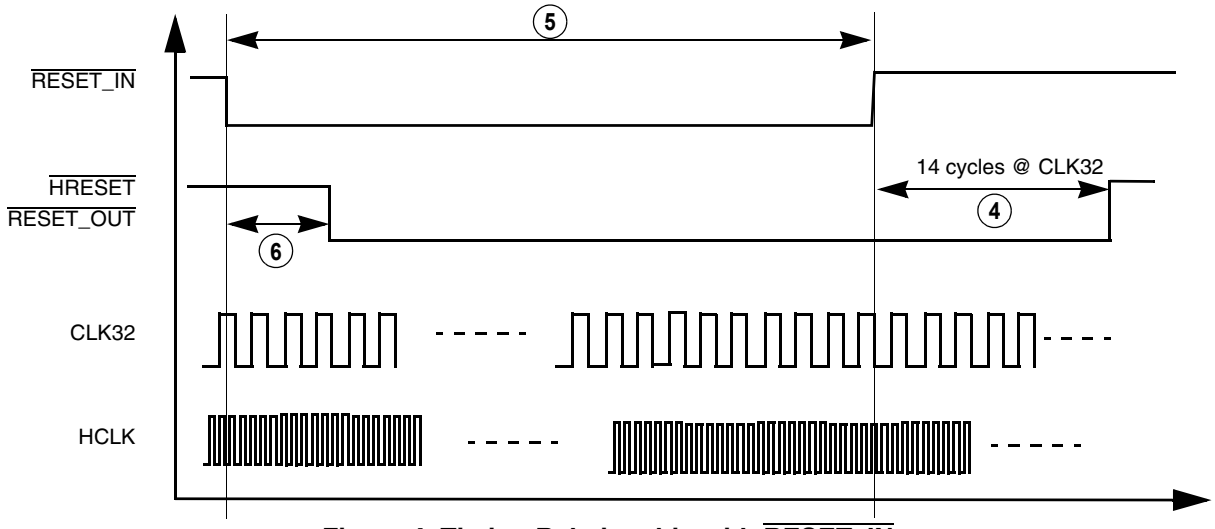


Figure 4. Timing Relationship with RESET_IN

Table 11. Reset Module Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	note[1]	–	note[1]	–	–
2	Width of internal POWER_ON_RESET (9600 *CLK32 at 32 kHz)	300	300	300	300	ms
3	7K to 32K-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14K to 32K-cycle stretcher for internal system reset HRESERT and output reset at pin RESET_OUT	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset RESET_IN	4	–	4	–	Cycles of CLK32
6	4K to 32K-cycle qualifier	4	4	4	4	Cycles of CLK32

[1] POR width is dependent on the 32 or 32.768 kHz crystal oscillator start-up time. Design margin should allow for crystal tolerance, i.MX chip variations, temperature impact, and supply voltage influence. Through the process of supplying crystals for use with CMOS oscillators, crystal manufacturers have developed a working knowledge of start-up time of their crystals. Typically, start-up times range from 400 ms to 1.2 seconds for this type of crystal.
If an external stable clock source (already running) is used instead of a crystal, the width of POR should be ignored in calculating timing for the start-up process.

4.4 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the i.MX1 processor, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
7	Wait asserted to $\overline{RW}$ negated	1T+2.15	2T+7.34	ns
8	Data hold timing after $\overline{RW}$ negated	2.5T-1.18	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{EB}$ negated after $\overline{CS5}$ is negated	1.5T+0.74	1.5T+2.35	ns
11	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion can also be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.2.4 WAIT Write Cycle DMA Enabled

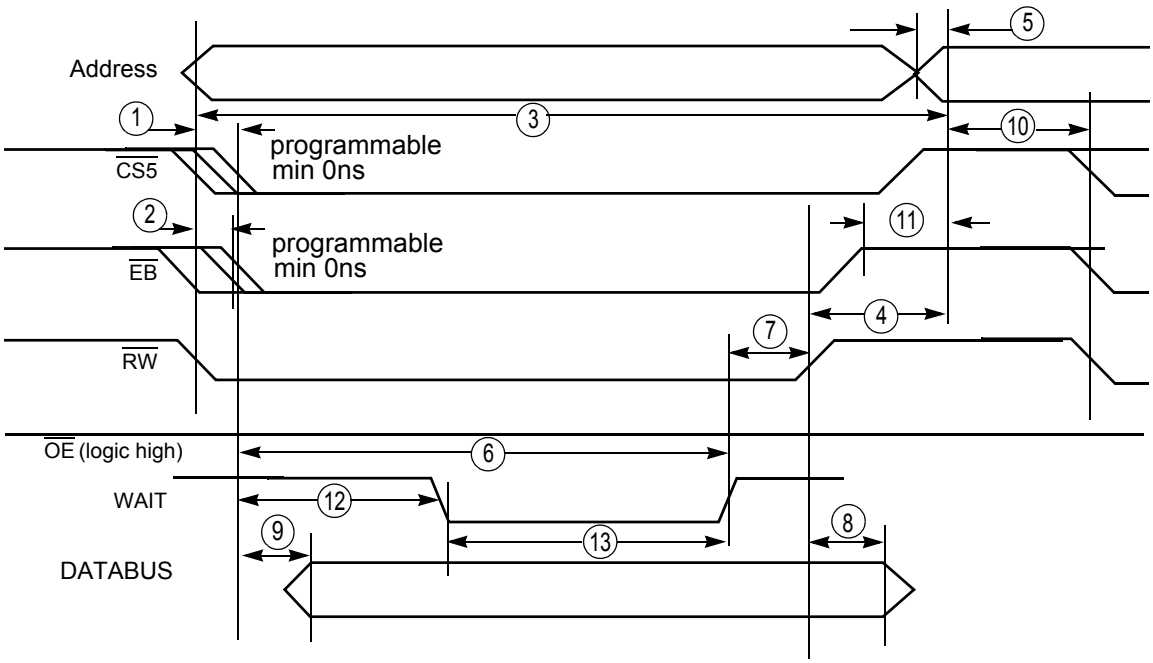
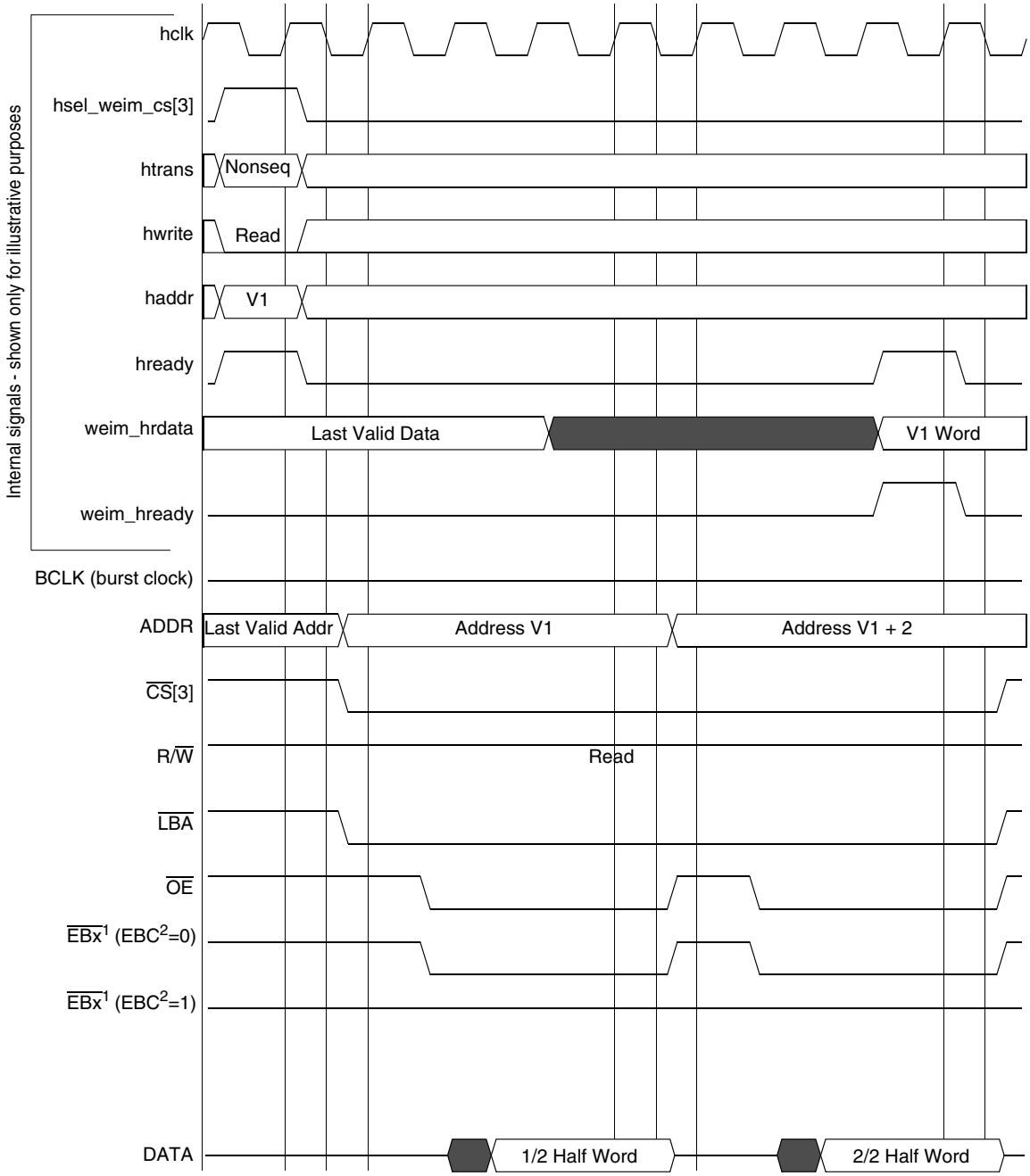
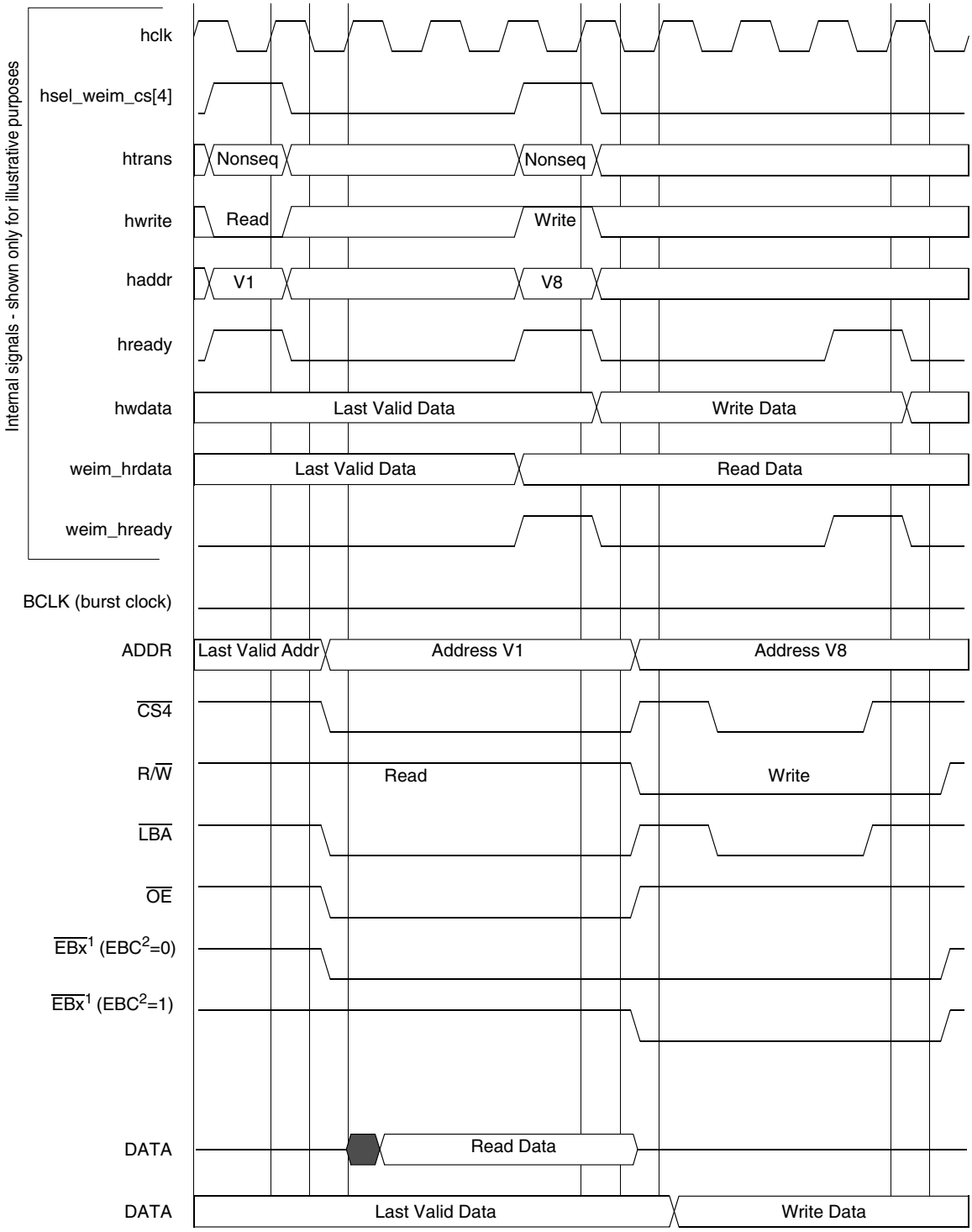


Figure 9. WAIT Write Cycle DMA Enabled



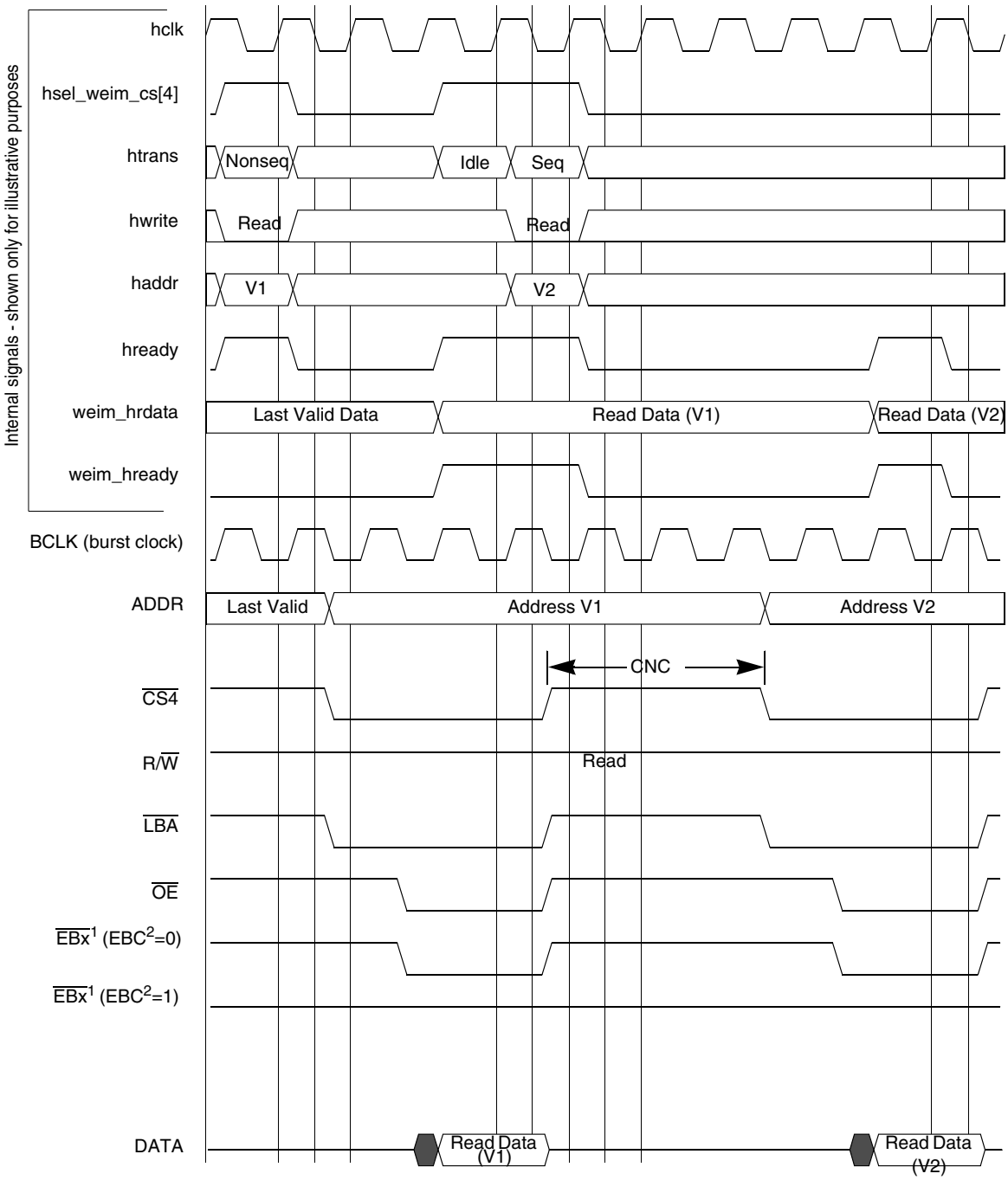
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 25. WSC = 3, CSA = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF

4.4.4 Non-TFT Panel Timing

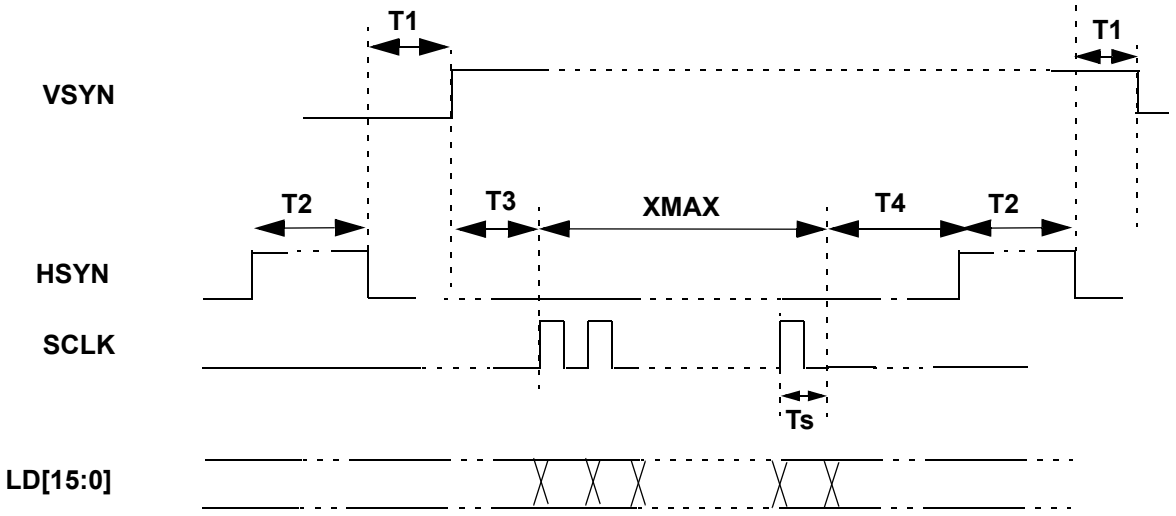


Figure 33. Non-TFT Panel Timing

Table 17. Non TFT Panel Timing Diagram

Symbol	Parameter	Allowed Register Minimum Value[1, 2]	Actual Value	Unit
T1	HSYN to VSYN delay[3]	0	HWAIT2+2	Tpix[4]
T2	HSYN pulse width	0	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	0 ≤ T3 ≤ Ts[5]	–
T4	SCLK to HSYN	0	HWAIT1+1	Tpix

1 Maximum frequency of LCDC_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.
2 Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.
3 VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.
4 Tpix is the pixel clock period which equals LCDC_CLK period * (PCD + 1).
5 Ts is the shift clock period. Ts = Tpix * (panel data bus width).

4.5 Pen ADC Specifications

The specifications for the pen ADC are shown in Table 18 through Table 20.

Table 18. Pen ADC System Performance

Full Range Resolution[1]	13 bits
Non-Linearity Error[1]	4 bits
Accuracy [1]	9 bits

1 Tested under input = 0~1.8V at 25°C

4.6.2 Gain Calculations

The ideal mapping of input voltage to output digital sample is defined as follows:

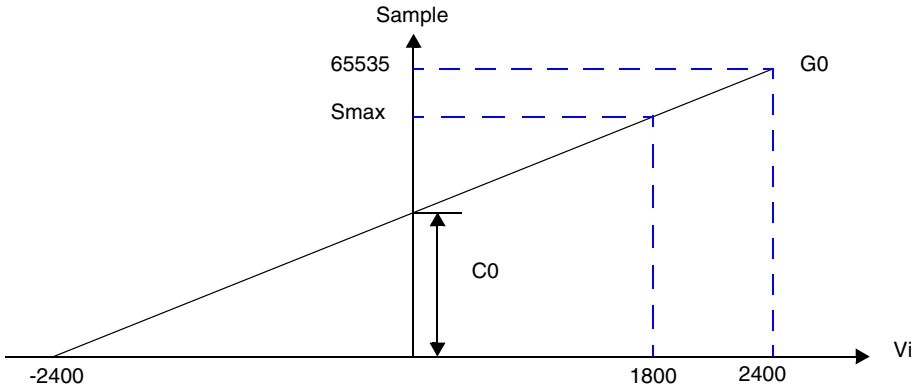


Figure 34. Gain Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

4.6.3 Offset Calculations

The ideal mapping of input voltage to output digital sample is defined as:

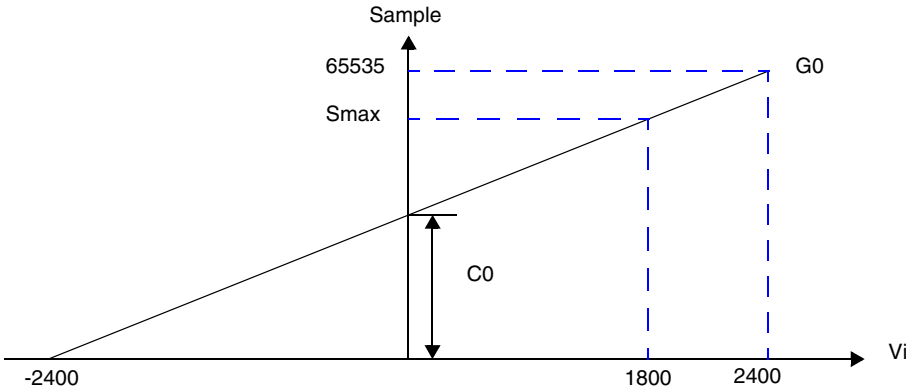


Figure 35. Offset Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

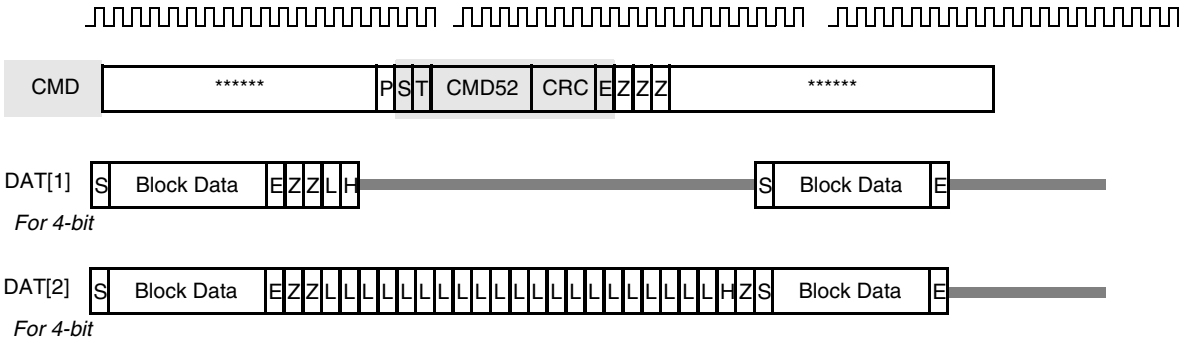


Figure 54. SDIO ReadWait Timing Diagram

4.11 Memory Stick Host Controller

The Memory Stick protocol requires three interface signal line connections for data transfers: MS_BS, MS_SDIO, and MS_SCLKO. Communication is always initiated by the MSHC and operates the bus in either four-state or two-state access mode.

The MS_BS signal classifies data on the SDIO into one of four states (BS0, BS1, BS2, or BS3) according to its attribute and transfer direction. BS0 is the INT transfer state, and during this state no packet transmissions occur. During the BS1, BS2, and BS3 states, packet communications are executed. The BS1, BS2, and BS3 states are regarded as one packet length and one communication transfer is always completed within one packet length (in four-state access mode).

The Memory Stick usually operates in four state access mode and in BS1, BS2, and BS3 bus states. When an error occurs during packet communication, the mode is shifted to two-state access mode, and the BS0 and BS1 bus states are automatically repeated to avoid a bus collision on the SDIO.

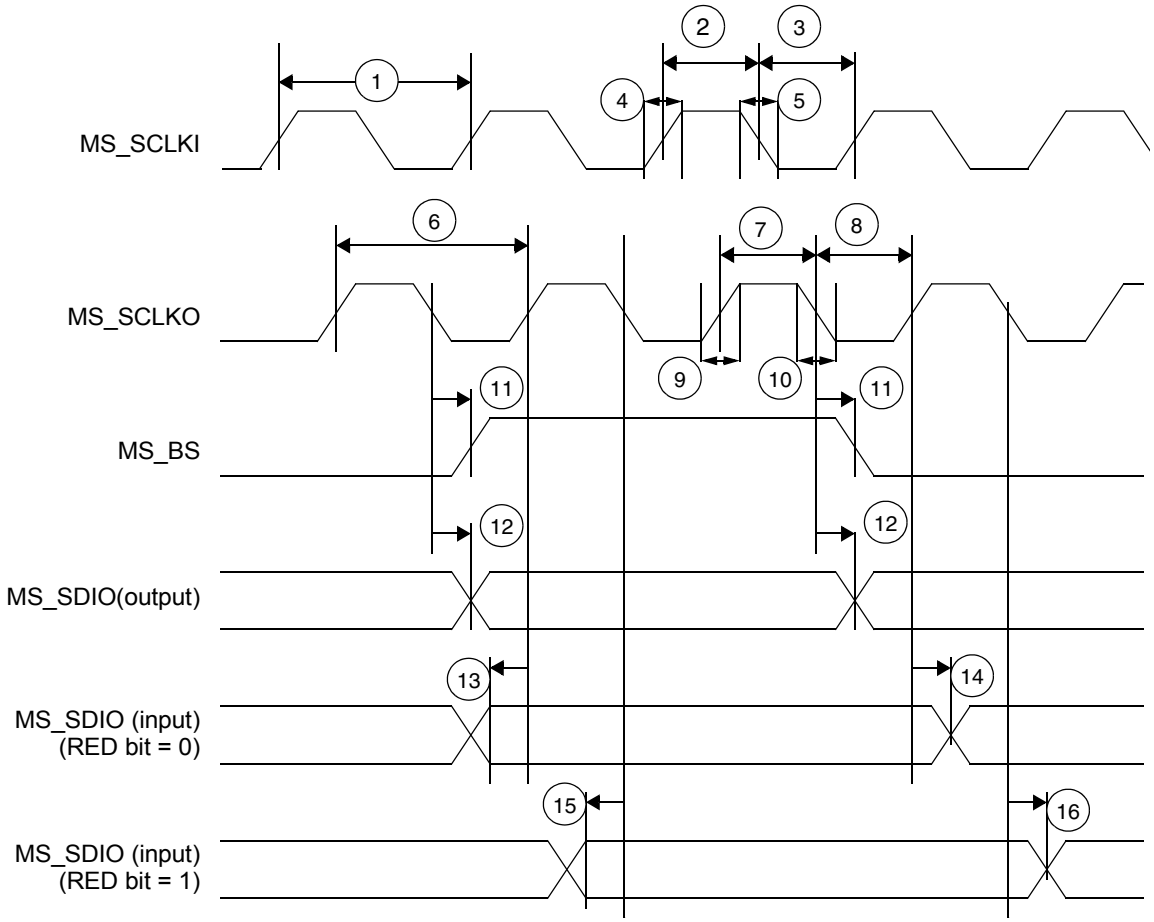


Figure 55. MSHC Signal Timing Diagram

Table 31. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	–	25	MHz
2	MS_SCLKI high pulse width	20	–	ns
3	MS_SCLKI low pulse width	20	–	ns
4	MS_SCLKI rise time	–	3	ns
5	MS_SCLKI fall time	–	3	ns
6	MS_SCLKO frequency[1]	–	25	MHz
7	MS_SCLKO high pulse width[1]	20	–	ns
8	MS_SCLKO low pulse width[1]	15	–	ns
9	MS_SCLKO rise time[1]	–	5	ns
10	MS_SCLKO fall time[1]	–	5	ns
11	MS_BS delay time[1]	–	3	ns

Table 31. MSHC Signal Timing Parameter Table (Continued)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	MS_SDIO output delay time[1,2]	–	3	ns
13	MS_SDIO input setup time for MS_SCLKO rising edge (RED bit = 0)[3]	18	–	ns
14	MS_SDIO input hold time for MS_SCLKO rising edge (RED bit = 0)[3]	0	–	ns
15	MS_SDIO input setup time for MS_SCLKO falling edge (RED bit = 1)[4]	23	–	ns
16	MS_SDIO input hold time for MS_SCLKO falling edge (RED bit = 1)[4]	0	–	ns

1 Loading capacitor condition is less than or equal to 30pF.

2 An external resistor (100 ~ 200 ohm) should be inserted in series to provide current control on the MS_SDIO pin, because of a possibility of signal conflict between the MS_SDIO pin and Memory Stick SDIO pin when the pin direction changes.

3 If the MSC2[RED] bit = 0, MSHC samples MS_SDIO input data at MS_SCLKO rising edge.

4 If the MSC2[RED] bit = 1, MSHC samples MS_SDIO input data at MS_SCLKO falling edge.

4.12 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in Figure 56 and the parameters are listed in Table 32.

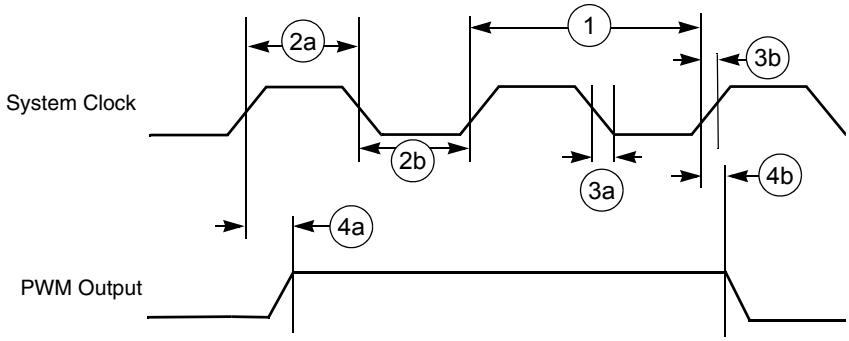


Figure 56. PWM Output Timing Diagram

Table 32. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency[1]	0	87	0	100	MHz
2a	Clock high time[1]	3.3	–	5/10	–	ns
2b	Clock low time[1]	7.5	–	5/10	–	ns
3a	Clock fall time[1]	–	5	–	5/10	ns

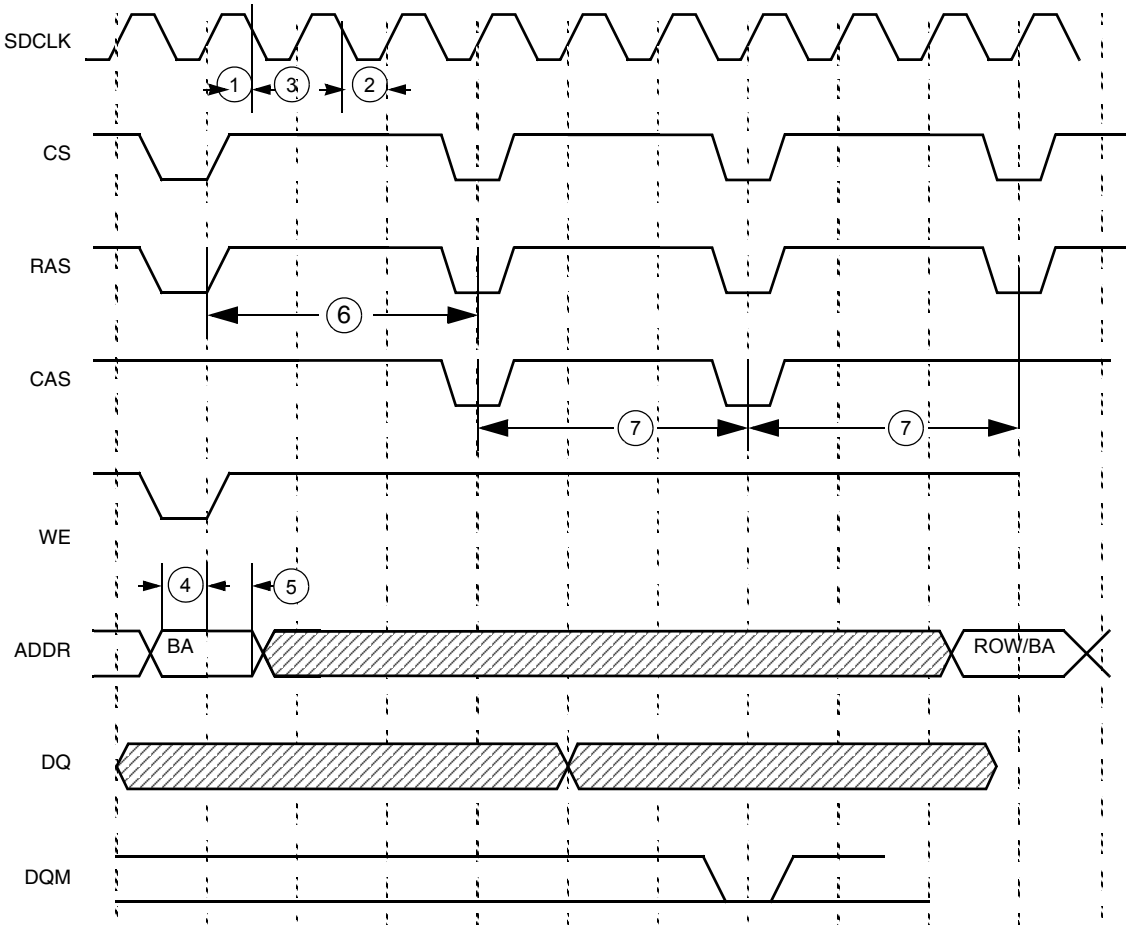


Figure 59. SDRAM Refresh Timing Diagram

Table 35. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP1}	–	ns
7	Auto precharge command period	t_{RC1}	–	t_{RC1}	–	ns

[1] t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *MC9328MX1 reference manual*.

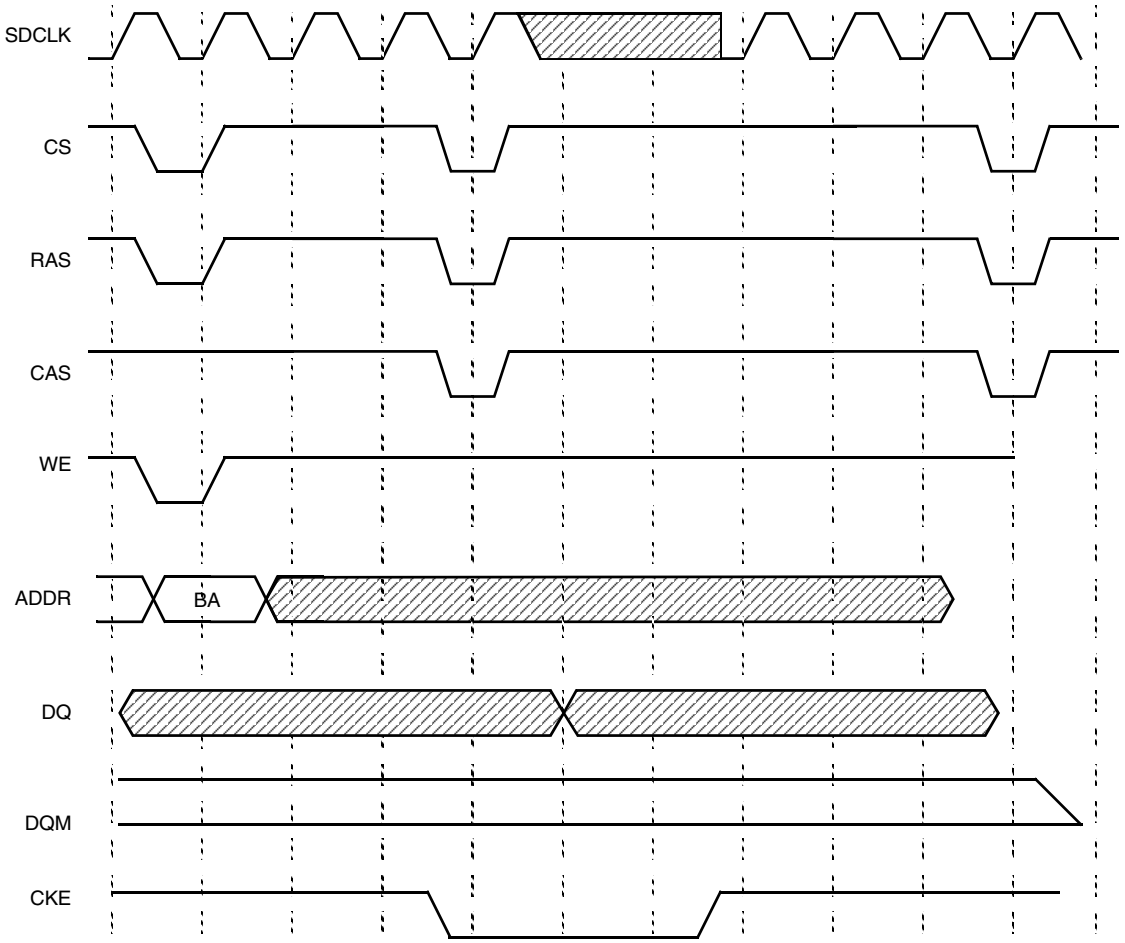


Figure 60. SDRAM Self-Refresh Cycle Timing Diagram

4.14 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers, and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

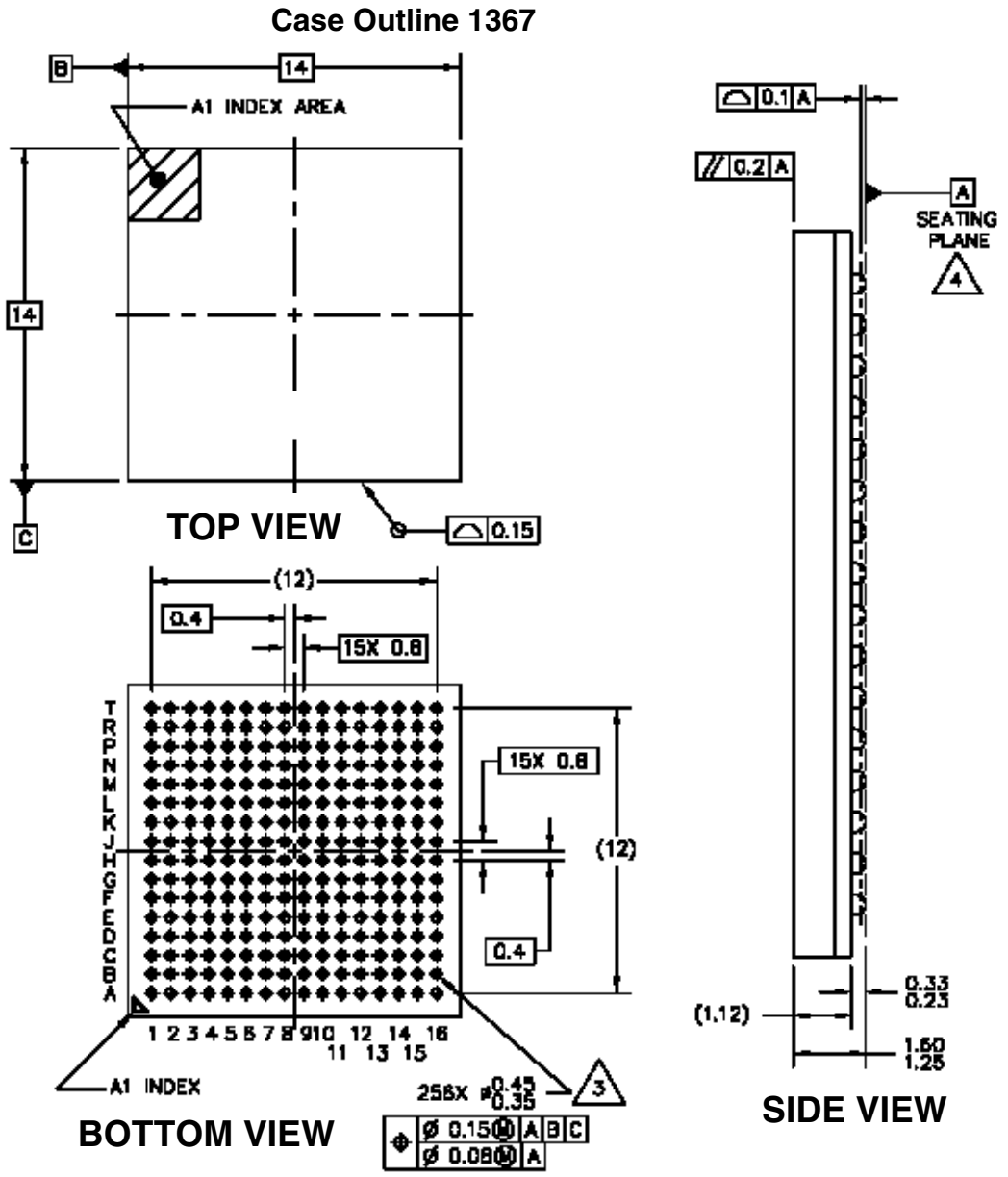
Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, however, because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

Table 40. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port B Alternate Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port B Alternate Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns

5.1 MAPBGA 256 Package Dimensions

Figure 72 illustrates the 256 MAPBGA 14 mm × 14 mm × 1.30 mm package, with an 0.8 mm pad pitch. The device designator for the MAPBGA package is VH.



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2.INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14 5M-1994.
3.MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 72. i.MXL 256 MAPBGA Mechanical Drawing

NOTES