Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx1dvm15r2

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SDIBA [3:0]	SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles.
DQM [3:0]	SDRAM data enable
$\overline{\text{CSD0}}$	SDRAM Chip-select signal which is multiplexed with the $\overline{\text{CS2}}$ signal. These two signals are selectable by programming the system control register.
$\overline{\text{CSD1}}$	SDRAM Chip-select signal which is multiplexed with $\overline{\text{CS3}}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{\text{CSD1}}$ is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins.
$\overline{\text{RAS}}$	SDRAM Row Address Select signal
$\overline{\text{CAS}}$	SDRAM Column Address Select signal
$\overline{\text{SDWE}}$	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
$\overline{\text{RESET\_SF}}$	Not Used
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 kHz crystal input
XTAL32K	32 kHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
$\overline{\text{RESET\_IN}}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
$\overline{\text{RESET\_OUT}}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{\text{RESET\_IN}}$), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{\text{TDO}}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	N1	A4	O									L	
NVDD1	M3	D11	I/O	69K								Pull-H	
NVDD1	P3	$\overline{EB0}$	O									H	
NVDD1	N3	D10	I/O	69K								Pull-H	
NVDD1	P1	A3	O									L	
NVDD1	N2	$\overline{EB1}$	O									H	
NVDD1	P2	D9	I/O	69K								Pull-H	
NVDD1	R1	$\overline{EB2}$	O									H	
	M6	VSS	Static										
NVDD1	H6	NVDD1	Static										
NVDD1	T2	A2	O									L	
NVDD1	R2	$\overline{EB3}$	O									H	
NVDD1	R5	D8	I/O	69K								Pull-H	
NVDD1	T3	$\overline{OE}$	O									H	
NVDD1	R3	A1	O									L	
NVDD1	T4	$\overline{CS5}$	O				PA23	69K				Pull-H	PA23
NVDD1	N4	D7	I/O	69K								Pull-H	
NVDD1	R4	$\overline{CS4}$	O				PA22	69K				Pull-H	PA22
NVDD1	N5	A0	O				PA21	69K				L	A0
NVDD1	P4	$\overline{CS3}$	O		$\overline{CSD1}$							H	$\overline{CSD1}$
NVDD1	P5	D6	I/O	69K								Pull-H	
NVDD1	T5	$\overline{CS2}$	O		$\overline{CSD0}$							H	$\overline{CSD0}$
	H7	VSS	Static										
NVDD1	J6	NVDD1	Static										
NVDD1	M5	SDCLK	O									H	

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	T6	$\overline{CS1}$	O									H	
NVDD1	T7	$\overline{CS0}$	O									H[1]	
NVDD1	R6	D5	I/O	69K								Pull-H	
NVDD1	P6	$\overline{ECB}$	I		ETMTRACEPKT7		PA20	69K				Pull-H	$\overline{ECB}$
NVDD1	N6	D4	I/O	69K								Pull-H	
NVDD1	R7	$\overline{LBA}$	O		ETMTRACEPKT6		PA19	69K				H	$\overline{LBA}$
NVDD1	P8	D3	I/O	69K								Pull-H	
NVDD1	R8	BCLK			ETMTRACEPKT5		PA18	69K				L	BCLK
NVDD1	P7	D2	I/O	69K								Pull-H	
	J7	VSS	Static										
NVDD1	L6	NVDD1	Static										
NVDD1	N7	DTACK	I		ETMTRACEPKT4		PA17	69K	SPI2_SS	A25		Pull-H	PA17
NVDD1	N8	D1	I/O	69K								Pull-H	
NVDD1	M7	$\overline{RW}$										H	
NVDD1	T8	MA11	O									L	
NVDD1	M8	MA10	O									L	
NVDD1	R9	D0	I/O	69K								Pull-H	
	K7	VSS	Static										
NVDD1	P9	DQM3	O									L	
NVDD1	T9	DQM2	O									L	
NVDD1	N9	DQM1	O									L	
NVDD1	R10	DQM0	O									L	
NVDD1	M9	$\overline{RAS}$	O									H	
NVDD1	L8	$\overline{CAS}$	O									H	
NVDD1	J8	NVDD1	Static										

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD3	C9	UART1_TXD	O				PC11	69K				Pull-H	PC11
NVDD3	A8	$\overline{\text{UART1\_RTS}}$	I				PC10	69K				Pull-H	PC10
NVDD3	G8	$\overline{\text{UART1\_CTS}}$	O				PC9	69K				Pull-H	PC9
NVDD3	B8	SSI_TXCLK	I/O				PC8	69K				Pull-H	PC8
NVDD3	F8	SSI_TXFS	I/O				PC7	69K				Pull-H	PC7
NVDD3	E8	SSI_TXDAT	O				PC6	69K				Pull-H	PC6
NVDD3	D8	SSI_RXDAT	I				PC5	69K				Pull-H	PC5
NVDD3	B7	SSI_RXCLK	I/O				PC4	69K				Pull-H	PC4
NVDD3	C8	SSI_RXFS	I/O				PC3	69K				Pull-H	PC3
	A7	VSS	Static										
NVDD4	C7	UART2_RXD	I				PB31	69K				Pull-H	PB31
NVDD4	F7	UART2_TXD	O				PB30	69K				Pull-H	PB30
NVDD4	E7	$\overline{\text{UART2\_RTS}}$	I				PB29	69K				Pull-H	PB29
NVDD4	C6	$\overline{\text{UART2\_CTS}}$	O				PB28	69K				Pull-H	PB28
NVDD4	D7	USBD_VMO	O				PB27	69K				Pull-H	PB27
NVDD4	D6	USBD_VPO	O				PB26	69K				Pull-H	PB26
NVDD4	E6	USBD_VM	I				PB25	69K				Pull-H	PB25
NVDD4	B6	USBD_VP	I				PB24	69K				Pull-H	PB24
NVDD4	D5	USBD_SUSPND	O				PB23	69K				Pull-H	PB23
NVDD4	C5	USBD_RCV	I/O				PB22	69K				Pull-H	PB22
NVDD4	B5	$\overline{\text{USBD\_ROE}}$	O				PB21	69K				Pull-H	PB21
NVDD4	A5	USBD_AFE	O				PB20	69K				Pull-H	PB20
	A4	VSS	Static										
NVDD4	A6	NVDD4	Static										
NVDD4	G7	SIM_CLK	O		SSI_TXCLK	I/O	PB19	69K				Pull-H	PB19

in the system, these Bluetooth pins can be used as general purpose I/O pins and BTRFVDD can be used as other NVDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 5. Recommended Operating Range

Symbol	Rating	Minimum	Maximum	Unit
T_A	Operating temperature range MC9328MX1VM20\MC9328MX1VM15	0	70	°C
T_A	Operating temperature range MC9328MX1DVM20\MC9328MX1DVM15	-30	70	°C
T_A	Operating temperature range MC9328MX1CVM15	-40	85	°C
NVDD	I/O supply voltage (if using MSHC, CSI, SPI, BTA, LCD, and USBd which are only 3 V interfaces)	2.70	3.30	V
NVDD	I/O supply voltage (if not using the peripherals listed above)	1.70	3.30	V
QVDD	Internal supply voltage (Core = 150 MHz)	1.70	1.90	V
QVDD	Internal supply voltage (Core = 200 MHz)	1.80	2.00	V
AVDD	Analog supply voltage	1.70	3.30	V

3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the “Power-Up Sequence” section of application note AN2537 on the i.MX applications processor website.

3.4 DC Electrical Characteristics

Table 6 contains both maximum and minimum DC characteristics of the i.MX1 processor.

Table 6. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Min	Typical	Max	Unit
Iop	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, MPEG4 decoding playback from external memory card to both external SSI audio decoder and driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	–	QVDD at 1.8V = 120mA; NVDD+AVDD at 3.0V = 30mA	–	mA
$Sidd_1$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 25°C)	–	25	–	µA
$Sidd_2$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 55°C)	–	45	–	µA
$Sidd_3$	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 25°C)	–	35	–	µA

4.4.2.1 WAIT Read Cycle without DMA

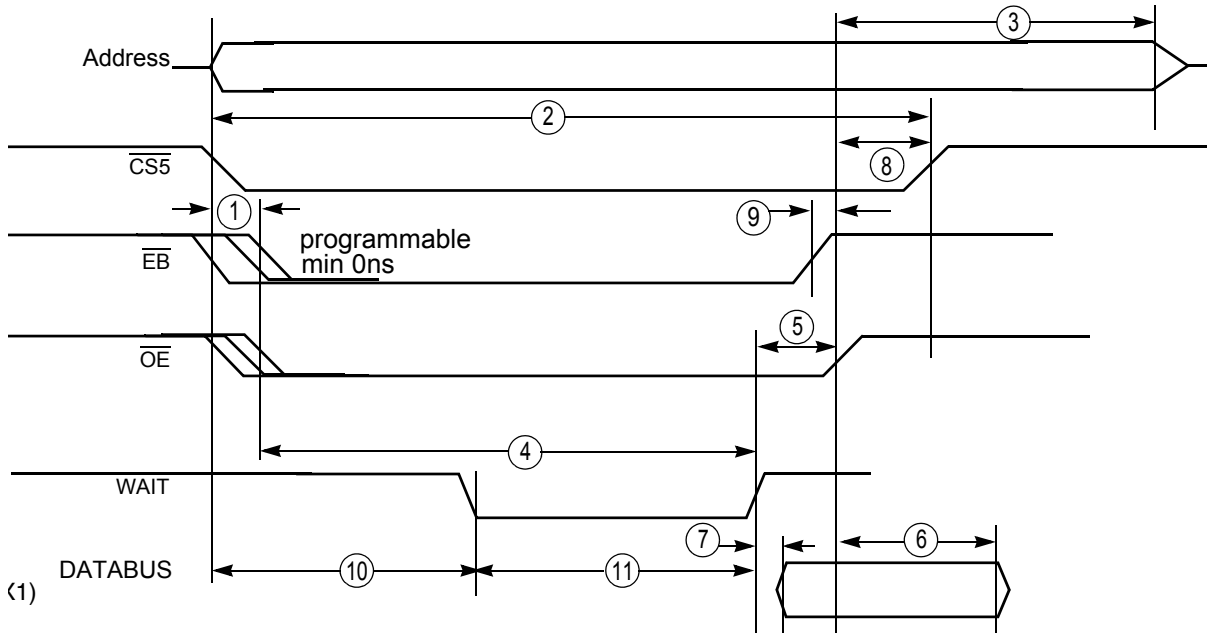


Figure 6. WAIT Read Cycle without DMA

Table 13. WAIT Read Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS5}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated to address inactive	56.81	–	ns
4	Wait asserted after $\overline{OE}$ asserted	–	1020T	ns
5	Wait asserted to $\overline{OE}$ negated	2T+2.2	3T+7.17	ns
6	Data hold timing after $\overline{OE}$ negated	T-1.86	–	ns
7	Data ready after wait asserted	0	T	ns
8	OE negated to CS negated	1.5T+0.24	1.5T+0.85	ns
9	OE negated after EB negated	0.5	1.5	ns
10	Become low after CS5 asserted	0	1019T	ns
11	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA

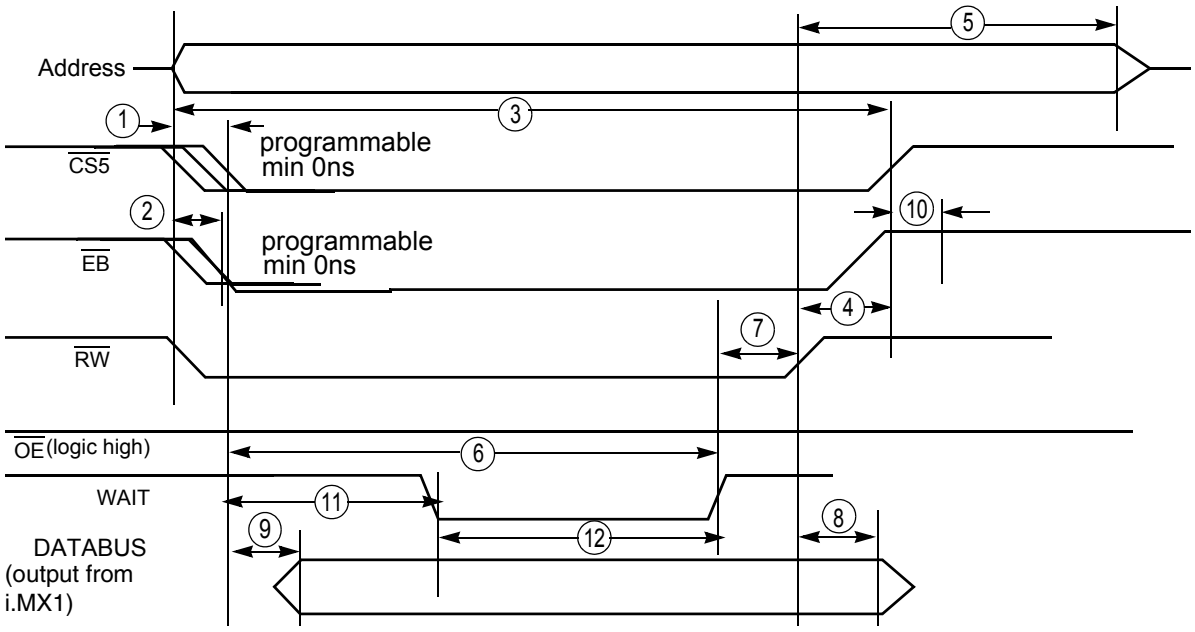


Figure 8. WAIT Write Cycle without DMA

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-0.29	2.5T+0.68	ns
5	$\overline{RW}$ negated to Address inactive	67.28	–	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns

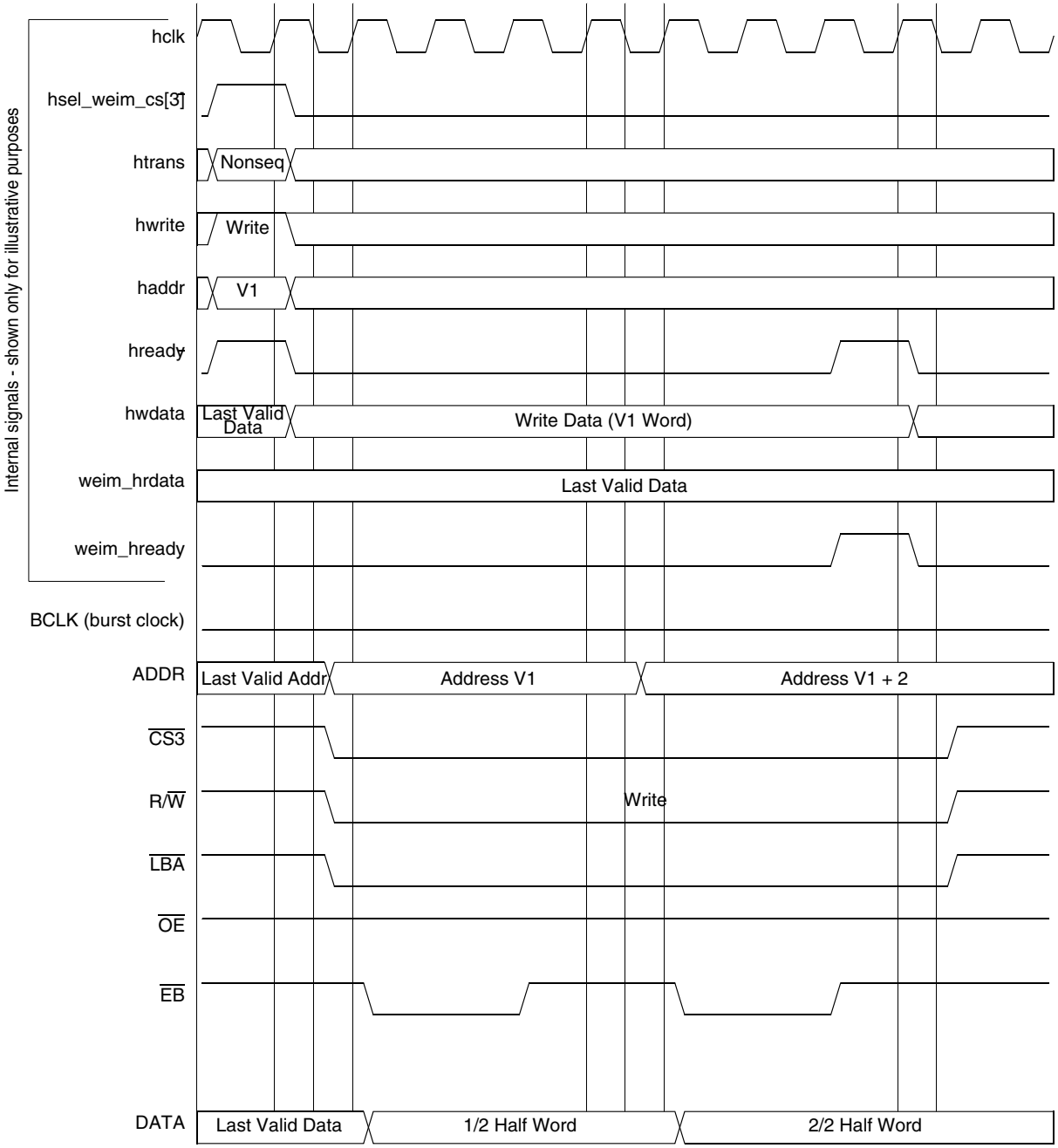
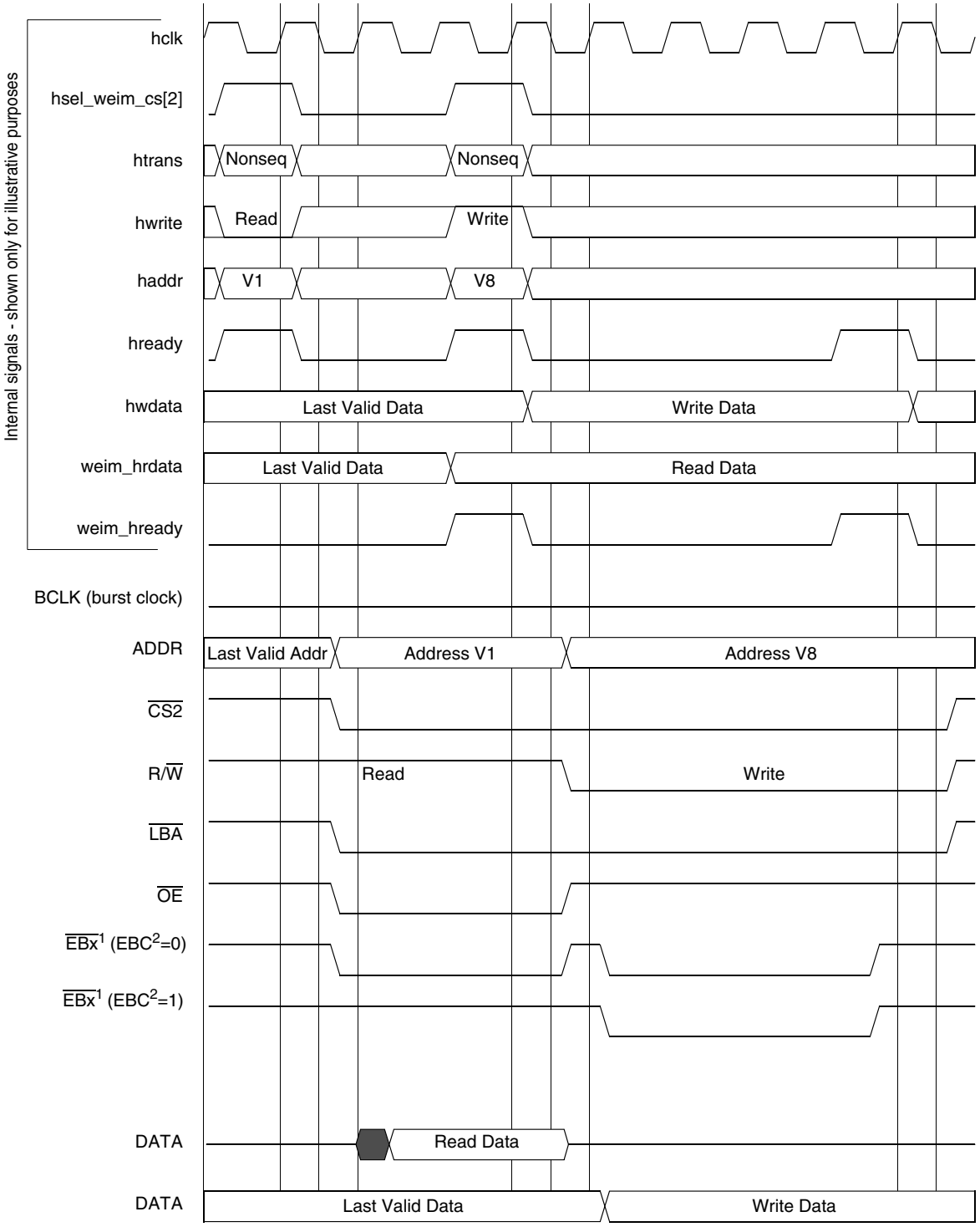
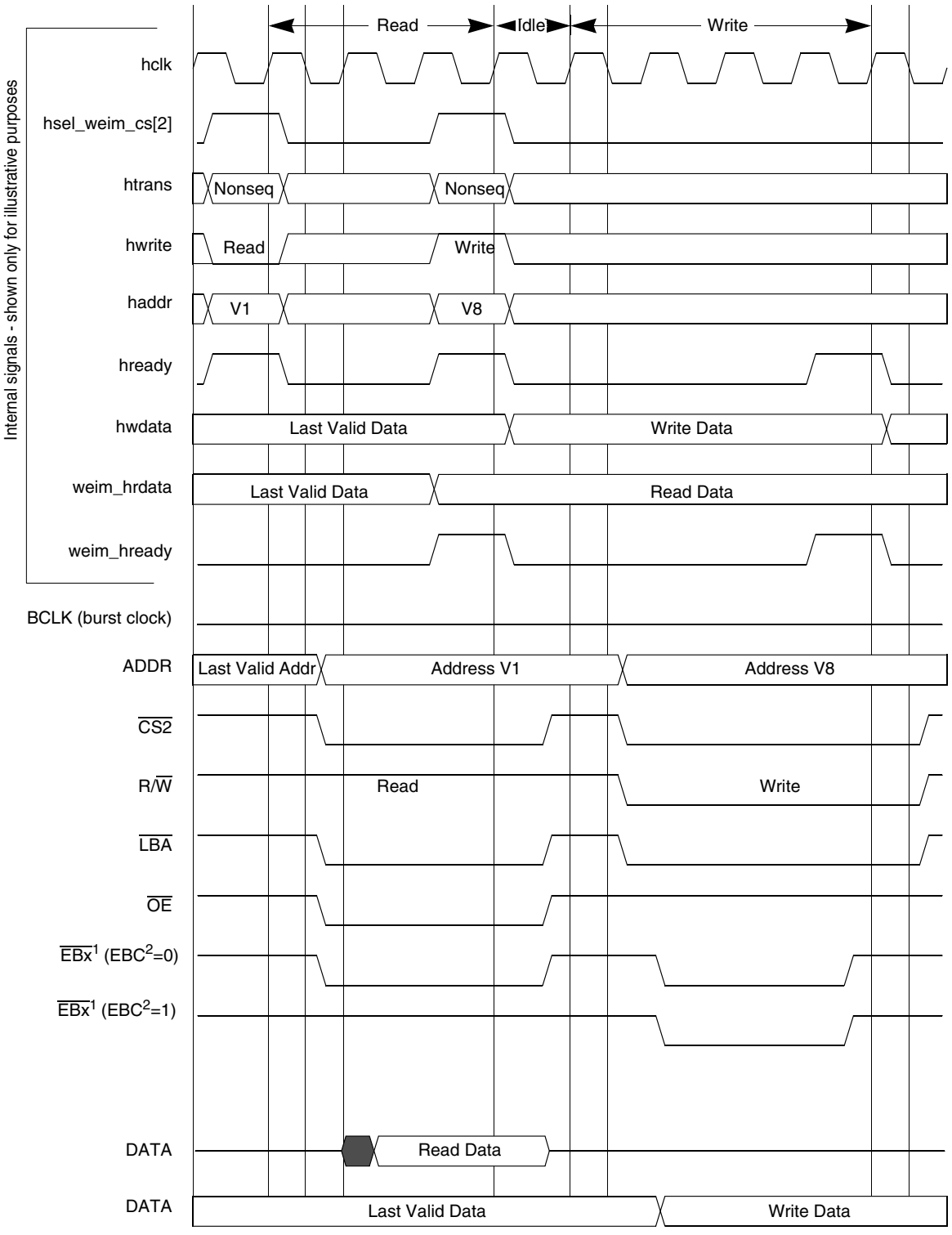


Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF



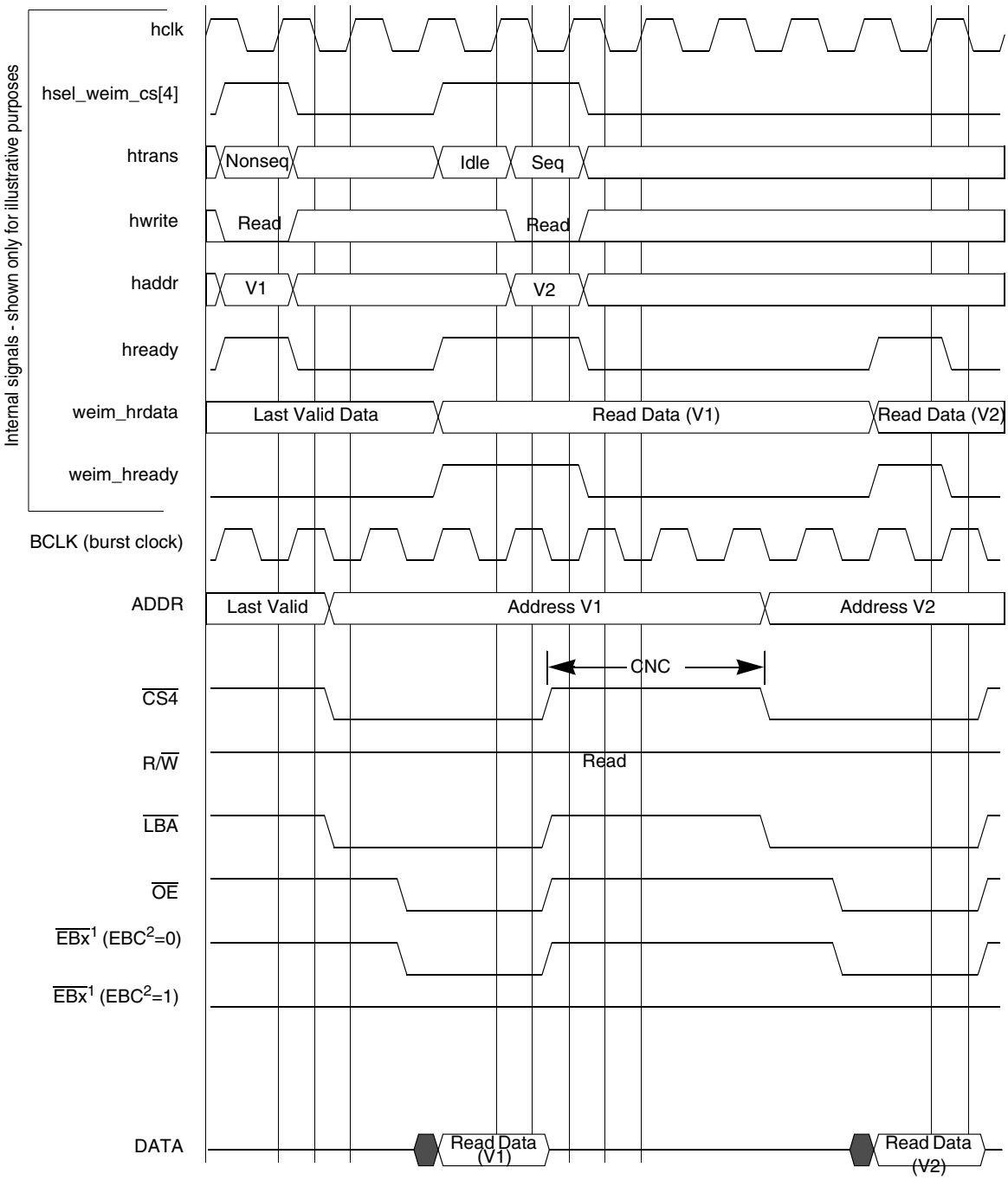
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 23. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF

4.6.2 Gain Calculations

The ideal mapping of input voltage to output digital sample is defined as follows:

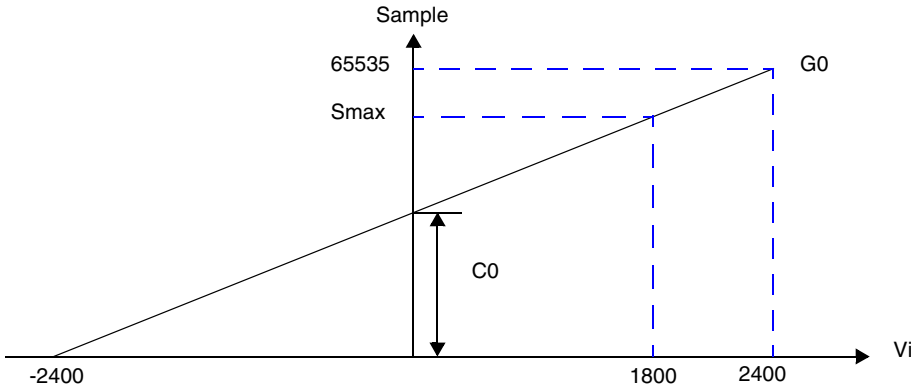


Figure 34. Gain Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

4.6.3 Offset Calculations

The ideal mapping of input voltage to output digital sample is defined as:

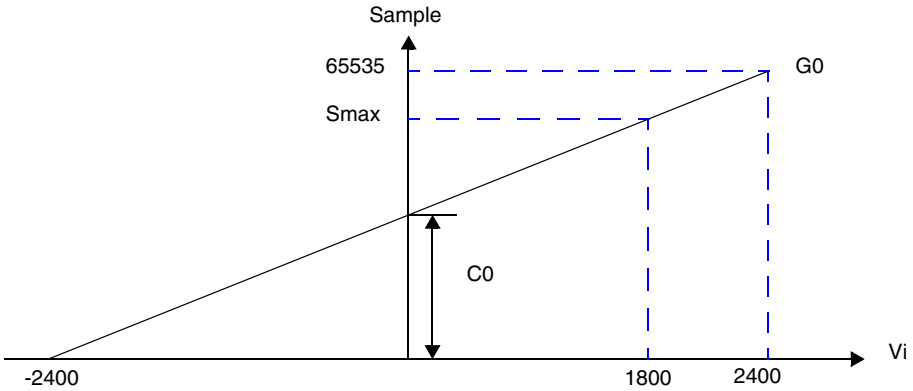


Figure 35. Offset Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

Table 24. Timing Parameter Table for Figure 39 through Figure 43

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low	2T[1]	–	ns
2	$\overline{\text{SS}}$ output low to first SCLK edge	3 • Tsclk[2]	–	ns
3	Last SCLK edge to $\overline{\text{SS}}$ output high	2 • Tsclk	–	ns
4	$\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low	0	–	ns
5	$\overline{\text{SS}}$ output pulse width	Tsclk + WAIT [3]	–	ns
6	$\overline{\text{SS}}$ input low to first SCLK edge	T	–	ns
7	$\overline{\text{SS}}$ input pulse width	T	–	ns

1 T = CSPI system clock period (PERCLK2).

2 Tsclk = Period of SCLK.

3 WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

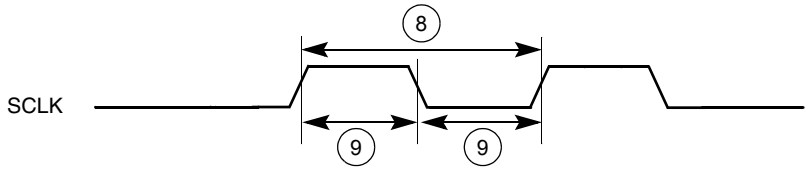


Figure 44. SPI SCLK Timing Diagram

Table 25. Timing Parameter Table for SPI SCLK

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
8	SCLK frequency	0	10	MHz
9	SCLK pulse width	100	–	ns

4.9 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *MC9328MX1 Reference Manual*.

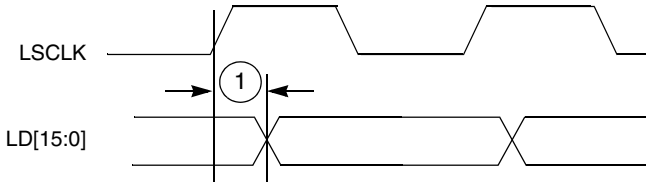


Figure 45. SCLK to LD Timing Diagram

Table 28. SDHC Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency at Data transfer Mode (PP)[1]—10/30 cards	0	25/5	0	25/5	MHz
2	CLK frequency at Identification Mode[2]	0	400	0	400	kHz
3a	Clock high time[1]—10/30 cards	6/33	–	10/50	–	ns
3b	Clock low time[1]—10/30 cards	15/75	–	10/50	–	ns
4a	Clock fall time[1]—10/30 cards	–	10/50 (5.00)[3]	–	10/50	ns
4b	Clock rise time[1]—10/30 cards	–	14/67 (6.67)[3]	–	10/50	ns
5a	Input hold time[3]—10/30 cards	10.3/10.3	–	9/9	–	ns
5b	Input setup time[3]—10/30 cards	10.3/10.3	–	9/9	–	ns
6a	Output hold time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
6b	Output setup time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
7	Output delay time[3]	0	16	0	14	ns

1 $C_L \leq 100$ pF / 250 pF (10/30 cards)
2 $C_L \leq 250$ pF (21 cards)
3 $C_L \leq 25$ pF (1 card)

4.10.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is NCR clock cycles as illustrated in Figure 48. The symbols for Figure 48 through Figure 52 are defined in Table 29.

Table 29. State Signal Parameters for Figure 48 through Figure 52

Card Active		Host Active	
Symbol	Definition	Symbol	Definition
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)

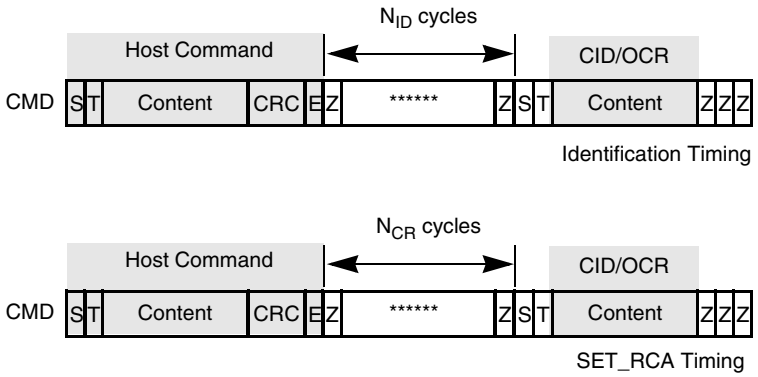


Figure 48. Timing Diagrams at Identification Mode

After a card receives its RCA, it switches to data transfer mode. As shown on the first diagram in Figure 49, SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods N_{RC} and N_{CC}.

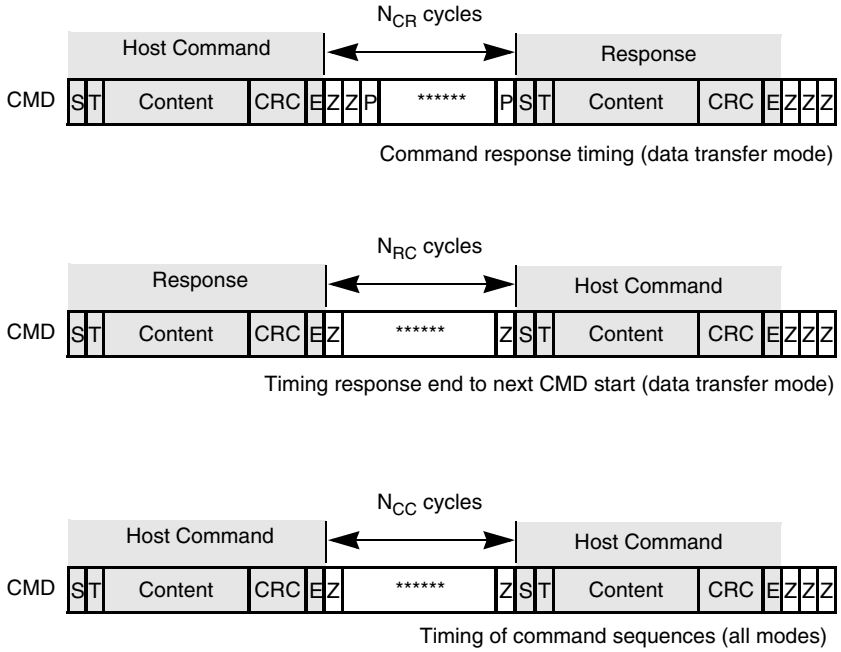


Figure 49. Timing Diagrams at Data Transfer Mode

Figure 50 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC}, beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

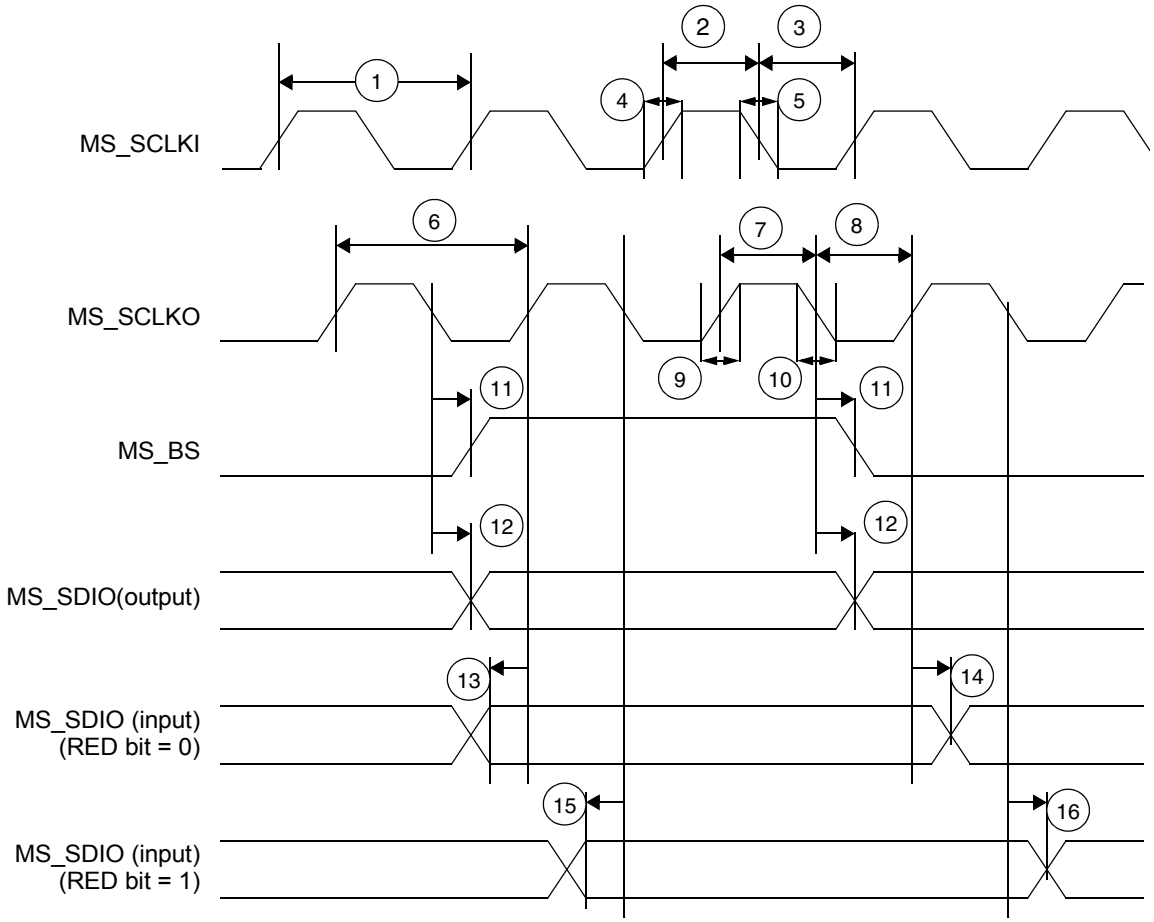


Figure 55. MSHC Signal Timing Diagram

Table 31. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	–	25	MHz
2	MS_SCLKI high pulse width	20	–	ns
3	MS_SCLKI low pulse width	20	–	ns
4	MS_SCLKI rise time	–	3	ns
5	MS_SCLKI fall time	–	3	ns
6	MS_SCLKO frequency[1]	–	25	MHz
7	MS_SCLKO high pulse width[1]	20	–	ns
8	MS_SCLKO low pulse width[1]	15	–	ns
9	MS_SCLKO rise time[1]	–	5	ns
10	MS_SCLKO fall time[1]	–	5	ns
11	MS_BS delay time[1]	–	3	ns

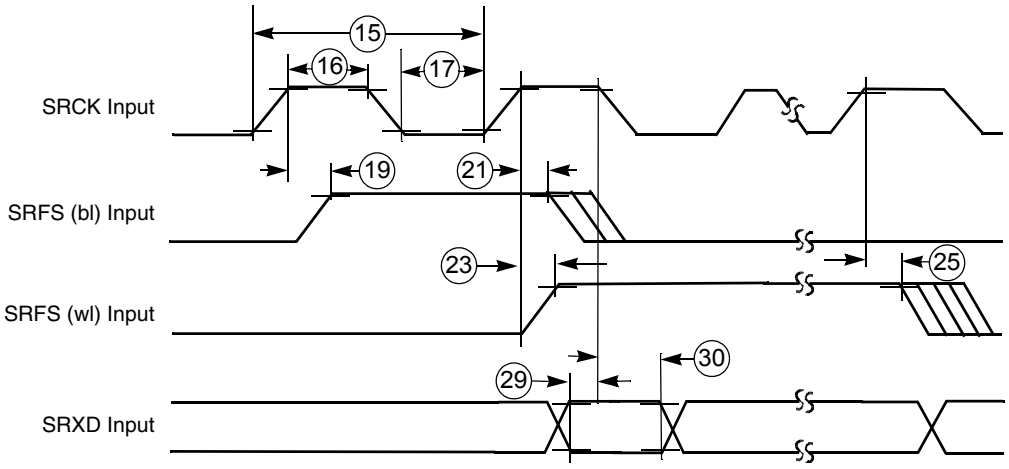


Figure 67. SSI Receiver External Clock Timing Diagram

Table 39. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Primary Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.5	4.5	1.3	3.9	ns
3	SRCK high to SRFS (bl) high[3]	-1.2	-1.7	-1.1	-1.5	ns
4	STCK high to STFS (bl) low[3]	2.5	4.3	2.2	3.8	ns
5	SRCK high to SRFS (bl) low[3]	0.1	-0.8	0.1	-0.8	ns
6	STCK high to STFS (wl) high[3]	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high[3]	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low[3]	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low[3]	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	–	18.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Primary Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns

Table 40. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	STCK high to STXD high impedance	17.90	29.75	15.7	26.1	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hold time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port B Alternate Function[2])						
31	SRXD setup before STCK falling	18.81	–	16.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port B Alternate Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1 All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

2 There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

3 bl = bit length; wl = word length.

Table 41. SSI 2 (Port C Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8V +/- 0.10V		3.0V +/- 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Alternate Function)[2]						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns

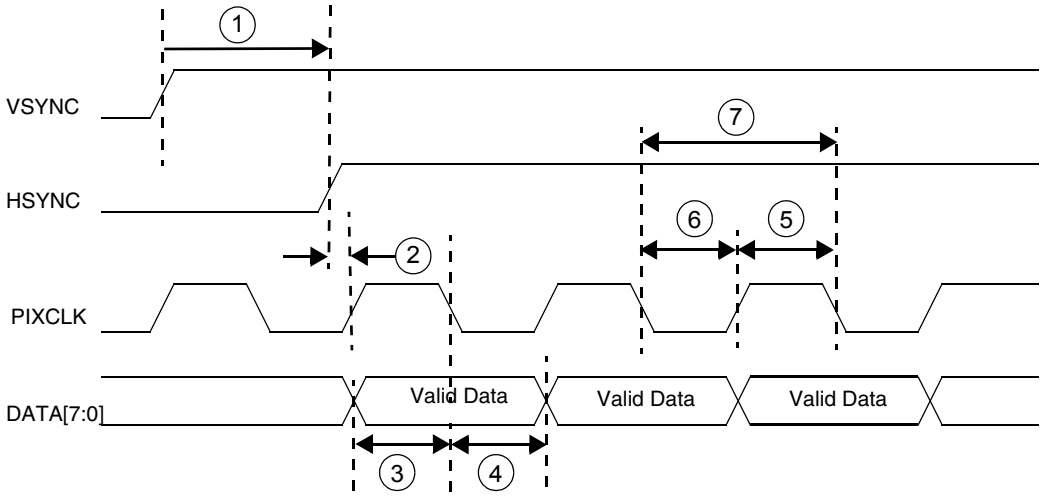


Figure 69. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge

Table 42. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

NOTES