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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx1dvm20

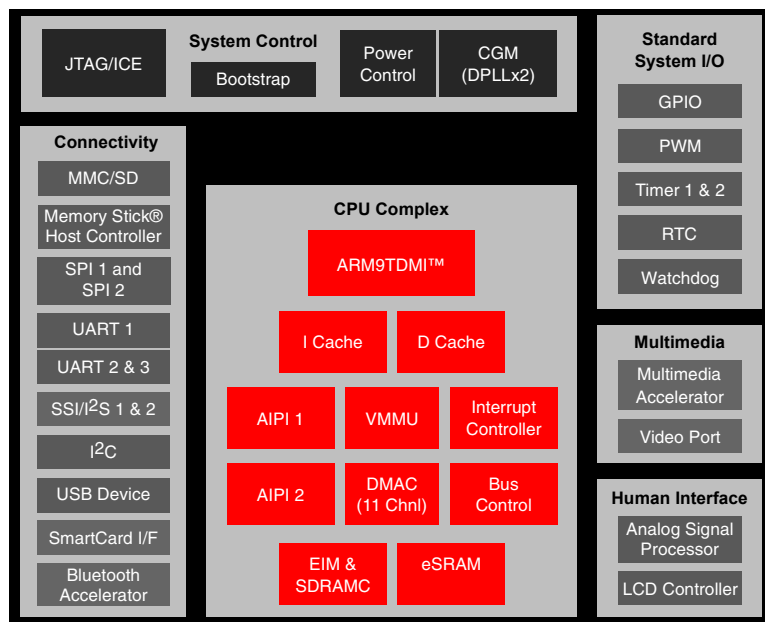


Figure 1. i.MX1 Functional Block Diagram

1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Three Universal Asynchronous Receiver/Transmitters (UART 1, UART 2, and UART3)
- Two Serial Peripheral Interfaces (SPI1 and SPI2)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)
- Direct Memory Access Controller (DMAC)
- Two Synchronous Serial Interfaces and an Inter-IC Sound (SSI1 and SSI2/I²S) Module
- Inter-IC (I²C) Bus Module
- Video Port

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
DMA	
DMA_REQ	DMA Request—external DMA request signal. Multiplexed with SPI1_SPI_RDY.
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{ECB}$, $\overline{LBA}$, BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SIM	
SIM_CLK	SIM Clock
SIM_RST	SIM Reset
SIM_RX	Receive Data

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	T6	$\overline{CS1}$	O									H	
NVDD1	T7	$\overline{CS0}$	O									H ¹	
NVDD1	R6	D5	I/O	69K								Pull-H	
NVDD1	P6	$\overline{ECB}$	I		ETMTRACEPKT7		PA20	69K				Pull-H	$\overline{ECB}$
NVDD1	N6	D4	I/O	69K								Pull-H	
NVDD1	R7	$\overline{LBA}$	O		ETMTRACEPKT6		PA19	69K				H	$\overline{LBA}$
NVDD1	P8	D3	I/O	69K								Pull-H	
NVDD1	R8	BCLK			ETMTRACEPKT5		PA18	69K				L	BCLK
NVDD1	P7	D2	I/O	69K								Pull-H	
	J7	VSS	Static										
NVDD1	L6	NVDD1	Static										
NVDD1	N7	DTACK	I		ETMTRACEPKT4		PA17	69K	SPI2_SS	A25		Pull-H	PA17
NVDD1	N8	D1	I/O	69K								Pull-H	
NVDD1	M7	$\overline{RW}$										H	
NVDD1	T8	MA11	O									L	
NVDD1	M8	MA10	O									L	
NVDD1	R9	D0	I/O	69K								Pull-H	
	K7	VSS	Static										
NVDD1	P9	DQM3	O									L	
NVDD1	T9	DQM2	O									L	
NVDD1	N9	DQM1	O									L	
NVDD1	R10	DQM0	O									L	
NVDD1	M9	$\overline{RAS}$	O									H	
NVDD1	L8	$\overline{CAS}$	O									H	
NVDD1	J8	NVDD1	Static										



Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	T10	SDWE	O									H	
NVDD1	R11	SDCKE0	O									H	
NVDD1	P10	SDCKE1	O									H	
NVDD1	N10	RESET_SF	O									L/H	
NVDD1	T11	CLKO	O									L	
	L7	VSS	Static										
AVDD1	T12	AVDD1	Static										
AVDD1	M10	RESET_IN	I	69K								L/H ²	
AVDD1	N11	RESET_OUT	O									L/H	
AVDD1	R12	POR	I									H/L ²	
AVDD1	M11	BIG_ENDIAN	I									Hiz ³	
AVDD1	P11	BOOT3	I									Hiz ⁴	
AVDD1	N12	BOOT2	I									Hiz ⁴	
AVDD1	R13	BOOT1	I									Hiz ⁴	
AVDD1	P12	BOOT0	I									Hiz ⁴	
AVDD1	T13	TRISTATE	I									Hiz ⁴	
AVDD1	P13	TRST	I	69K								H	
QVDD2	R15	QVDD2	Static										
	T16	VSS	Static										
AVDD1	T14	EXTAL16M	I									Hiz	
AVDD1	T15	XTAL16M	O										
AVDD1	R16	EXTAL32K	I									Hiz	
AVDD1	P16	XTAL32K	O										
NVDD2	K10	NVDD2	Static										

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
	J9	VSS	Static										
QVDD ⁶	E16	R2A	I									qvdd	
QVDD ⁶	D16	R2B	I										
QVDD ⁶	F14	PX1	I										
QVDD ⁶	F13	PY1	I										
QVDD ⁶	E15	PX2	I										
QVDD ⁶	E14	PY2	I										
QVDD ⁶	D15	R1A	I										
QVDD ⁶	C16	R1B	I										
	C15	VSS	Static										
AVDD2 ⁶	C14	AVDD2	Static										
QVDD ⁶	B16	NC	I										
QVDD ⁶	A16	NC	I										
QVDD ⁶	B15	UIN	I										
QVDD ⁶	A15	UIP	I										
QVDD ⁶	E13	NC	I										
QVDD ⁶	D14	NC	I										
QVDD ⁶	B14	RVM	I										
QVDD ⁶	A14	RVP	I										
QVDD ⁶	D13	NC	I										
QVDD ⁶	C13	NC	I										
QVDD ⁶	E12	NC	O										



Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns
4a	Output hold time	2.28	–	2	–	ns
4b	Output setup time	3.42	–	3	–	ns

4.2 DPLL Timing Specifications

Parameters of the DPLL are given in [Table 10](#). In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 10. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
DPLL input clock freq range	Vcc = 1.8V	5	–	100	MHz
Pre-divider output clock freq range	Vcc = 1.8V	5	–	30	MHz
DPLL output clock freq range	Vcc = 1.8V	80	–	220	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Pre-multiplier lock-in time	–	–	–	312.5	μsec
Freq lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	250	280 (56 μs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	250 (50 μs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	300	350 (70 μs)	400	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	270	320 (64 μs)	370	T_{ref}
Freq jitter (p-p)	–	–	0.005 (0.01%)	0.01	$2 \cdot T_{dck}$

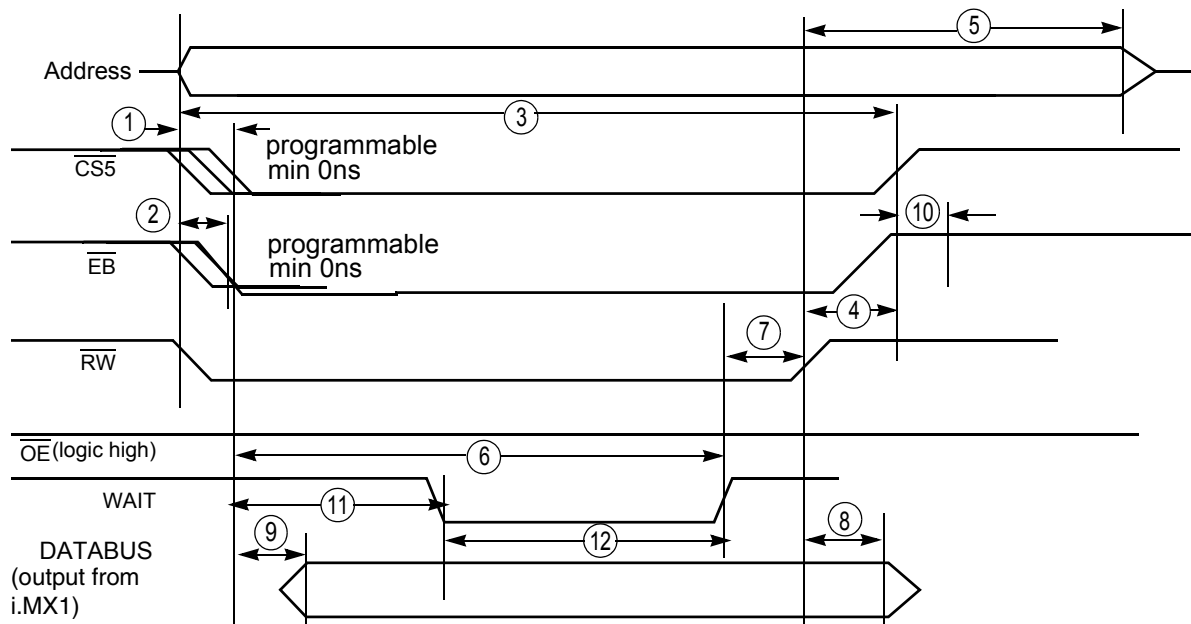
Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	Wait pulse width	1T	1020T	ns

Note:

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS}$ is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA


Figure 8. WAIT Write Cycle without DMA
Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS}$ is negated	2.5T-0.29	2.5T+0.68	ns
5	$\overline{RW}$ negated to Address inactive	67.28	–	ns
6	Wait asserted after $\overline{CS}$ asserted	–	1020T	ns

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
7	Wait asserted to $\overline{RW}$ negated	1T+2.15	2T+7.34	ns
8	Data hold timing after $\overline{RW}$ negated	2.5T-1.18	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{EB}$ negated after $\overline{CS5}$ is negated	1.5T+0.74	1.5T+2.35	ns
11	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion can also be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

4.4.2.4 WAIT Write Cycle DMA Enabled

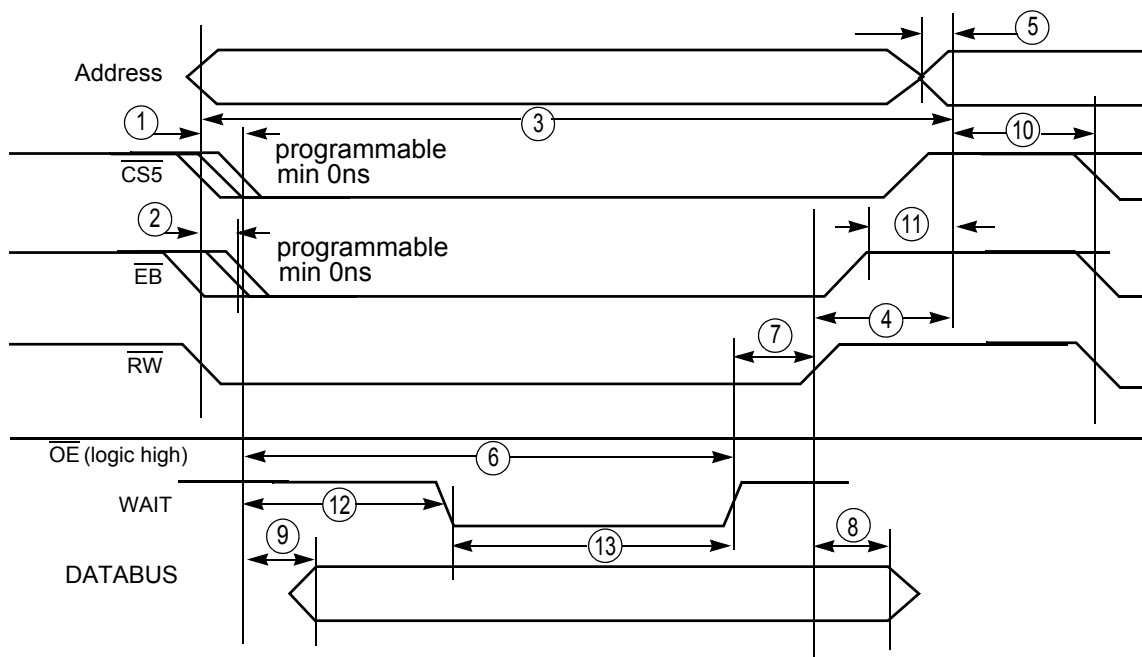


Figure 9. WAIT Write Cycle DMA Enabled

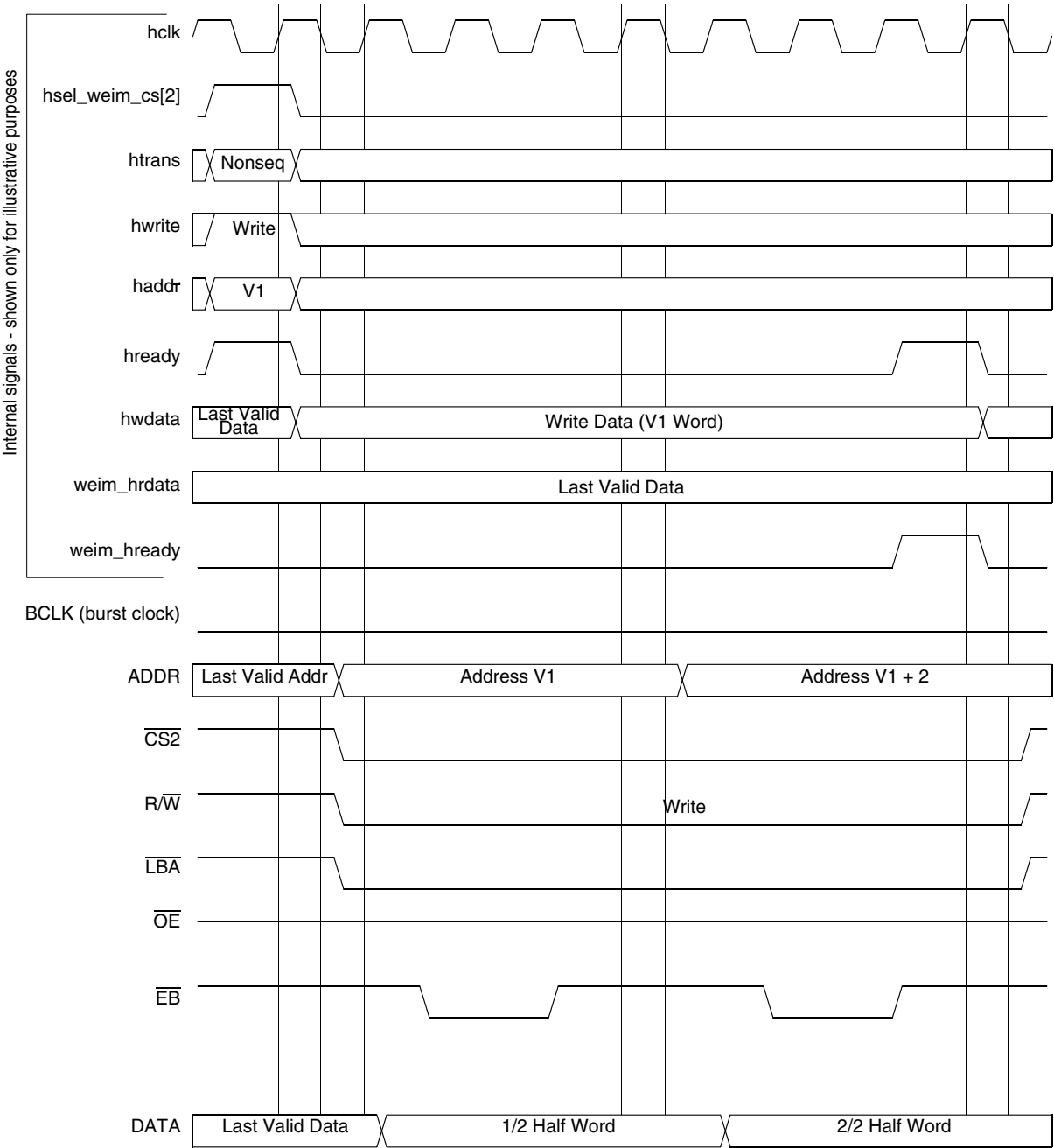


Figure 17. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF

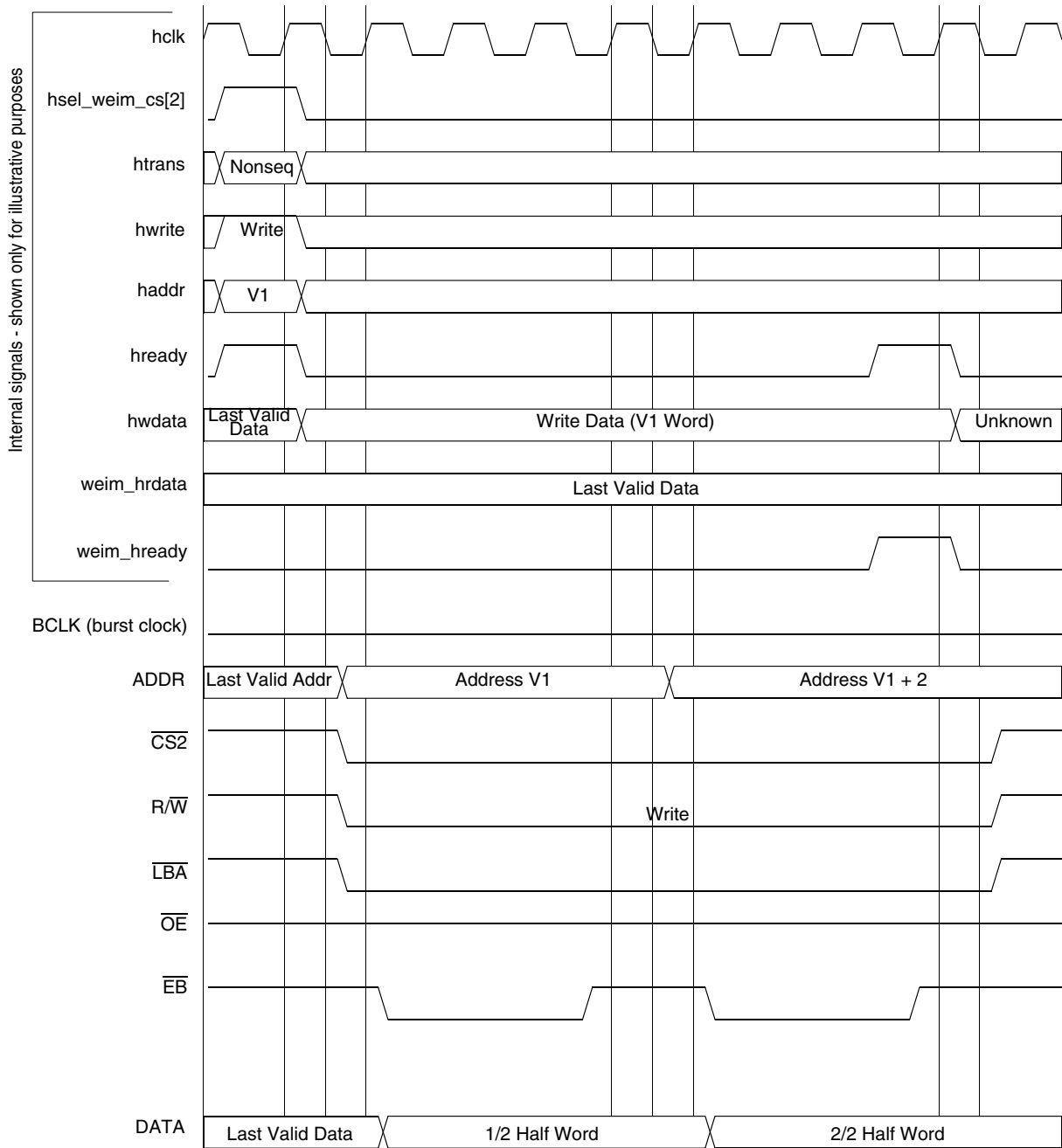
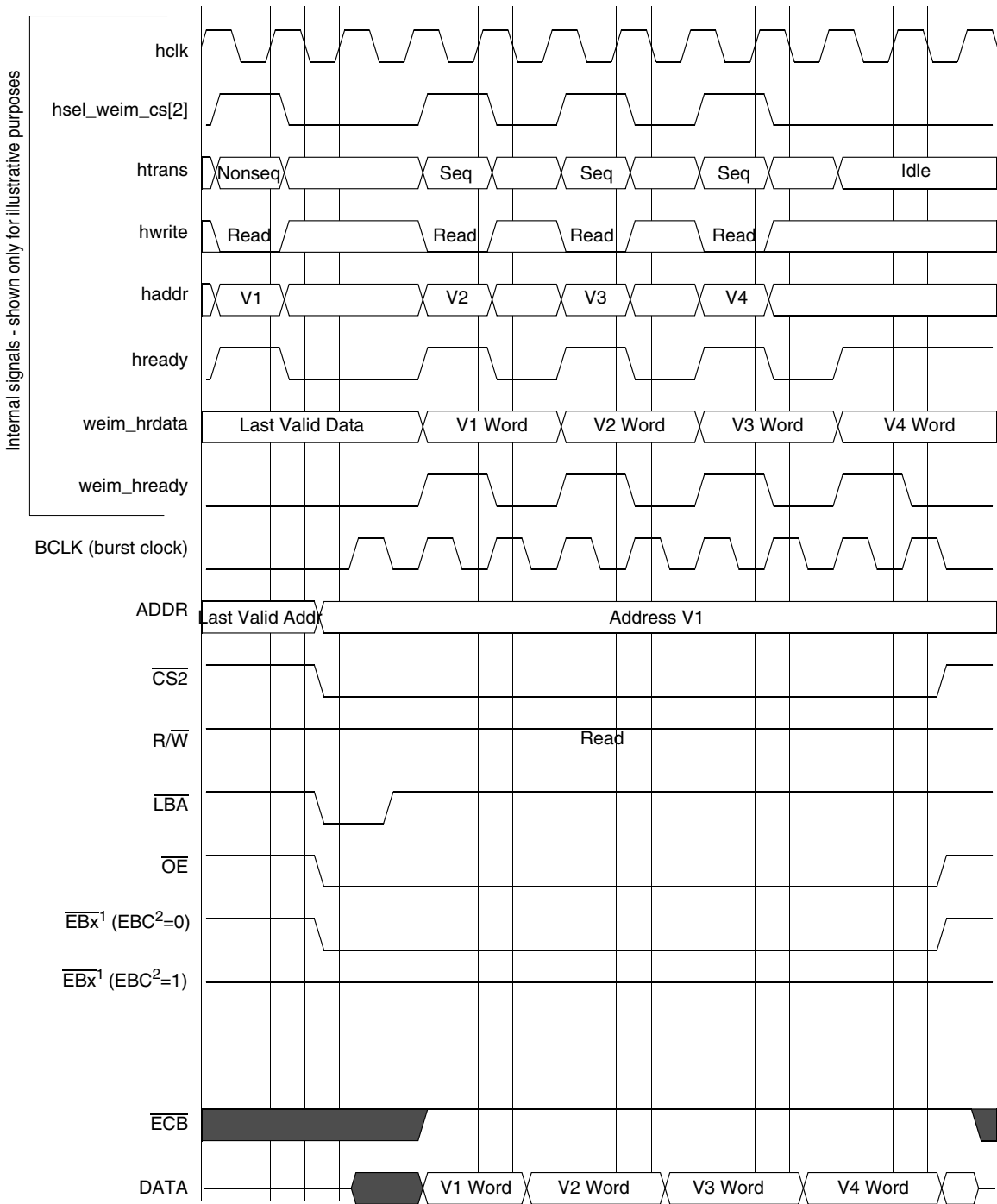


Figure 20. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 29. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

Table 28. SDHC Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency at Data transfer Mode (PP) ¹ —10/30 cards	0	25/5	0	25/5	MHz
2	CLK frequency at Identification Mode ²	0	400	0	400	kHz
3a	Clock high time ¹ —10/30 cards	6/33	—	10/50	—	ns
3b	Clock low time ¹ —10/30 cards	15/75	—	10/50	—	ns
4a	Clock fall time ¹ —10/30 cards	—	10/50 (5.00) ³	—	10/50	ns
4b	Clock rise time ¹ —10/30 cards	—	14/67 (6.67) ³	—	10/50	ns
5a	Input hold time ³ —10/30 cards	10.3/10.3	—	9/9	—	ns
5b	Input setup time ³ —10/30 cards	10.3/10.3	—	9/9	—	ns
6a	Output hold time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
6b	Output setup time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
7	Output delay time ³	0	16	0	14	ns

¹ C_L ≤ 100 pF / 250 pF (10/30 cards)

² C_L ≤ 250 pF (21 cards)

³ C_L ≤ 25 pF (1 card)

4.10.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is NCR clock cycles as illustrated in Figure 48. The symbols for Figure 48 through Figure 52 are defined in Table 29.

Table 29. State Signal Parameters for Figure 48 through Figure 52

Card Active		Host Active	
Symbol	Definition	Symbol	Definition
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)

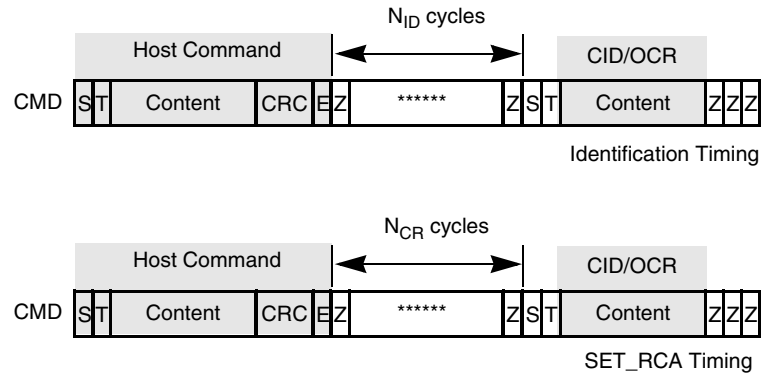


Figure 48. Timing Diagrams at Identification Mode

After a card receives its RCA, it switches to data transfer mode. As shown on the first diagram in [Figure 49](#), SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods N_{RC} and N_{CC} .

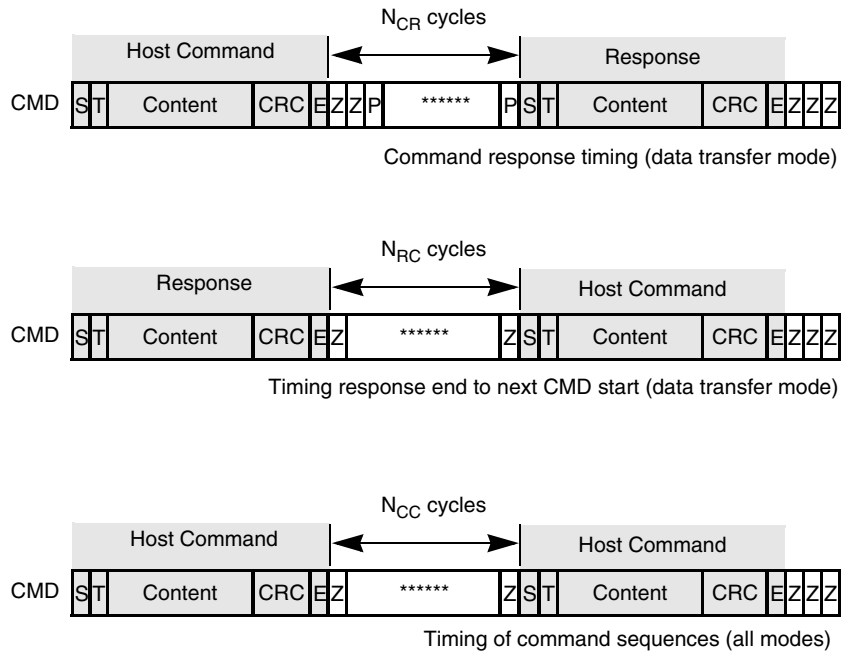


Figure 49. Timing Diagrams at Data Transfer Mode

[Figure 50](#) shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC} , beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

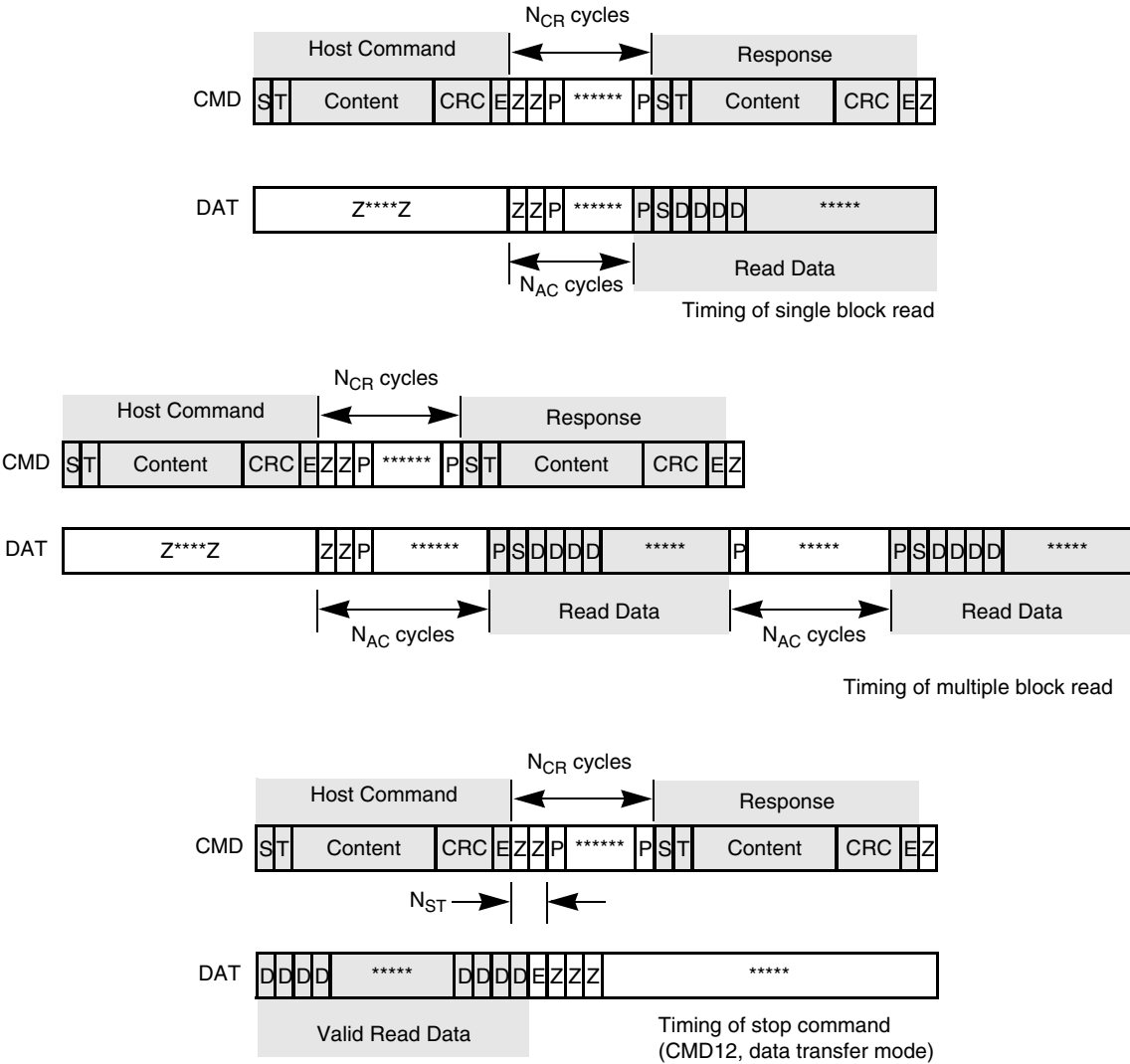


Figure 50. Timing Diagrams at Data Read

Figure 51 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

Table 33. SDRAM Read Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	3.42	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	2.28	–	2	–	ns
4S	Address setup time	3.42	–	3	–	ns
4H	Address hold time	2.28	–	2	–	ns
5	SDRAM access time (CL = 3)	–	6.84	–	6	ns
5	SDRAM access time (CL = 2)	–	6.84	–	6	ns
5	SDRAM access time (CL = 1)	–	22	–	22	ns
6	Data out hold time	2.85	–	2.5	–	ns
7	Data out high-impedance time (CL = 3)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 2)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 1)	–	22	–	22	ns
8	Active to read/write command period (RC = 1)	t_{RCD}^1	–	t_{RCD1}	–	ns

¹ t_{RCD} = SDRAM clock cycle time. This settings can be found in the *MC9328MX1 reference manual*.

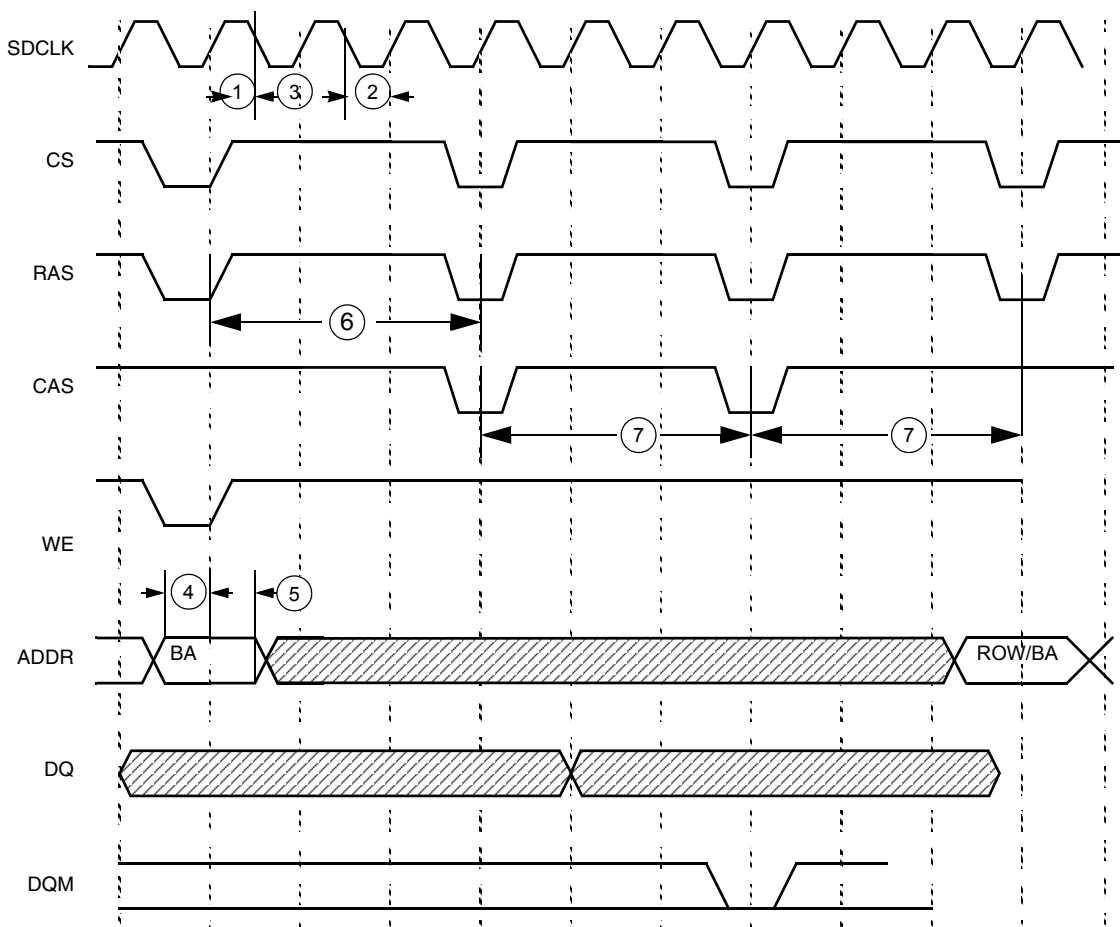


Figure 59. SDRAM Refresh Timing Diagram

Table 35. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}^1	–	t_{RP1}	–	ns
7	Auto precharge command period	t_{RC1}	–	t_{RC1}	–	ns

¹ t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *MC9328MX1 reference manual*.

Table 39. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
18	STCK high to STFS (bl) high ³	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high ³	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low ³	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low ³	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high ³	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high ³	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low ³	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low ³	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function²)						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port C Primary Function²)						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

¹ All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSS/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

² There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

³ bl = bit length; wl = word length.

Table 41. SSI 2 (Port C Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V +/- 0.10V		3.0V +/- 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Alternate Function)²						
15	STCK/SRCK clock period ¹	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high ³	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high ³	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low ³	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low ³	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high ³	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high ³	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low ³	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low ³	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns
28	STCK high to STXD high impedance	17.90	29.75	15.7	26.1	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Alternate Function)²						
31	SRXD setup before STCK falling	18.81	–	16.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port C Alternate Function)²						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

¹ All the timings for both SSI modules are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

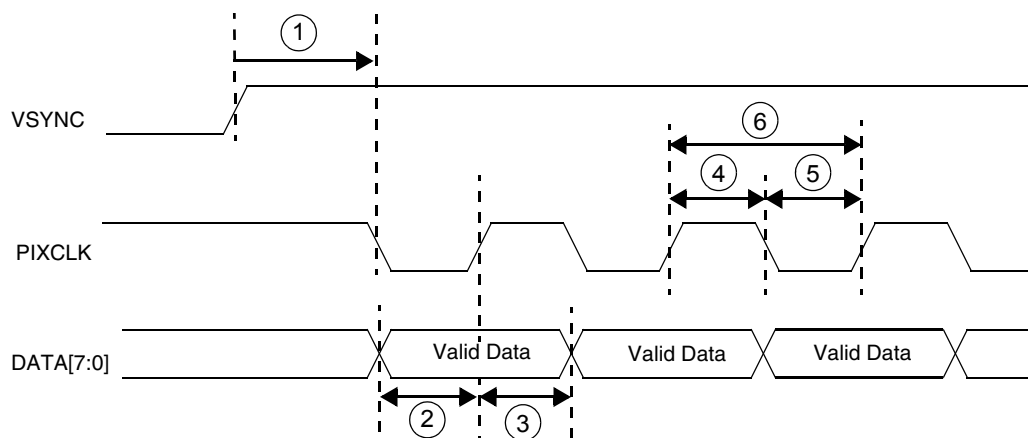
Falling-edge latch data

max fall time allowed = (negative duty cycle - hold time)

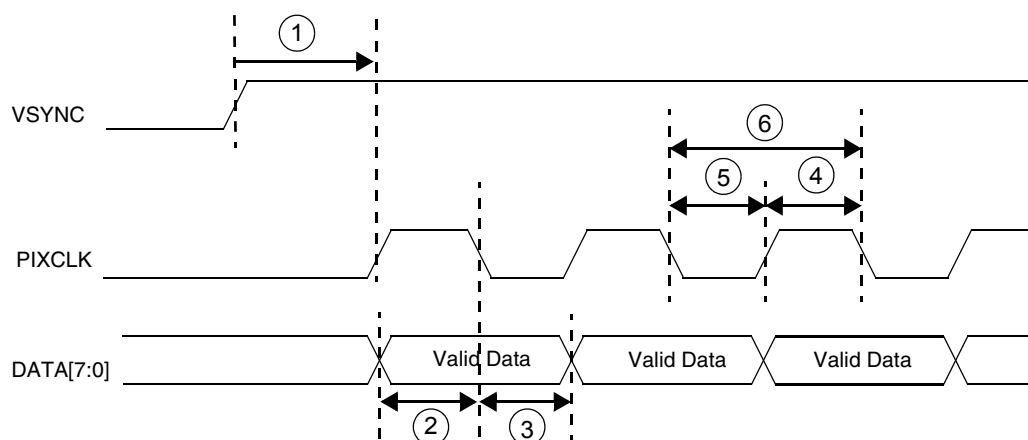
max rise time allowed = (positive duty cycle - setup time)

4.17.2 Non-Gated Clock Mode

Figure 70 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 71 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 43.



**Figure 70. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**



**Figure 71. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge**

Table 43. Non-Gated Clock Mode Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_pixclk	180	—	ns
2	csi_d setup time	1	—	ns

5 Pin-Out and Package Information

Table 44 illustrates the package pin assignments for the 256-pin MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 11.

Table 44. i.MX1 256 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NVSS	SD_DAT3	SD_CLK	NVSS	USBD_AFE	NVDD4	NVSS	UART1_RTS	UART1_RXD	NVDD3	BT5	BT3	QVDD4	RVP	UIP	N.C.	A
B	A24	SD_DAT1	SD_CMD	SIM_TX	USBD_ROE	USBD_VP	SSI_RXCLK	SSI_TXCLK	SPI1_SCLK	BT11	BT7	BT1	QVSS	RVM	UIN	N.C.	B
C	A23	D31	SD_DAT0	SIM_PD	USBD_RCV	UART2_CTS	UART2_RXD	SSI_RXFS	UART1_TXD	BTRFGND	BT8	BTRFVDD	N.C.	AVDD2 ¹	VSS	R1B	C
D	A22	D30	D29	SIM_SVEN	USBD_SUSPND	USBD_VPO	USBD_VMO	SSI_RXDAT	SPI1_SPL_RDY	BT13	BT6	N.C.	N.C.	N.C.	R1A	R2B	D
E	A20	A21	D28	D26	SD_DAT2	USBD_VM	UART2_RTS	SSI_TXDAT	SPI1_SS	BT12	BT4	N.C.	N.C.	PY2	PX2	R2A	E
F	A18	D27	D25	A19	A16	SIM_RST	UART2_TXD	SSI_TXFS	SPI1_MISO	BT10	BT2	REV	PY1	PX1	LSCLK	SPL_SPR	F
G	A15	A17	D24	D23	D21	SIM_RX	SIM_CLK	UART1_CTS	SPI1_MOSI	BT9	CLS	CONTRAST	ACD/OE	LP/HSYNC	FLM/VSYNC	LD1	G
H	A13	D22	A14	D20	NVDD1	NVDD1	NVSS	QVSS	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3	H
J	A12	A11	D18	D19	NVDD1	NVDD1	NVSS	NVDD1	NVSS	NVSS	LD6	LD7	LD8	LD11	QVDD3	QVSS	J
K	A10	D16	A9	D17	NVDD1	NVSS	NVSS	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TMR2OUT	LD15	K
L	A8	A7	D13	D15	D14	NVDD1	NVSS	CAS	TCK	TIN	PWMO	CSI_MCLK	CSI_D0	CSI_D1	CSI_D2	CSI_D3	L
M	A5	D12	D11	A6	SDCLK	NVSS	RW	MA10	RAS	RESET_IN	BIG_ENDIAN	CSI_D4	CSI_HSYNC	CSI_VSYNC	CSI_D6	CSI_D5	M
N	A4	EB1	D10	D7	A0	D4	PA17	D1	DQM1	RESET_SF ²	RESET_OUT	BOOT2	CSI_PIXCLK	CSI_D7	TMS	TDI	N
P	A3	D9	EB0	CS3	D6	ECB	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	TRST	I2C_SCL	I2C_SDA	XTAL32K	P
R	EB2	EB3	A1	CS4	D8	D5	LBA	BCLK ³	D0	DQM0	SDCKE0	POR	BOOT1	TD0	QVDD2	EXTAL32K	R
T	NVSS	A2	OE	CS5	CS2	CS1	CS0	MA11	DQM2	SDWE	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	QVSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

¹ ASP signals are clamped by AVDD2 to prevent ESD (Electrostatic Discharge) damage. AVDD2 must be greater than QVDD to keep diodes reversed-biased.

² This signal is not used and should be floated in an actual application.

³ burst clock