Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx1dvm20r2

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	T10	$\overline{\text{SDWE}}$	O									H	
NVDD1	R11	SDCKE0	O									H	
NVDD1	P10	SDCKE1	O									H	
NVDD1	N10	$\overline{\text{RESET\_SF}}$	O									L/H	
NVDD1	T11	CLKO	O									L	
	L7	VSS	Static										
AVDD1	T12	AVDD1	Static										
AVDD1	M10	$\overline{\text{RESET\_IN}}$	I	69K								L/H[2]	
AVDD1	N11	$\overline{\text{RESET\_OUT}}$	O									L/H	
AVDD1	R12	POR	I									H/L[2]	
AVDD1	M11	BIG_ENDIAN	I									Hiz[3]	
AVDD1	P11	BOOT3	I									Hiz[4]	
AVDD1	N12	BOOT2	I									Hiz[4]	
AVDD1	R13	BOOT1	I									Hiz[4]	
AVDD1	P12	BOOT0	I									Hiz[4]	
AVDD1	T13	TRISTATE	I									Hiz[4]	
AVDD1	P13	$\overline{\text{TRST}}$	I	69K								H	
QVDD2	R15	QVDD2	Static										
	T16	VSS	Static										
AVDD1	T14	EXTAL16M	I									Hiz	
AVDD1	T15	XTAL16M	O										
AVDD1	R16	EXTAL32K	I									Hiz	
AVDD1	P16	XTAL32K	O										
NVDD2	K10	NVDD2	Static										

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD3	C9	UART1_TXD	O				PC11	69K				Pull-H	PC11
NVDD3	A8	$\overline{\text{UART1\_RTS}}$	I				PC10	69K				Pull-H	PC10
NVDD3	G8	$\overline{\text{UART1\_CTS}}$	O				PC9	69K				Pull-H	PC9
NVDD3	B8	SSI_TXCLK	I/O				PC8	69K				Pull-H	PC8
NVDD3	F8	SSI_TXFS	I/O				PC7	69K				Pull-H	PC7
NVDD3	E8	SSI_TXDAT	O				PC6	69K				Pull-H	PC6
NVDD3	D8	SSI_RXDAT	I				PC5	69K				Pull-H	PC5
NVDD3	B7	SSI_RXCLK	I/O				PC4	69K				Pull-H	PC4
NVDD3	C8	SSI_RXFS	I/O				PC3	69K				Pull-H	PC3
	A7	VSS	Static										
NVDD4	C7	UART2_RXD	I				PB31	69K				Pull-H	PB31
NVDD4	F7	UART2_TXD	O				PB30	69K				Pull-H	PB30
NVDD4	E7	$\overline{\text{UART2\_RTS}}$	I				PB29	69K				Pull-H	PB29
NVDD4	C6	$\overline{\text{UART2\_CTS}}$	O				PB28	69K				Pull-H	PB28
NVDD4	D7	USBD_VMO	O				PB27	69K				Pull-H	PB27
NVDD4	D6	USBD_VPO	O				PB26	69K				Pull-H	PB26
NVDD4	E6	USBD_VM	I				PB25	69K				Pull-H	PB25
NVDD4	B6	USBD_VP	I				PB24	69K				Pull-H	PB24
NVDD4	D5	USBD_SUSPND	O				PB23	69K				Pull-H	PB23
NVDD4	C5	USBD_RCV	I/O				PB22	69K				Pull-H	PB22
NVDD4	B5	$\overline{\text{USBD\_ROE}}$	O				PB21	69K				Pull-H	PB21
NVDD4	A5	USBD_AFE	O				PB20	69K				Pull-H	PB20
	A4	VSS	Static										
NVDD4	A6	NVDD4	Static										
NVDD4	G7	SIM_CLK	O		SSI_TXCLK	I/O	PB19	69K				Pull-H	PB19

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD4	F6	SIM_RST	O		SSI_TXFS	I/O	PB18	69K				Pull-H	PB18
NVDD4	G6	SIM_RX	I		SSI_TXDAT	O	PB17	69K				Pull-H	PB17
NVDD4	B4	SIM_TX	I/O		SSI_RXDAT	I	PB16	69K				Pull-H	PB16
NVDD4	C4	SIM_PD	I		SSI_RXCLK	I/O	PB15	69K				Pull-H	PB15
NVDD4	D4	SIM_SVEN	O		SSI_RXFS	I/O	PB14	69K				Pull-H	PB14
NVDD4	B3	SD_CMD	I/O		MS_BS	O	PB13	69K				Pull-H	PB13
NVDD4	A3	SD_CLK	O		MS_SCLKO	O	PB12	69K				Pull-H	PB12
NVDD4	A2	SD_DAT3	I/O		MS_SDIO	I/O	PB11	69K (pull down)				Pull-L	PB11
NVDD4	E5	SD_DAT2	I/O		MS_SCLKI	I	PB10	69K				Pull-H	PB10
NVDD4	B2	SD_DAT1	I/O		MS_PI1	I	PB9	69K				Pull-H	PB9
NVDD4	C3	SD_DAT0	I/O		MS_PI0	I	PB8	69K				Pull-H	PB8

1 After reset, $\overline{CS0}$ goes H/L depends on BOOT[3:0].

2 Need external circuitry to drive the signal.

3 Need external pull-up.

4 External resistor is needed.

5 Need external pull-up or pull-down.

6 ASP signals are clamped by AVDD2 to prevent ESD (electrostatic discharge) damage. AVDD2 must be greater than QVDD to keep diodes reverse-biased.

3 Electrical Characteristics

This section contains the electrical specifications and timing diagrams for the i.MX1 processor.

3.1 Maximum Ratings

Table 4 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 5 on page 23 or the DC Characteristics table.

Table 4. Maximum Ratings

Symbol	Rating	Minimum	Maximum	Unit
NV_{DD}	DC I/O Supply Voltage	-0.3	3.3	V
QV_{DD}	DC Internal (core = 150 MHz) Supply Voltage	-0.3	1.9	V
QV_{DD}	DC Internal (core = 200 MHz) Supply Voltage	-0.3	2.0	V
AV_{DD}	DC Analog Supply Voltage	-0.3	3.3	V
$BTRFV_{DD}$	DC Bluetooth Supply Voltage	-0.3	3.3	V
VESD_HBM	ESD immunity with HBM (human body model)	–	2000	V
VESD_MM	ESD immunity with MM (machine model)	–	100	V
ILatchup	Latch-up immunity	–	200	mA
Test	Storage temperature	-55	150	°C
Pmax	Power Consumption	800[1]	1300[2]	mW

1 A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM® core-that is, 7x GPIO, 15x Data bus, and 8x Address bus.

2 A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core-that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at MHz, and where the whole image is running out of SDRAM. QVDD at V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 5 provides the recommended operating ranges for the supply voltages and temperatures. The i.MX1 processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

BTRFVDD is the supply voltage for the Bluetooth interface signals. It is quite sensitive to the data transmit/receive accuracy. Please refer to Bluetooth RF spec for special handling. If Bluetooth is not used

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA

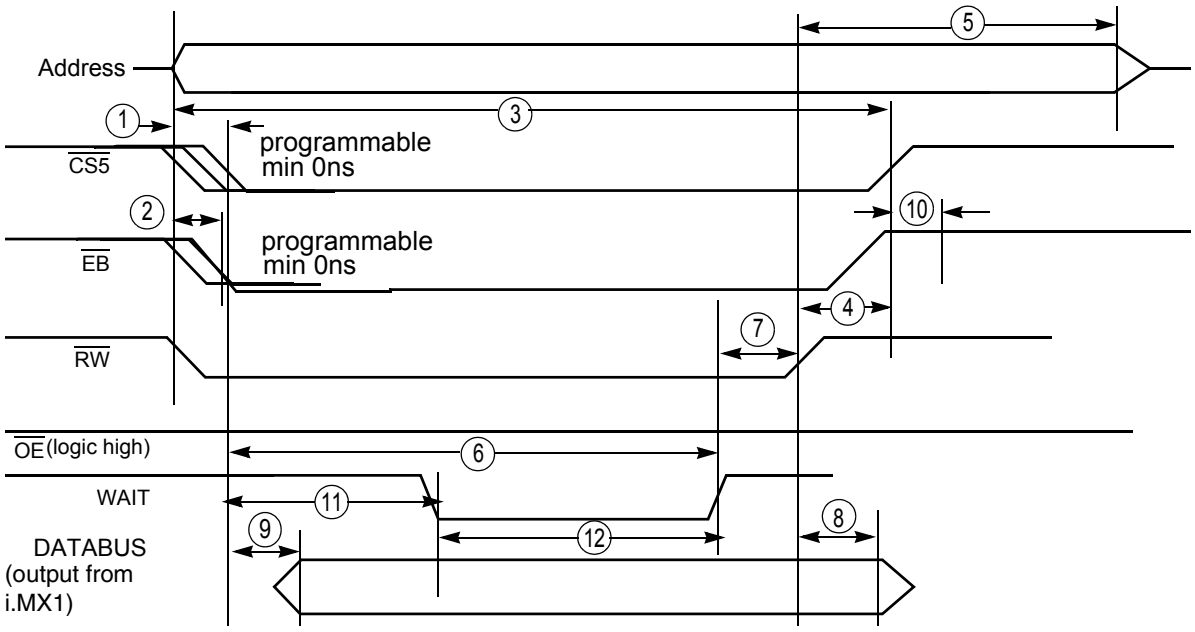
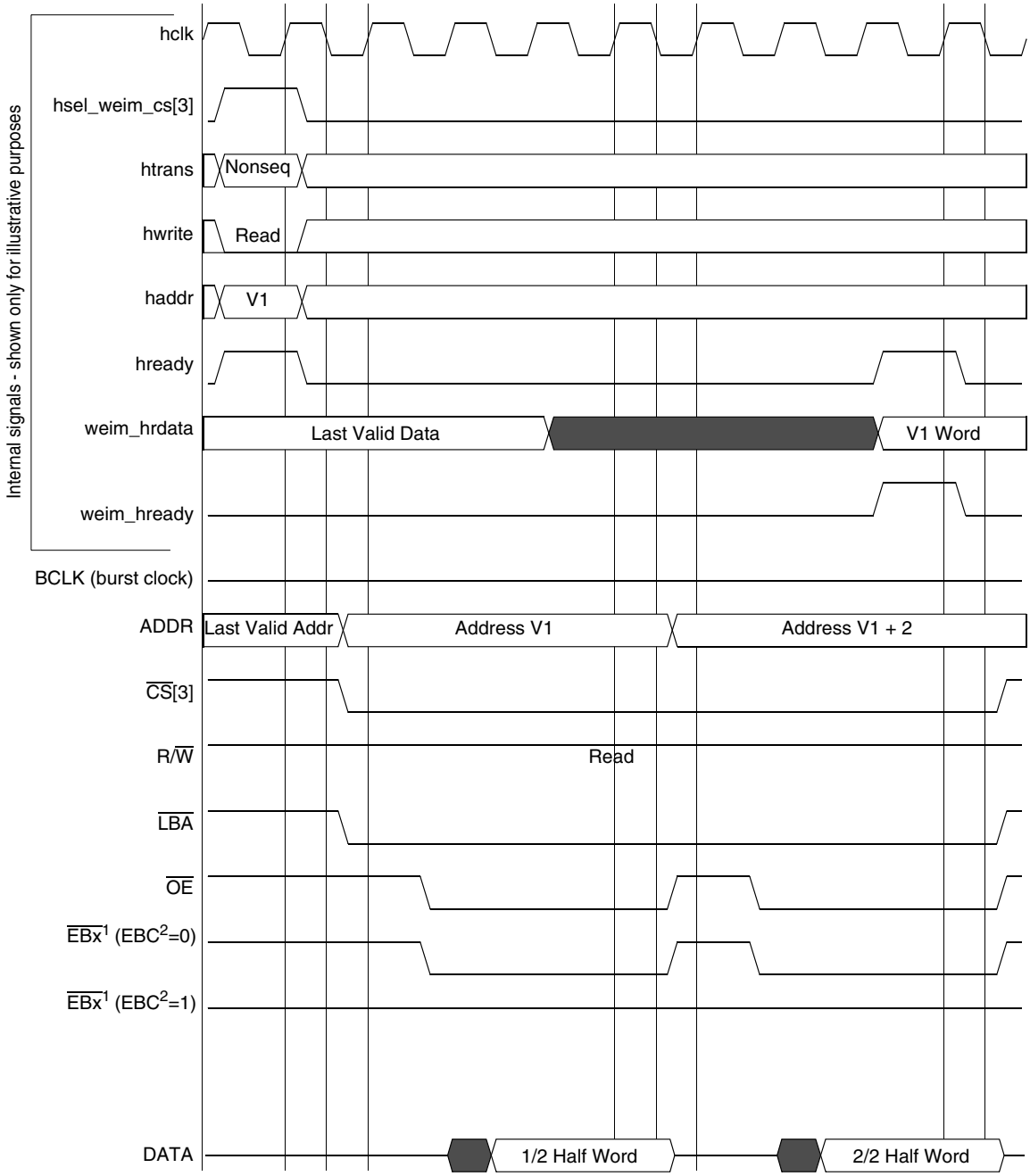


Figure 8. WAIT Write Cycle without DMA

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-0.29	2.5T+0.68	ns
5	$\overline{RW}$ negated to Address inactive	67.28	–	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF

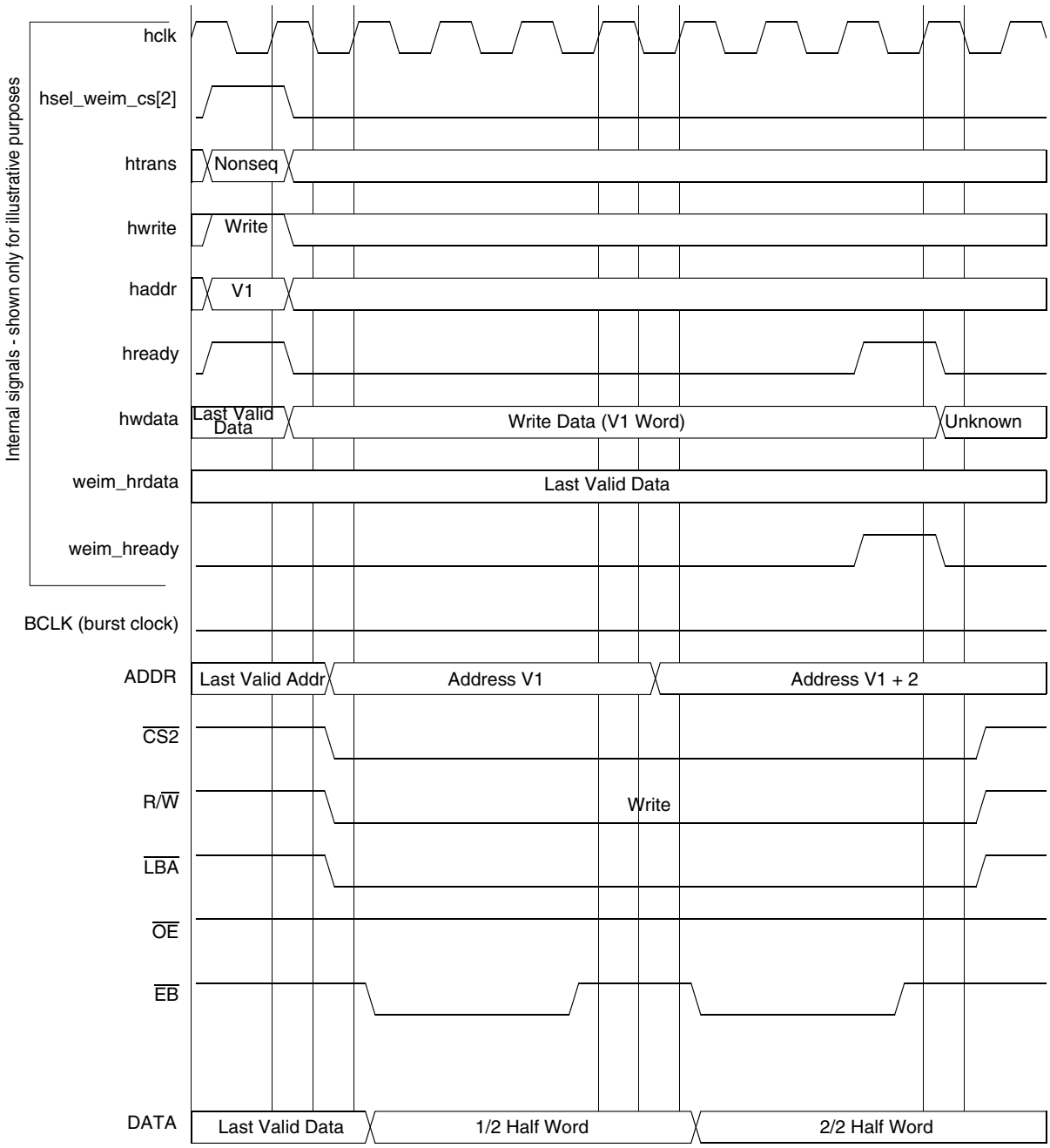
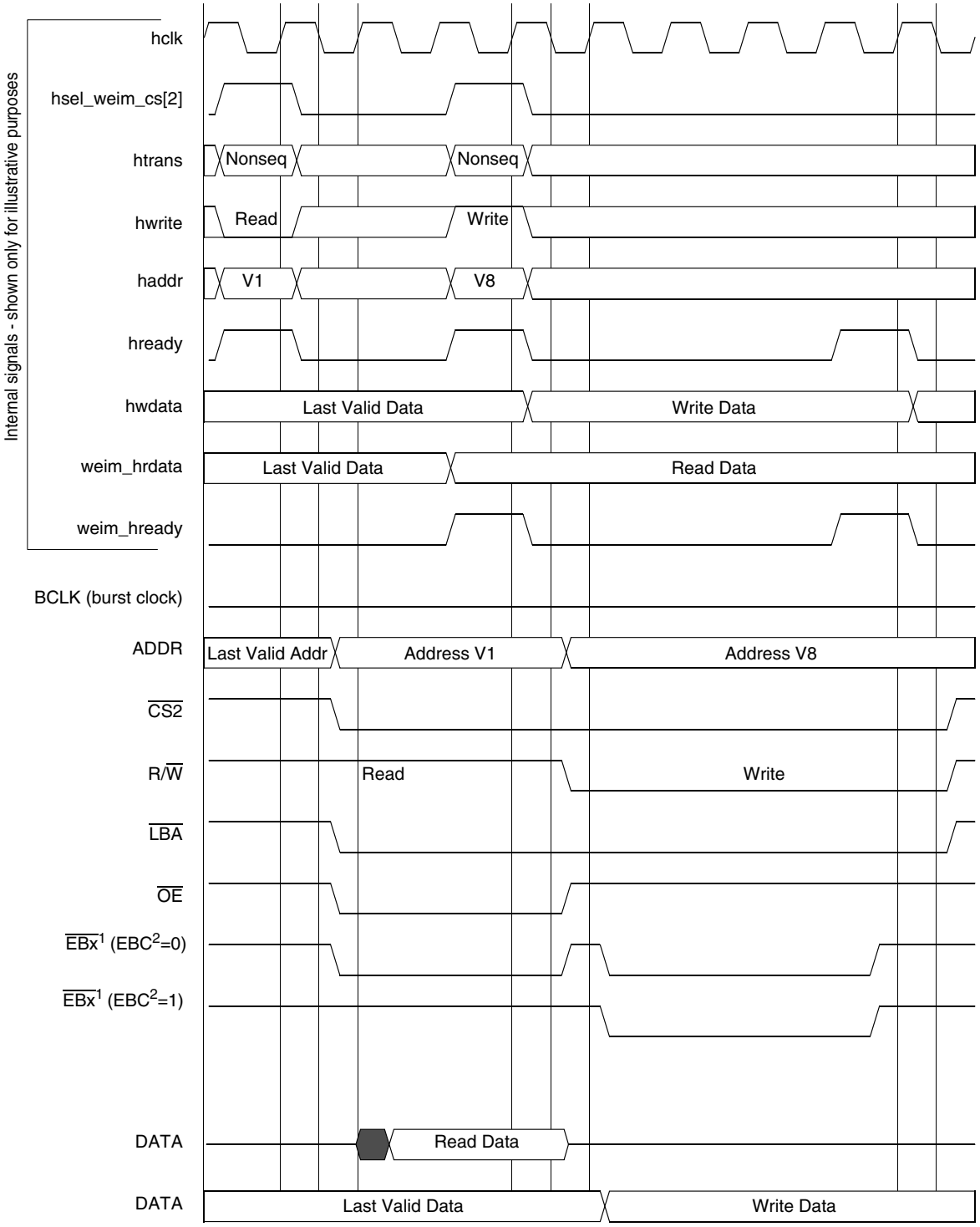
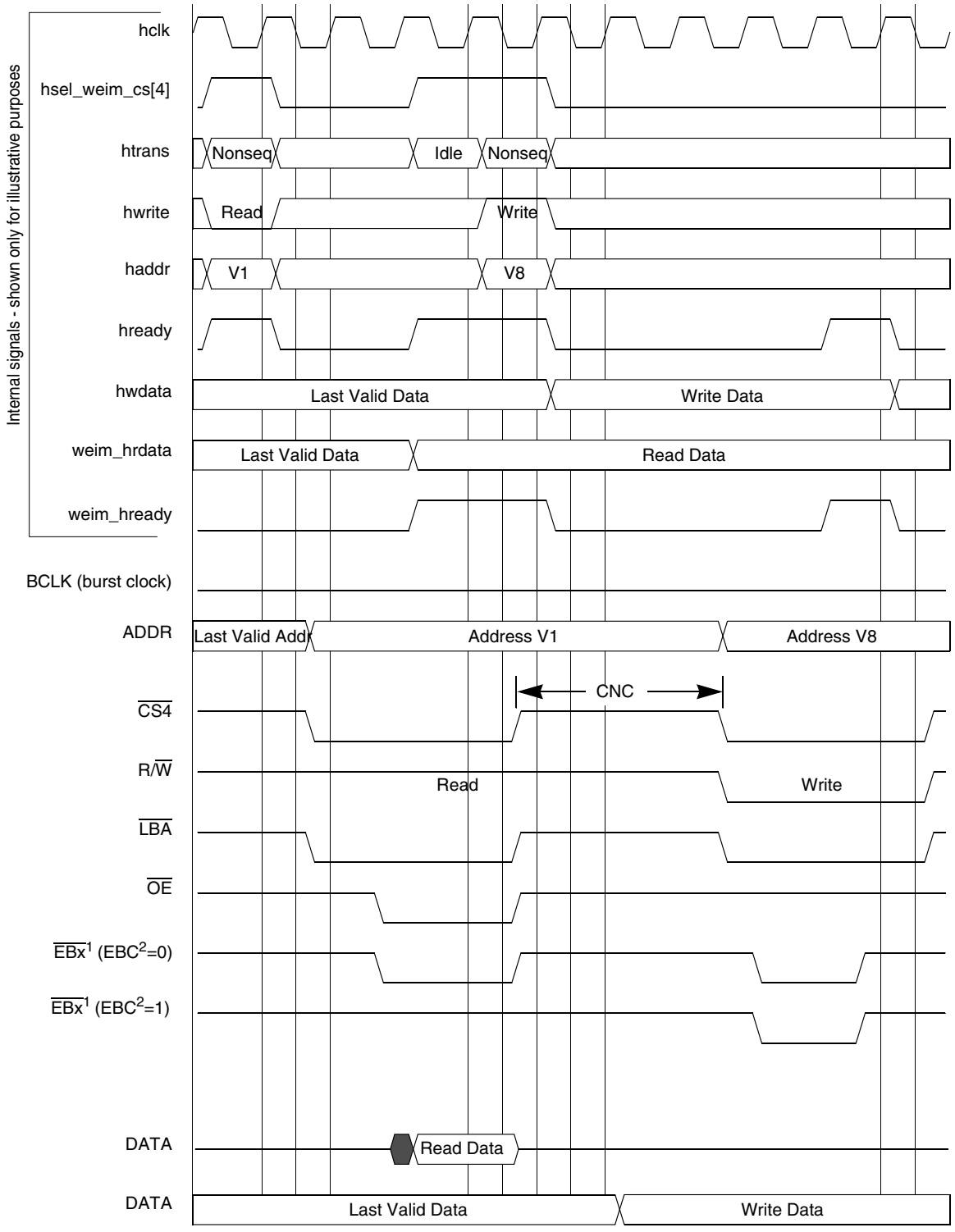


Figure 21. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF



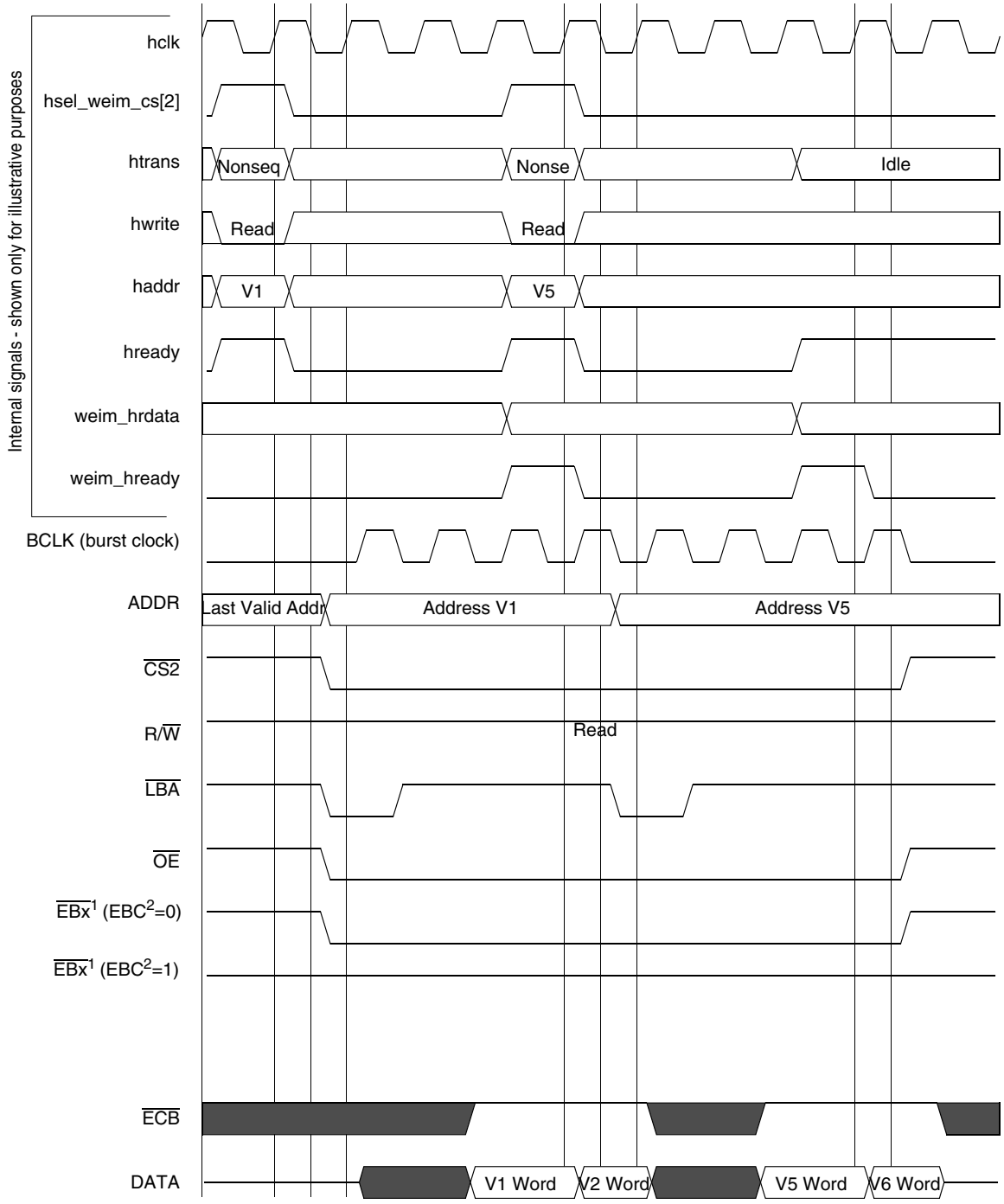
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 27. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 28. WSC = 3, SYNC = 1, A.HALF/E.HALF

Table 19. Pen ADC Test Conditions

Vp max	1800 mV	ip max	+7 µA
Vp min	GND	ip min	1.5 µA
Vn	GND	in	1.5 µA
Sample frequency		12 MHz	
Sample rate		1.2 KHz	
Input frequency		100 Hz	
Input range		0–1800 mV	
Note: Ru1 = Ru2 = 200K			

Table 20. Pen ADC Absolute Rating

ip max	+9.5 µA
ip min	-2.5 µA
in max	+9.5 µA
in min	-2.5 µA

4.6 ASP Touch Panel Controller

The following sections contain the electrical specifications of the ASP touch panel controller. The value of parameters and their corresponding measuring conditions are mentioned as well.

4.6.1 Electrical Specifications

Test conditions: Temperature = 25º C, QVDD = 1800mV.

Table 21. ASP Touch Panel Controller Electrical Spec

Parameter	Minimum	Typical	Maximum	Unit
Offset	–	32768	–	–
Offset Error	–	–	8199	–
Gain	–	13.65	–	mV^{-1}
Gain Error	–	–	33%	–
DNL	8	9	–	Bits
INL	–	0	–	Bits
Accuracy (without missing code)	8	9	–	Bits
Operating Voltage Range (Pen)	–	–	QVDD	mV
Operating Voltage Range (U)	Negative QVDD	–	QVDD	mV
On-resistance of switches SW[8:1]	–	10	–	Ohm

Note that QVDD should be 1800mV.

4.6.2 Gain Calculations

The ideal mapping of input voltage to output digital sample is defined as follows:

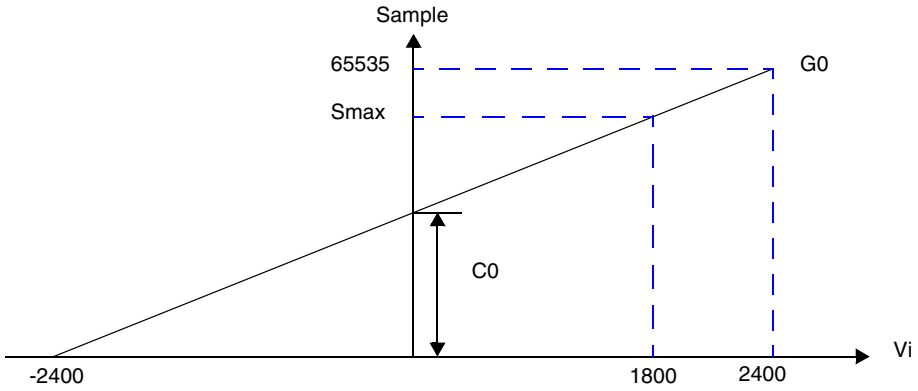


Figure 34. Gain Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

4.6.3 Offset Calculations

The ideal mapping of input voltage to output digital sample is defined as:

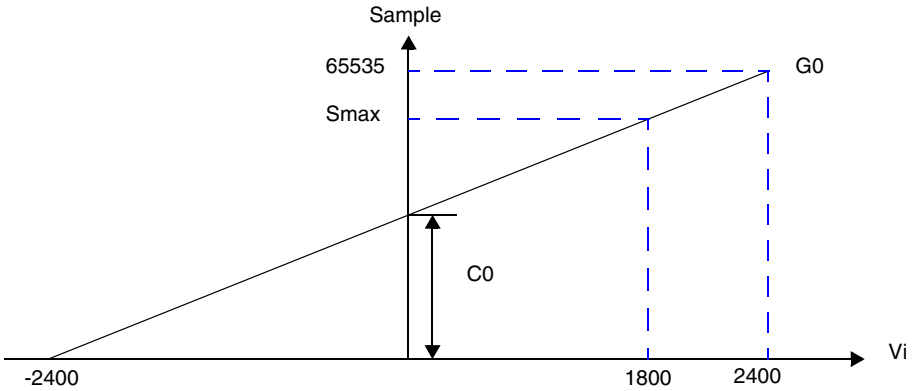


Figure 35. Offset Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

Table 27. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing (Continued)

Symbol	Description	Minimum	Corresponding Register Value	Unit
T8	SCLK to valid LD data	-3	3	ns
T9	End of HSYN idle2 to VSYN edge (for non-display region)	2	2	Ts
T9	End of HSYN idle2 to VSYN edge (for Display region)	1	1	Ts
T10	VSYN to OE active (Sharp = 0) when VWAIT2 = 0	1	1	Ts
T10	VSYN to OE active (Sharp = 1) when VWAIT2 = 0	2	2	Ts

Note:

- Ts is the SCLK period which equals LCDC_CLK / (PCD + 1). Normally LCDC_CLK = 15ns.
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 46, all 3 signals are active low.
- The polarity of SCLK and LD[15:0] can also be programmed.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 46, SCLK is always active.
- For T9 non-display region, VSYN is non-active. It is used as an reference.
- XMAX is defined in pixels.

4.10 Multimedia Card/Secure Digital Host Controller

The DMA interface block controls all data routing between the external data bus (DMA access), internal MMC/SD module data bus, and internal system FIFO access through a dedicated state machine that monitors the status of FIFO content (empty or full), FIFO address, and byte/block counters for the MMC/SD module (inner system) and the application (user programming).

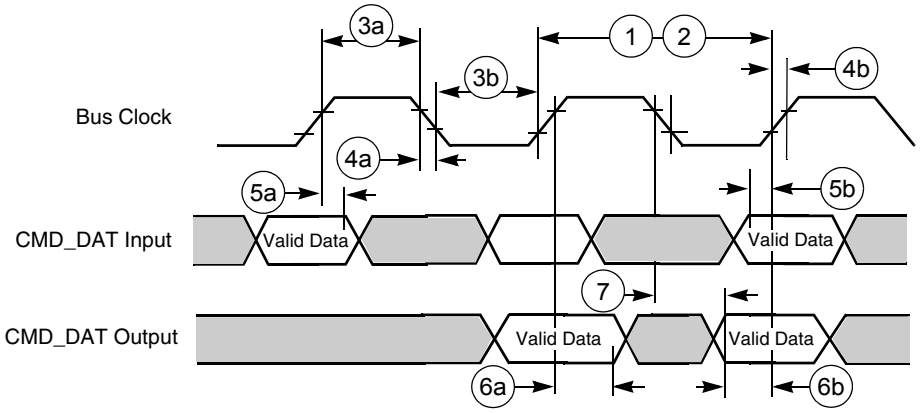


Figure 47. Chip-Select Read Cycle Timing Diagram

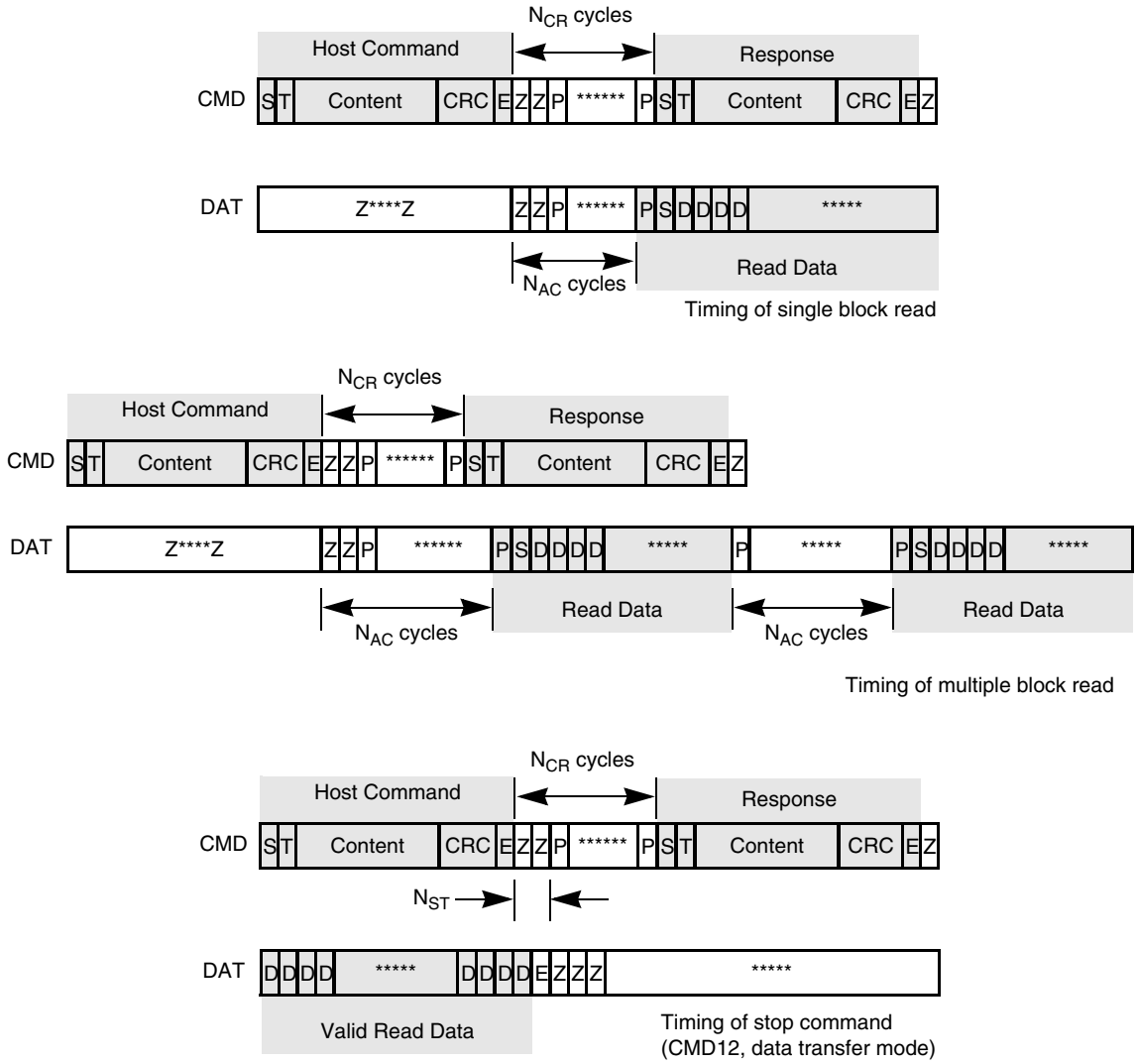


Figure 50. Timing Diagrams at Data Read

Figure 51 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

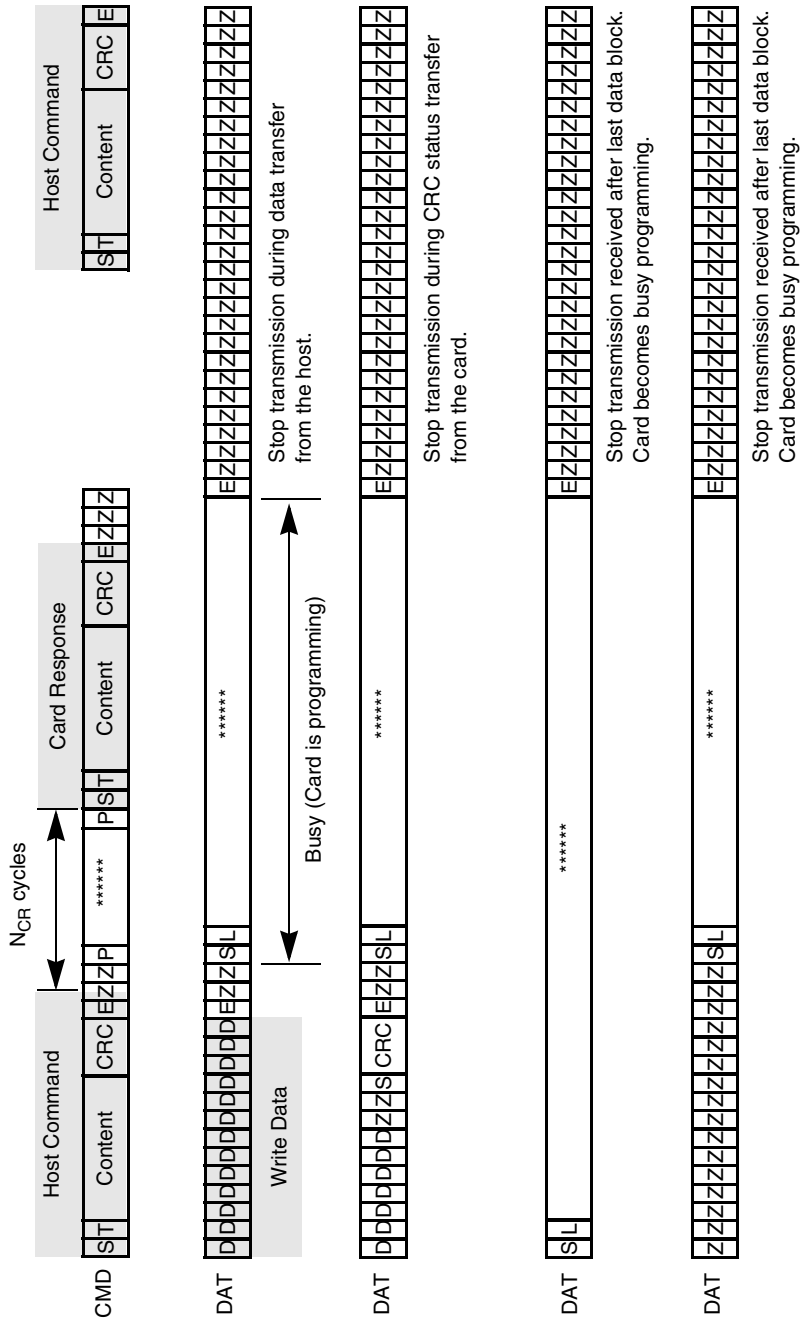


Figure 52. Stop Transmission During Different Scenarios

Table 30. Timing Values for Figure 48 through Figure 52

Parameter	Symbol	Minimum	Maximum	Unit
MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL)				
Command response cycle	NCR	2	64	Clock cycles
Identification response cycle	NID	5	5	Clock cycles
Access time delay cycle	NAC	2	TAAC + NSAC	Clock cycles

Table 31. MSHC Signal Timing Parameter Table (Continued)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	MS_SDIO output delay time[1,2]	–	3	ns
13	MS_SDIO input setup time for MS_SCLKO rising edge (RED bit = 0)[3]	18	–	ns
14	MS_SDIO input hold time for MS_SCLKO rising edge (RED bit = 0)[3]	0	–	ns
15	MS_SDIO input setup time for MS_SCLKO falling edge (RED bit = 1)[4]	23	–	ns
16	MS_SDIO input hold time for MS_SCLKO falling edge (RED bit = 1)[4]	0	–	ns

1 Loading capacitor condition is less than or equal to 30pF.

2 An external resistor (100 ~ 200 ohm) should be inserted in series to provide current control on the MS_SDIO pin, because of a possibility of signal conflict between the MS_SDIO pin and Memory Stick SDIO pin when the pin direction changes.

3 If the MSC2[RED] bit = 0, MSHC samples MS_SDIO input data at MS_SCLKO rising edge.

4 If the MSC2[RED] bit = 1, MSHC samples MS_SDIO input data at MS_SCLKO falling edge.

4.12 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in Figure 56 and the parameters are listed in Table 32.

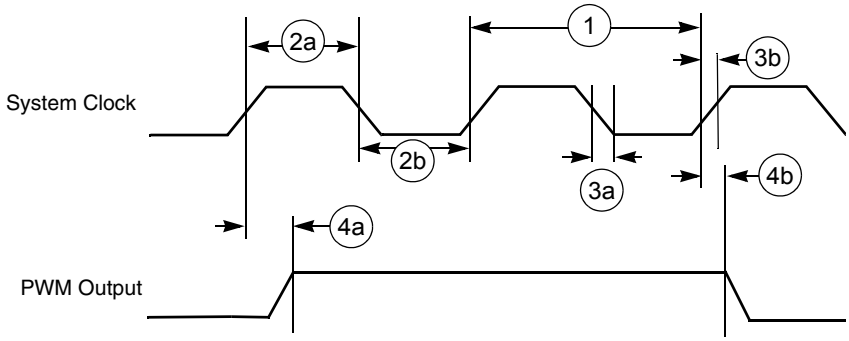


Figure 56. PWM Output Timing Diagram

Table 32. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency[1]	0	87	0	100	MHz
2a	Clock high time[1]	3.3	–	5/10	–	ns
2b	Clock low time[1]	7.5	–	5/10	–	ns
3a	Clock fall time[1]	–	5	–	5/10	ns

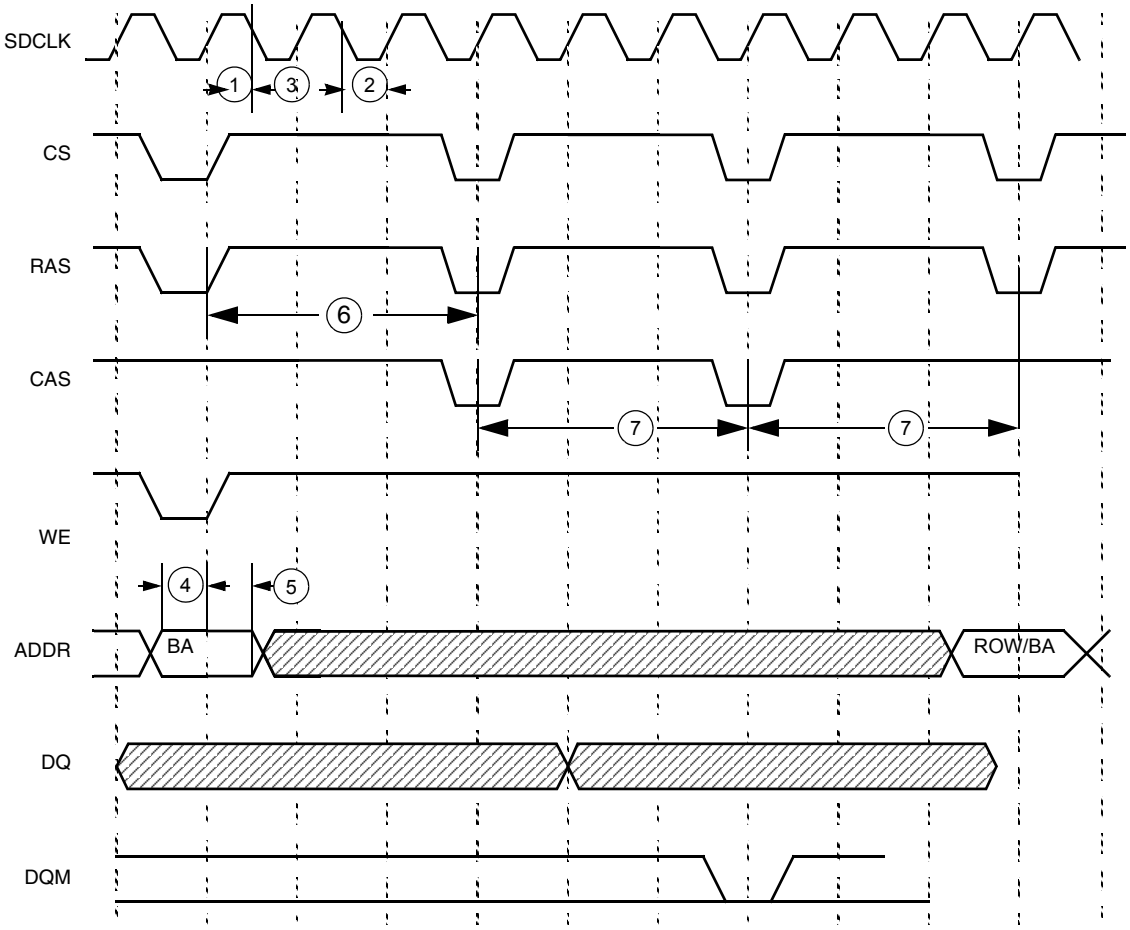


Figure 59. SDRAM Refresh Timing Diagram

Table 35. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP1}	–	ns
7	Auto precharge command period	t_{RC1}	–	t_{RC1}	–	ns

[1] t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *MC9328MX1 reference manual*.

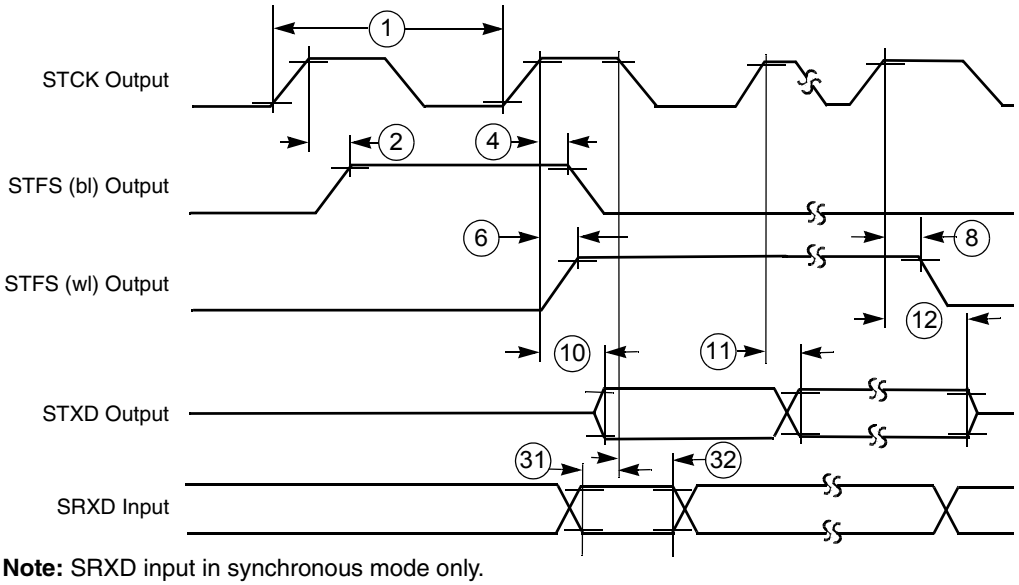
Table 38. I²C Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	Hold time (repeated) START condition	182	–	160	–	ns
2	Data hold time	0	171	0	150	ns
3	Data setup time	11.4	–	10	–	ns
4	HIGH period of the SCL clock	80	–	120	–	ns
5	LOW period of the SCL clock	480	–	320	–	ns
6	Setup time for STOP condition	182.4	–	160	–	ns

4.16 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 65 through Figure 67.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.



Note: SRXD input in synchronous mode only.

Figure 64. SSI Transmitter Internal Clock Timing Diagram

Table 40. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	STCK high to STXD high impedance	17.90	29.75	15.7	26.1	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hold time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port B Alternate Function[2])						
31	SRXD setup before STCK falling	18.81	–	16.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port B Alternate Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1 All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

2 There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

3 bl = bit length; wl = word length.

Table 41. SSI 2 (Port C Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8V +/- 0.10V		3.0V +/- 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Alternate Function)[2]						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale’s Environmental Products program, go to http://www.freescale.com/epp.

Document Number: MC9328MX1
Rev. 7
12/2006