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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx1vm15r2

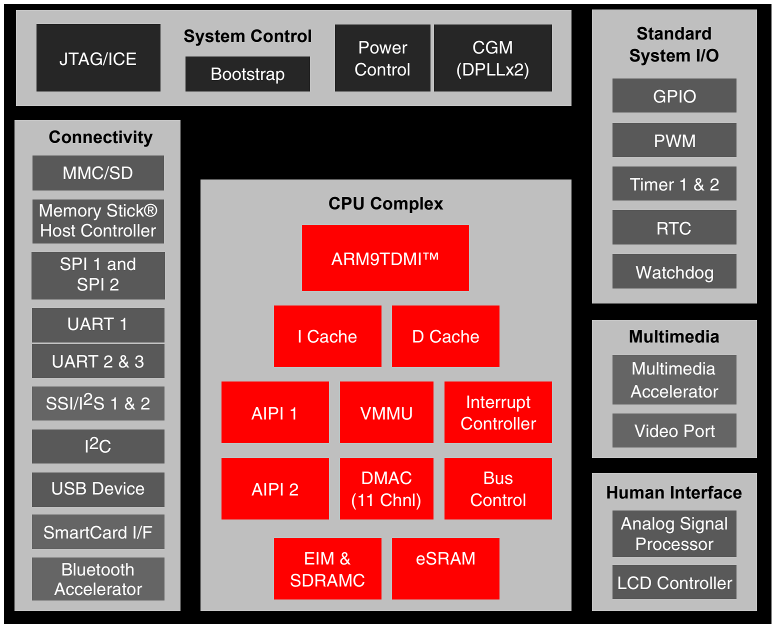


Figure 1. i.MX1 Functional Block Diagram

1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Three Universal Asynchronous Receiver/Transmitters (UART 1, UART 2, and UART3)
- Two Serial Peripheral Interfaces (SPI1 and SPI2)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)
- Direct Memory Access Controller (DMAC)
- Two Synchronous Serial Interfaces and an Inter-IC Sound (SSI1 and SSI2/I^2S) Module
- Inter-IC (I^2C) Bus Module
- Video Port

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SDIBA [3:0]	SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles.
DQM [3:0]	SDRAM data enable
$\overline{\text{CSD0}}$	SDRAM Chip-select signal which is multiplexed with the $\overline{\text{CS2}}$ signal. These two signals are selectable by programming the system control register.
$\overline{\text{CSD1}}$	SDRAM Chip-select signal which is multiplexed with $\overline{\text{CS3}}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{\text{CSD1}}$ is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins.
$\overline{\text{RAS}}$	SDRAM Row Address Select signal
$\overline{\text{CAS}}$	SDRAM Column Address Select signal
$\overline{\text{SDWE}}$	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
$\overline{\text{RESET\_SF}}$	Not Used
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 kHz crystal input
XTAL32K	32 kHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
$\overline{\text{RESET\_IN}}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
$\overline{\text{RESET\_OUT}}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{\text{RESET\_IN}}$), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{\text{TDO}}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
DMA	
$\overline{\text{DMA\_REQ}}$	$\overline{\text{DMA Request}}$—external DMA request signal. Multiplexed with SPI1_SPI_RDY.
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{\text{ECB}}$, $\overline{\text{LBA}}$, BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SIM	
SIM_CLK	SIM Clock
SIM_RST	SIM Reset
SIM_RX	Receive Data

Table 3. MC9328MX1 Signal Multiplexing Scheme

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	K8	NVDD1	Static										
NVDD1	B1	A24	O		ETMTRACESYNC	O	PA0	69K	SPI2_CLK			L	A24
NVDD1	C2	D31	I/O	69K								Pull-H	
NVDD1	C1	A23	O		ETMTRACECLK	O	PA31	69K				L	A23
NVDD1	D2	D30	I/O	69K								Pull-H	
NVDD1	D1	A22	O		ETMPIPESTAT2	O	PA30	69K				L	A22
NVDD1	D3	D29	I/O	69K								Pull-H	
NVDD1	E2	A21	O		ETMPIPESTAT1	O	PA29	69K				L	A21
NVDD1	E3	D28	I/O	69K								Pull-H	
NVDD1	E1	A20	O		ETMPIPESTAT0	O	PA28	69K				L	A20
NVDD1	F2	D27	I/O	69K								Pull-H	
NVDD1	F4	A19	O		ETMTRACEPKT3	O	PA27	69K				L	A19
NVDD1	E4	D26	I/O	69K								Pull-H	
	A1	VSS	Static										
NVDD1	H5	NVDD1	Static										
NVDD1	F1	A18	O		ETMTRACEPKT2	O	PA26	69K				L	A18
NVDD1	F3	D25	I/O	69K								Pull-H	
NVDD1	G2	A17	O		ETMTRACEPKT1	O	PA25	69K				L	A17
NVDD1	G3	D24	I/O	69K								Pull-H	
NVDD1	F5	A16	O		ETMTRACEPKT0	O	PA24	69K				L	A16
NVDD1	G4	D23	I/O	69K								Pull-H	
NVDD1	G1	A15	O									L	
NVDD1	H2	D22	I/O	69K								Pull-H	
NVDD1	H3	A14	O									L	

Table 12. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
4a	Clock[1] rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock[1] rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock[1] fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock[1] fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock[1] rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock[1] rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock[1] fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock[1] fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock[1] fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock[1] fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock[1] rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock[1] rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock[1] rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock[1] fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock[1] fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	–	–	5.5	–	–	ns
8b	Read Data hold time	0	–	–	0	–	–	ns
9a	Clock[1] rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock[1] fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock[1] rise to Write Data Invalid	1.63	–	–	1.62	–	–	ns
10a	$\overline{\text{DTACK}}$ setup time	2.52	–	–	2.5	–	–	ns

[1] Clock refers to the system clock signal, HCLK, generated from the System DPLL

4.4.1 $\overline{\text{DTACK}}$ Signal Description

The $\overline{\text{DTACK}}$ signal is the external input data acknowledge signal. When using the external $\overline{\text{DTACK}}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{\text{DTACK}}$ signal after 1022 HCLK counts have elapsed. Only the CS5 group supports DTACK signal function when the external DTACK signal is used for data acknowledgement.

4.4.2 $\overline{\text{DTACK}}$ Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. OE and EB assertion time is programmable by OEA bit in CS5L register. EB assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and CS asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA

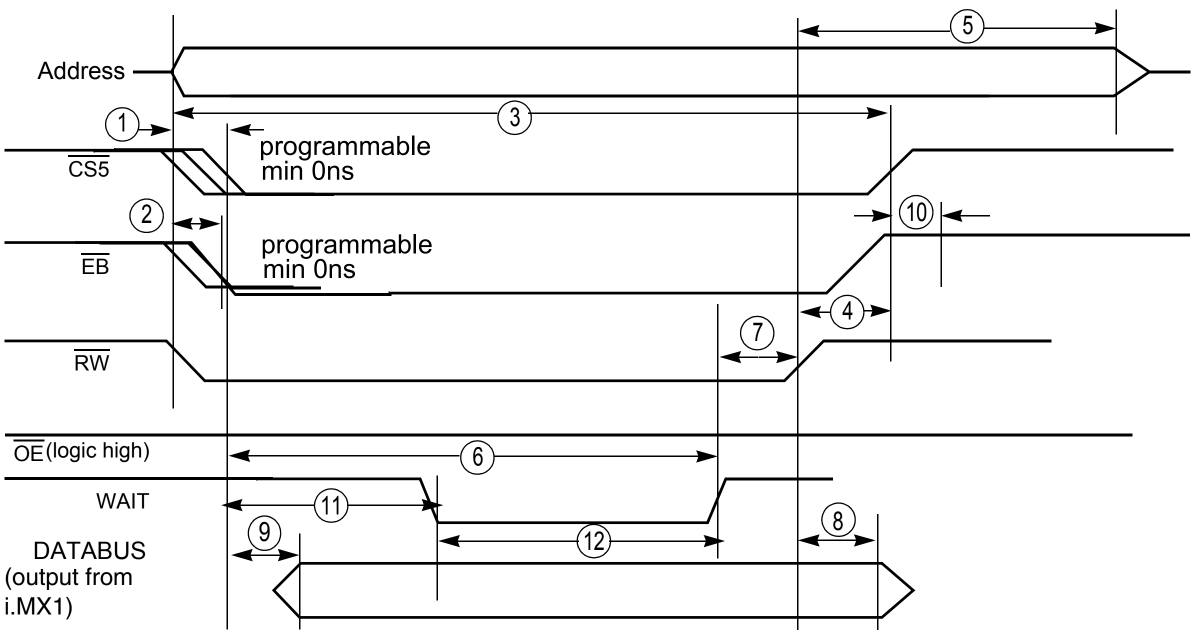


Figure 8. WAIT Write Cycle without DMA

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	CS5 assertion time	See note 2	–	ns
2	EB assertion time	See note 2	–	ns
3	CS5 pulse width	3T	–	ns
4	RW negated before CS5 is negated	2.5T-0.29	2.5T+0.68	ns
5	RW negated to Address inactive	67.28	–	ns
6	Wait asserted after CS5 asserted	–	1020T	ns

Table 16. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{\text{CS5}}$ assertion time	See note 2	–	ns
2	$\overline{\text{EB}}$ assertion time	See note 2	–	ns
3	$\overline{\text{CS5}}$ pulse width	3T	–	ns
4	$\overline{\text{RW}}$ negated before $\overline{\text{CS5}}$ is negated	2.5T-0.29	2.5T+0.68	ns
5	Address inactived after $\overline{\text{CS}}$ negated	–	0.93	ns
6	Wait asserted after $\overline{\text{CS5}}$ asserted	–	1020T	ns
7	Wait asserted to $\overline{\text{RW}}$ negated	T+2.15	2T+7.34	ns
8	Data hold timing after $\overline{\text{RW}}$ negated	24.87	–	ns
9	Data ready after $\overline{\text{CS5}}$ is asserted	–	T	ns
10	$\overline{\text{CS}}$ deactive to next $\overline{\text{CS}}$ active	T	–	ns
11	$\overline{\text{EB}}$ negate after $\overline{\text{CS}}$ negate	1.5T+0.74	1.5T+2.35	
12	Wait becomes low after $\overline{\text{CS5}}$ asserted	0	1019T	ns
13	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{\text{CS5}}$ assertion can be controlled by CSA bits. $\overline{\text{EB}}$ assertion also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{\text{RW}}$ asserts at the start of write access cycle.
4.The external wait input requirement is eliminated when $\overline{\text{CS5}}$ is programmed to use internal wait state.

4.4.3 EIM External Bus Timing

The External Interface Module (EIM) is the interface to devices external to the i.MX1, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.

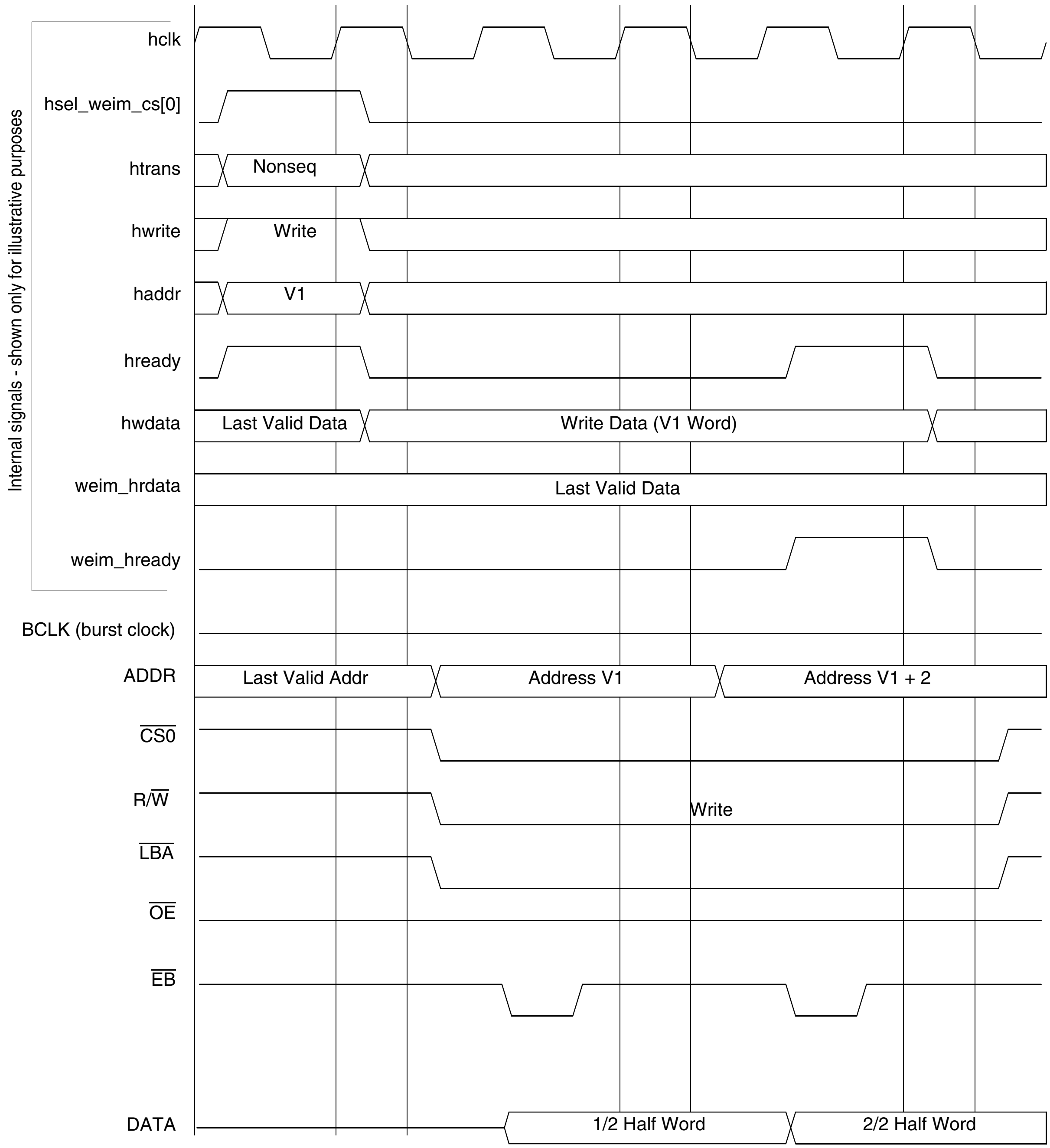
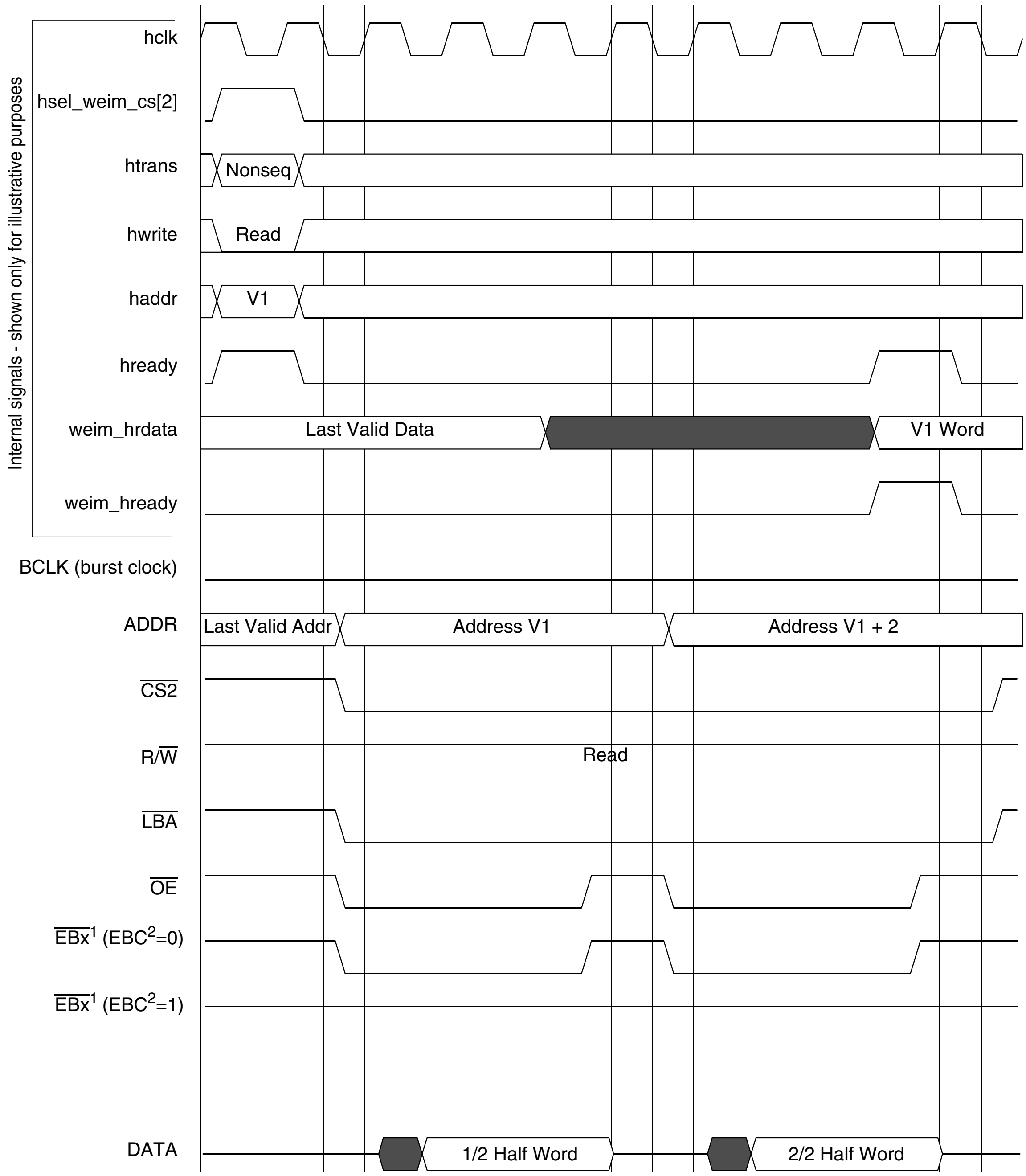


Figure 13. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF

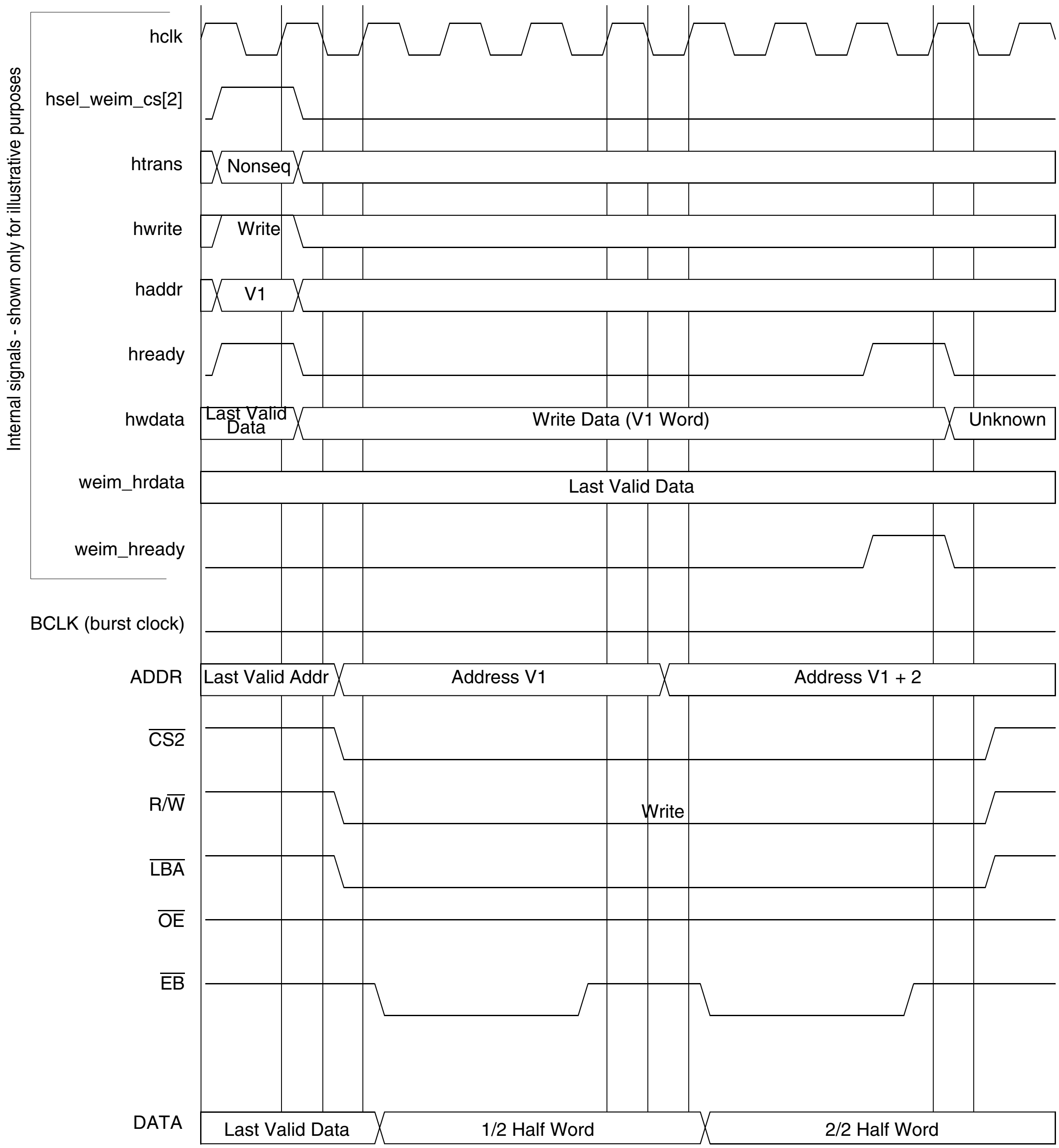
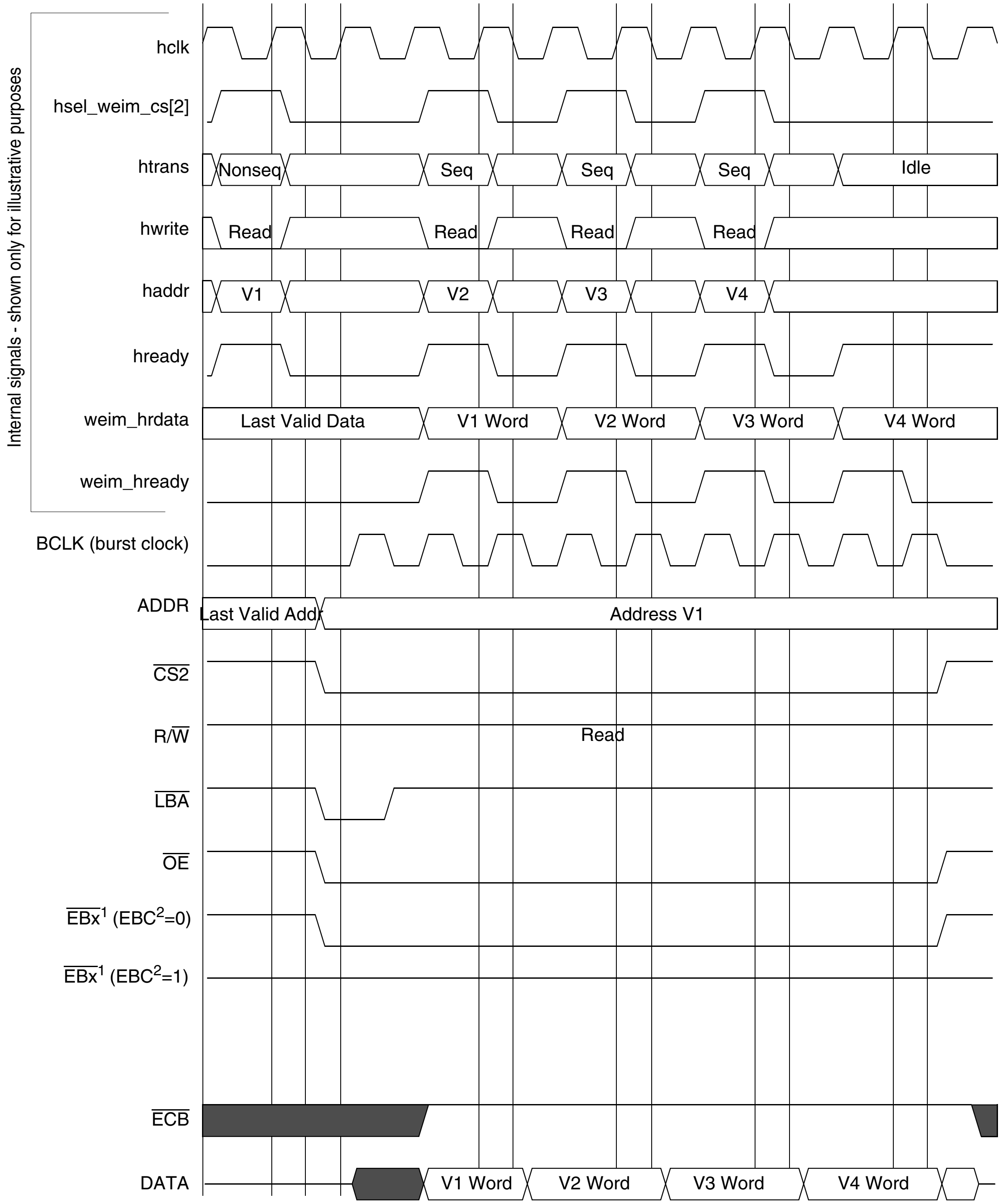


Figure 20. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 29. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

Table 19. Pen ADC Test Conditions

Vp max	1800 mV	ip max	+7 µA
Vp min	GND	ip min	1.5 µA
Vn	GND	in	1.5 µA
Sample frequency		12 MHz	
Sample rate		1.2 KHz	
Input frequency		100 Hz	
Input range		0–1800 mV	
Note: Ru1 = Ru2 = 200K			

Table 20. Pen ADC Absolute Rating

ip max	+9.5 µA
ip min	-2.5 µA
in max	+9.5 µA
in min	-2.5 µA

4.6 ASP Touch Panel Controller

The following sections contain the electrical specifications of the ASP touch panel controller. The value of parameters and their corresponding measuring conditions are mentioned as well.

4.6.1 Electrical Specifications

Test conditions: Temperature = 25º C, QVDD = 1800mV.

Table 21. ASP Touch Panel Controller Electrical Spec

Parameter	Minimum	Typical	Maximum	Unit
Offset	–	32768	–	–
Offset Error	–	–	8199	–
Gain	–	13.65	–	mV^{-1}
Gain Error	–	–	33%	–
DNL	8	9	–	Bits
INL	–	0	–	Bits
Accuracy (without missing code)	8	9	–	Bits
Operating Voltage Range (Pen)	–	–	QVDD	mV
Operating Voltage Range (U)	Negative QVDD	–	QVDD	mV
On-resistance of switches SW[8:1]	–	10	–	Ohm

Note that QVDD should be 1800mV.

4.6.2 Gain Calculations

The ideal mapping of input voltage to output digital sample is defined as follows:

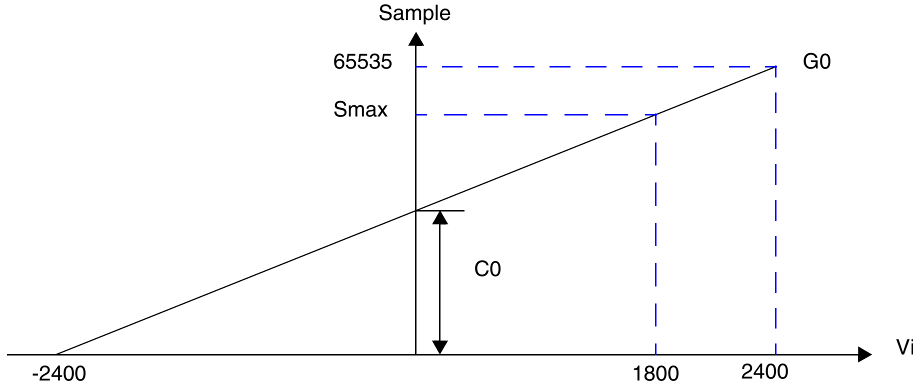


Figure 34. Gain Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65\text{mV}^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

4.6.3 Offset Calculations

The ideal mapping of input voltage to output digital sample is defined as:

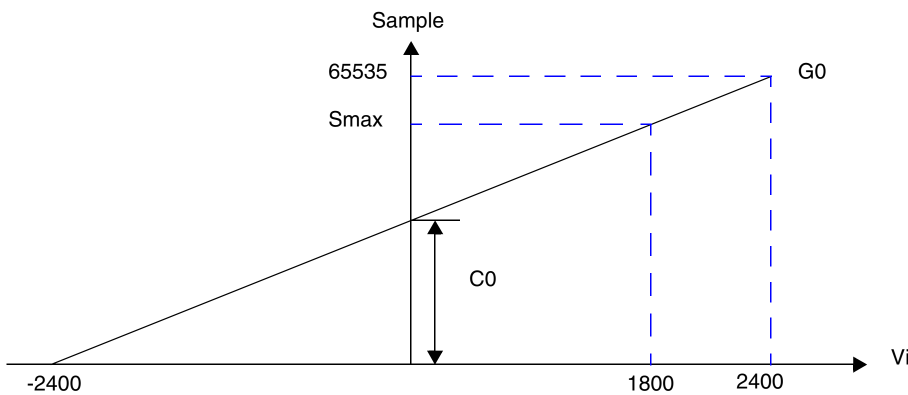


Figure 35. Offset Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65\text{mV}^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

4.6.4 Gain Error Calculations

Gain error calculations are made using the information in this section.

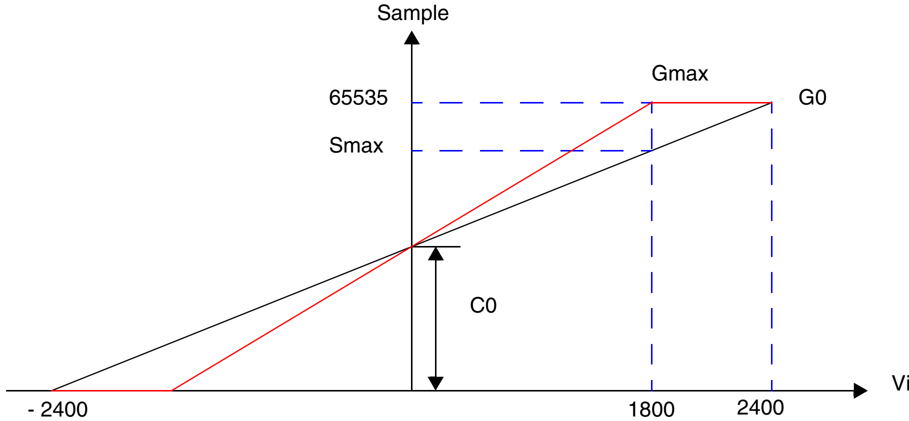


Figure 36. Gain Error Calculations

Assuming the offset remains unchanged, the mapping is rotated around y-intercept to determine the maximum gain allowed. This occurs when the sample at 1800mV has just reached the ceiling of the 16-bit range, 65535.

Maximum Offset G_{max},

G_{max} $= (65535 - C_{0)} / 1800$
$= (65535 - 32767) / 1800$
$= 18.20$

Gain Error G_r,

G_r $= (G_{max} - G_0) / G_0 * 100\%$
$= (18.20 - 13.65) / 13.65 * 100\%$
$= 33\%$

4.7 Bluetooth Accelerator

CAUTION

On-chip accelerator hardware is not supported by software. An external Bluetooth chip interfaced to a UART is recommended.

The Bluetooth Accelerator (BTA) radio interface supports the Wireless RF Transceiver, MC13180 using an SPI interface. This section provides the data bus timing diagrams and SPI interface timing diagrams shown in Figure 37 and Figure 38, and the associated parameters shown in Table 22 and Table 23.

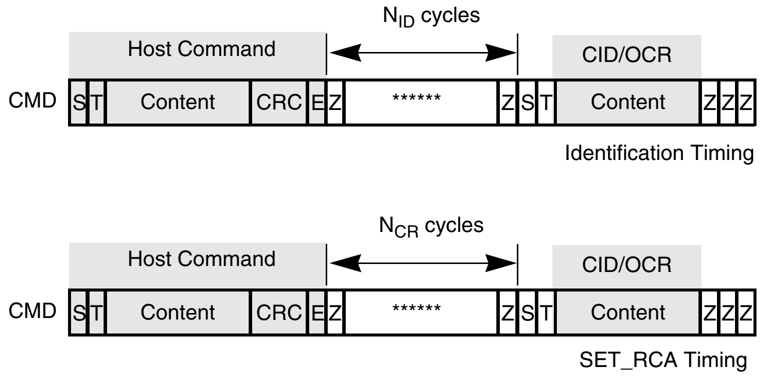


Figure 48. Timing Diagrams at Identification Mode

After a card receives its RCA, it switches to data transfer mode. As shown on the first diagram in Figure 49, SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods N_{RC} and N_{CC}.

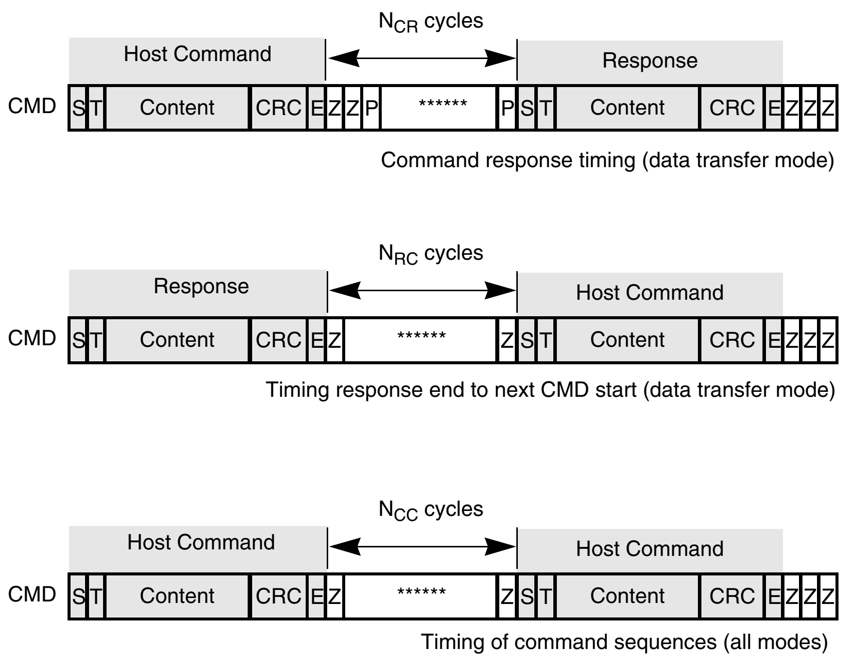


Figure 49. Timing Diagrams at Data Transfer Mode

Figure 50 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC}, beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

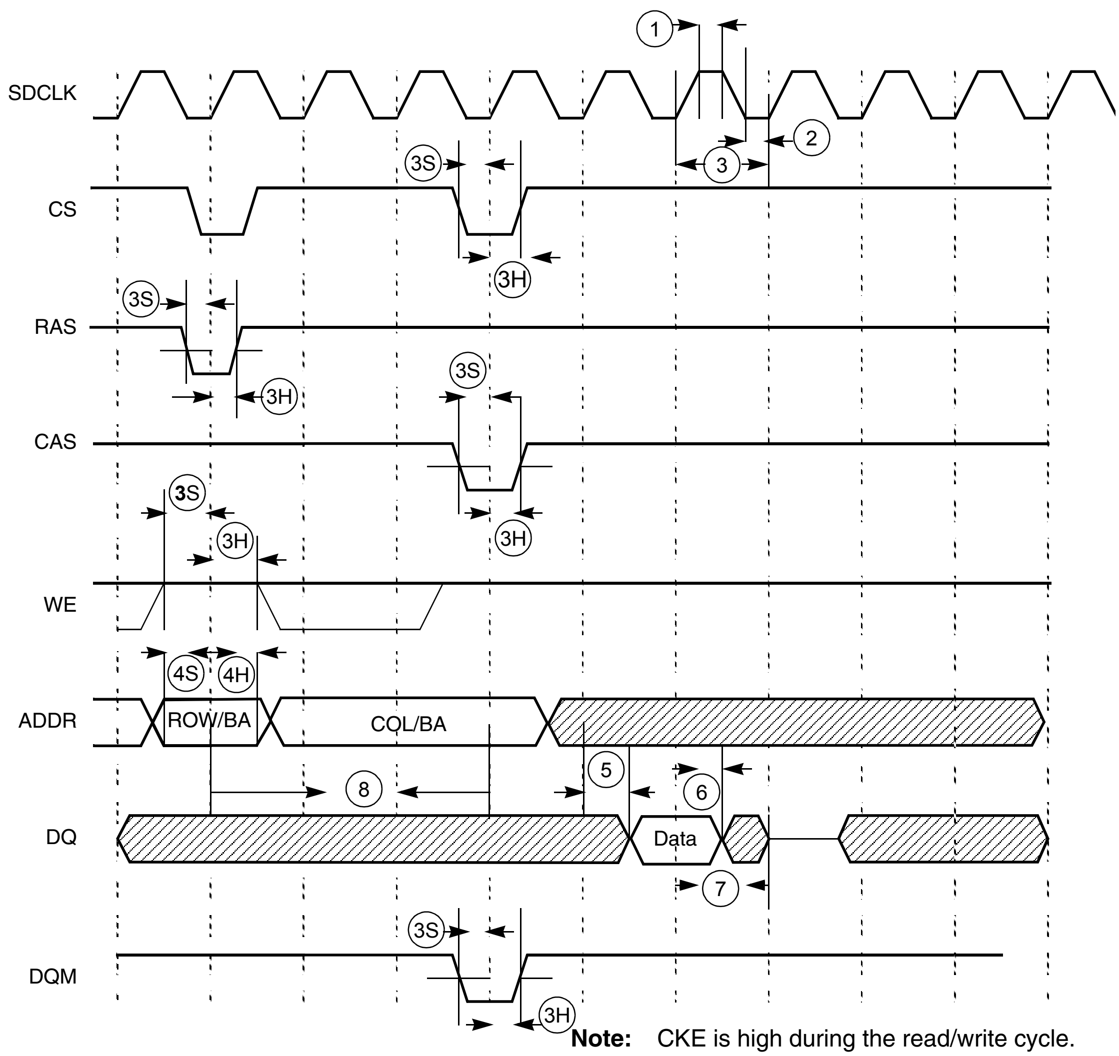
Table 32. PWM Output Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
3b	Clock rise time[1]	–	6.67	–	5/10	ns
4a	Output delay time[1]	5.7	–	5	–	ns
4b	Output setup time[1]	5.7	–	5	–	ns

[1] C_L of PWMO = 30 pF

4.13 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.



Note: CKE is high during the read/write cycle.

Figure 57. SDRAM Read Cycle Timing Diagram

Table 33. SDRAM Read Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	3.42	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	2.28	–	2	–	ns
4S	Address setup time	3.42	–	3	–	ns
4H	Address hold time	2.28	–	2	–	ns
5	SDRAM access time (CL = 3)	–	6.84	–	6	ns
5	SDRAM access time (CL = 2)	–	6.84	–	6	ns
5	SDRAM access time (CL = 1)	–	22	–	22	ns
6	Data out hold time	2.85	–	2.5	–	ns
7	Data out high-impedance time (CL = 3)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 2)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 1)	–	22	–	22	ns
8	Active to read/write command period (RC = 1)	t_{RCD}[1]	–	t_{RCD1}	–	ns

[1] t_{RCD} = SDRAM clock cycle time. This settings can be found in the *MC9328MX1 reference manua*l.

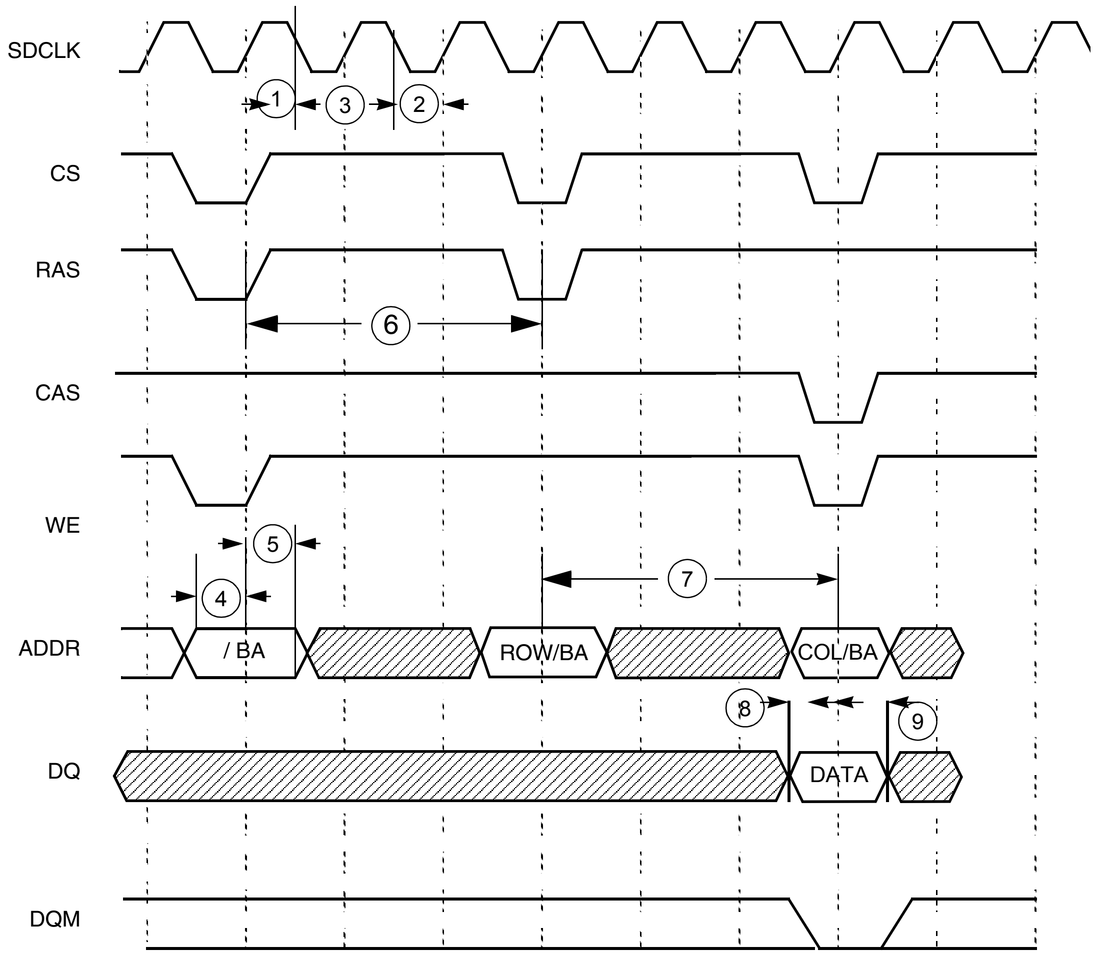


Figure 58. SDRAM Write Cycle Timing Diagram

Table 34. SDRAM Write Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period[1]	t_{RP}[2]	–	t_{RP2}	–	ns
7	Active to read/write command delay	t_{RCD2}	–	t_{RCD2}	–	ns
8	Data setup time	4.0	–	2	–	ns
9	Data hold time	2.28	–	2	–	ns

[1] Precharge cycle timing is included in the write timing diagram.

[2] t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the *MC9328MX1 reference manual.*

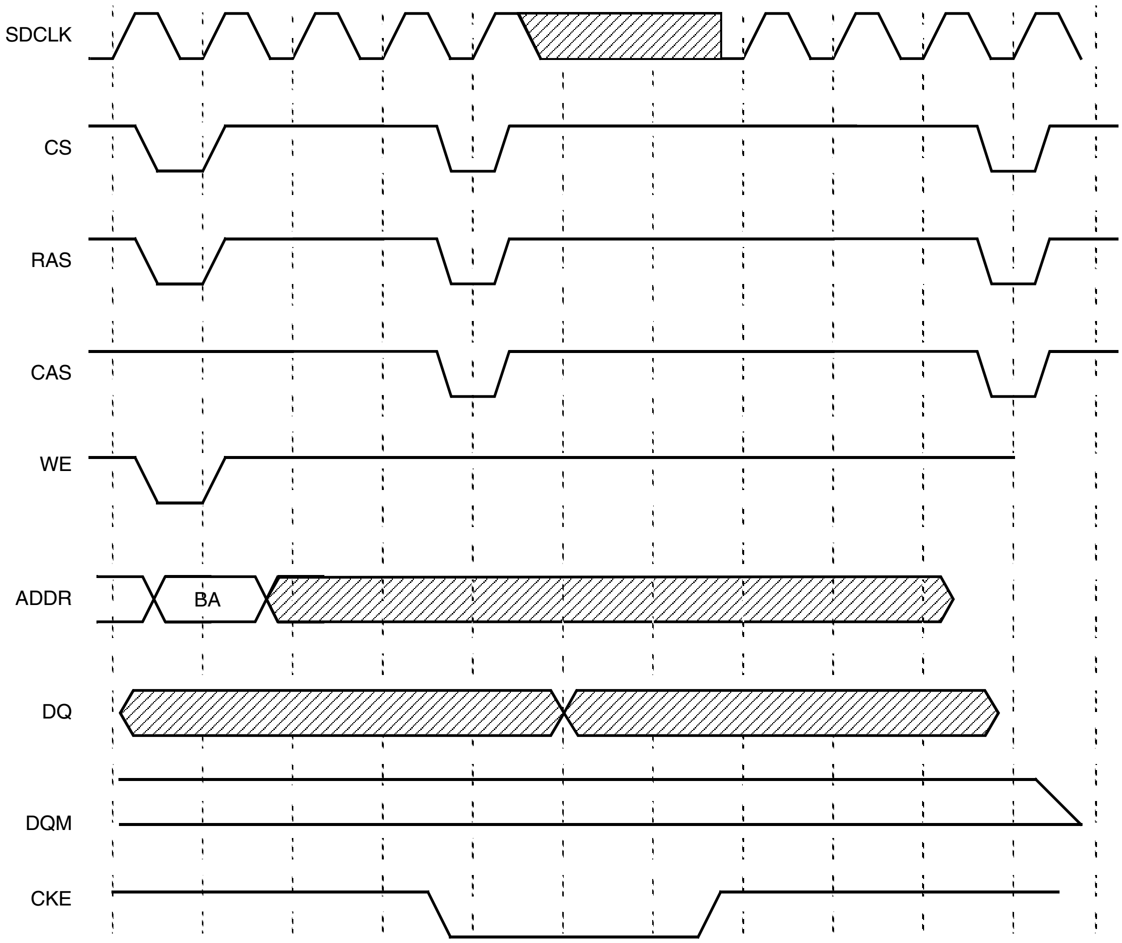


Figure 60. SDRAM Self-Refresh Cycle Timing Diagram

4.14 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers, and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, however, because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

Table 40. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port B Alternate Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port B Alternate Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns