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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx1vm20

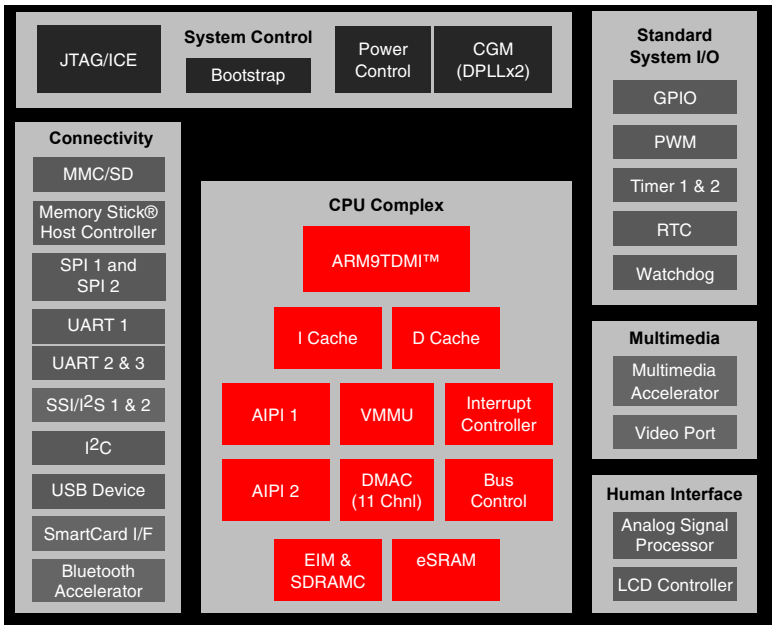


Figure 1. i.MX1 Functional Block Diagram

1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Three Universal Asynchronous Receiver/Transmitters (UART 1, UART 2, and UART3)
- Two Serial Peripheral Interfaces (SPI1 and SPI2)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)
- Direct Memory Access Controller (DMAC)
- Two Synchronous Serial Interfaces and an Inter-IC Sound (SSI1 and SSI2/I^2S) Module
- Inter-IC (I^2C) Bus Module
- Video Port

in the system, these Bluetooth pins can be used as general purpose I/O pins and BTRFVDD can be used as other NVDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 5. Recommended Operating Range

Symbol	Rating	Minimum	Maximum	Unit
T_A	Operating temperature range MC9328MX1VM20\MC9328MX1VM15	0	70	°C
T_A	Operating temperature range MC9328MX1DVM20\MC9328MX1DVM15	-30	70	°C
T_A	Operating temperature range MC9328MX1CVM15	-40	85	°C
NVDD	I/O supply voltage (if using MSHC, CSI, SPI, BTA, LCD, and USBd which are only 3 V interfaces)	2.70	3.30	V
NVDD	I/O supply voltage (if not using the peripherals listed above)	1.70	3.30	V
QVDD	Internal supply voltage (Core = 150 MHz)	1.70	1.90	V
QVDD	Internal supply voltage (Core = 200 MHz)	1.80	2.00	V
AVDD	Analog supply voltage	1.70	3.30	V

3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the “Power-Up Sequence” section of application note AN2537 on the i.MX applications processor website.

3.4 DC Electrical Characteristics

Table 6 contains both maximum and minimum DC characteristics of the i.MX1 processor.

Table 6. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Min	Typical	Max	Unit
Iop	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, MPEG4 decoding playback from external memory card to both external SSI audio decoder and driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	–	QVDD at 1.8V = 120mA; NVDD+AVDD at 3.0V = 30mA	–	mA
$Sidd_1$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 25°C)	–	25	–	µA
$Sidd_2$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 55°C)	–	45	–	µA
$Sidd_3$	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 25°C)	–	35	–	µA

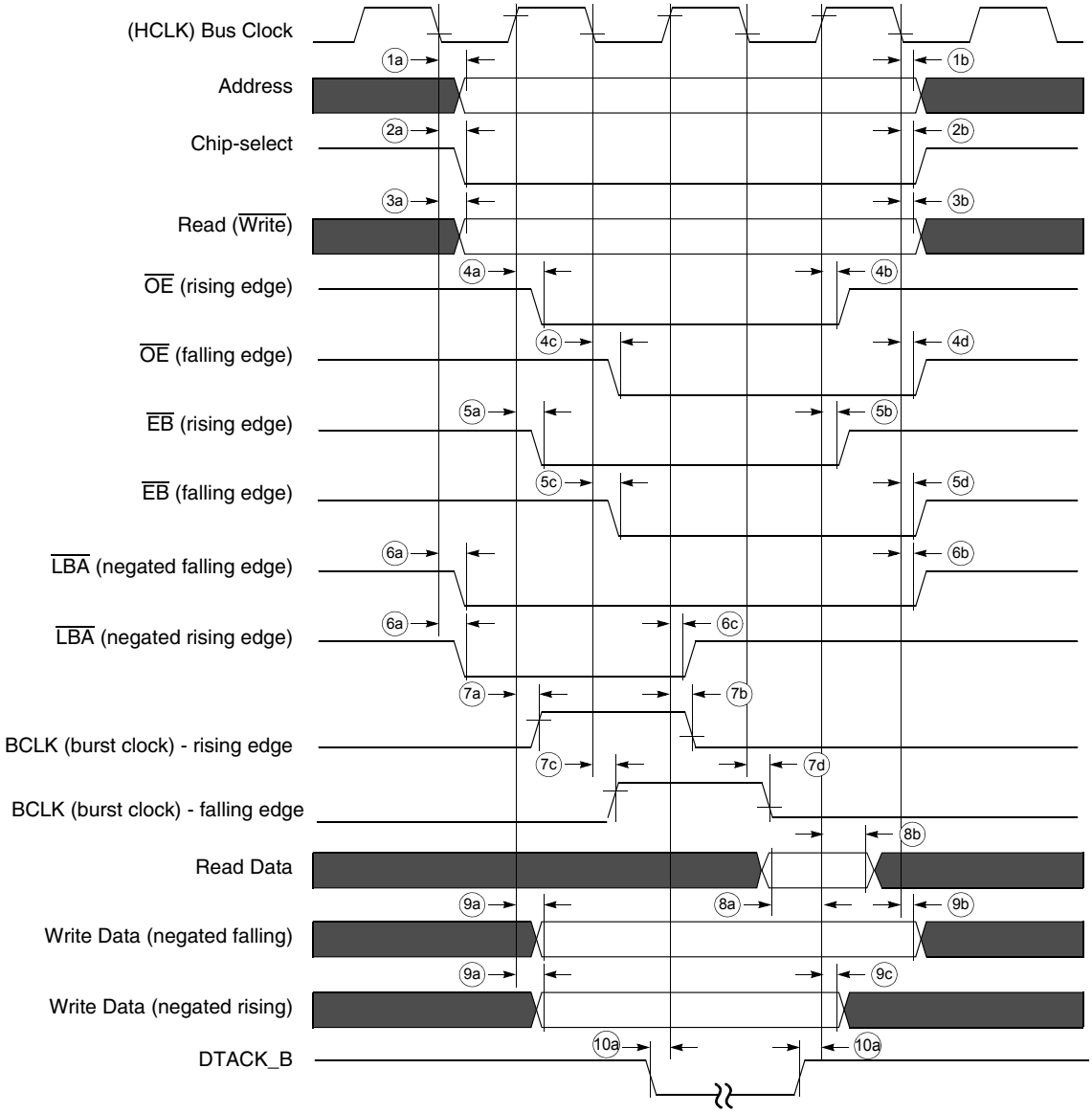
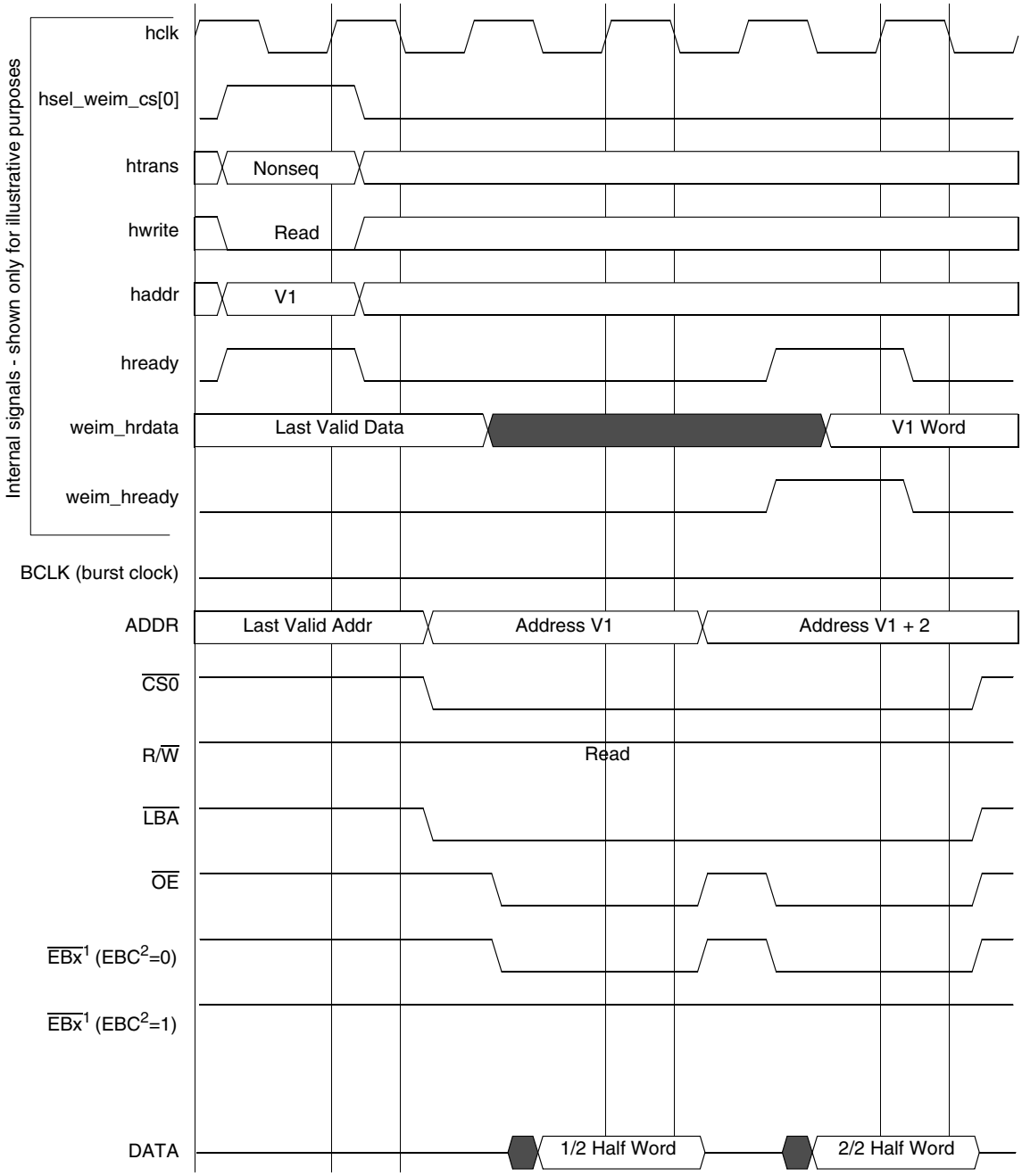


Figure 5. EIM Bus Timing Diagram

Table 12. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	2.48	3.31	9.11	2.4	3.2	8.8	ns
1b	Clock fall to address invalid	1.55	2.48	5.69	1.5	2.4	5.5	ns
2a	Clock fall to chip-select valid	2.69	3.31	7.87	2.6	3.2	7.6	ns
2b	Clock fall to chip-select invalid	1.55	2.48	6.31	1.5	2.4	6.1	ns
3a	Clock fall to Read (Write) Valid	1.35	2.79	6.52	1.3	2.7	6.3	ns
3b	Clock fall to Read (Write) Invalid	1.86	2.59	6.11	1.8	2.5	5.9	ns



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 12. WSC = 1, OEA = 1, A.WORD/E.HALF

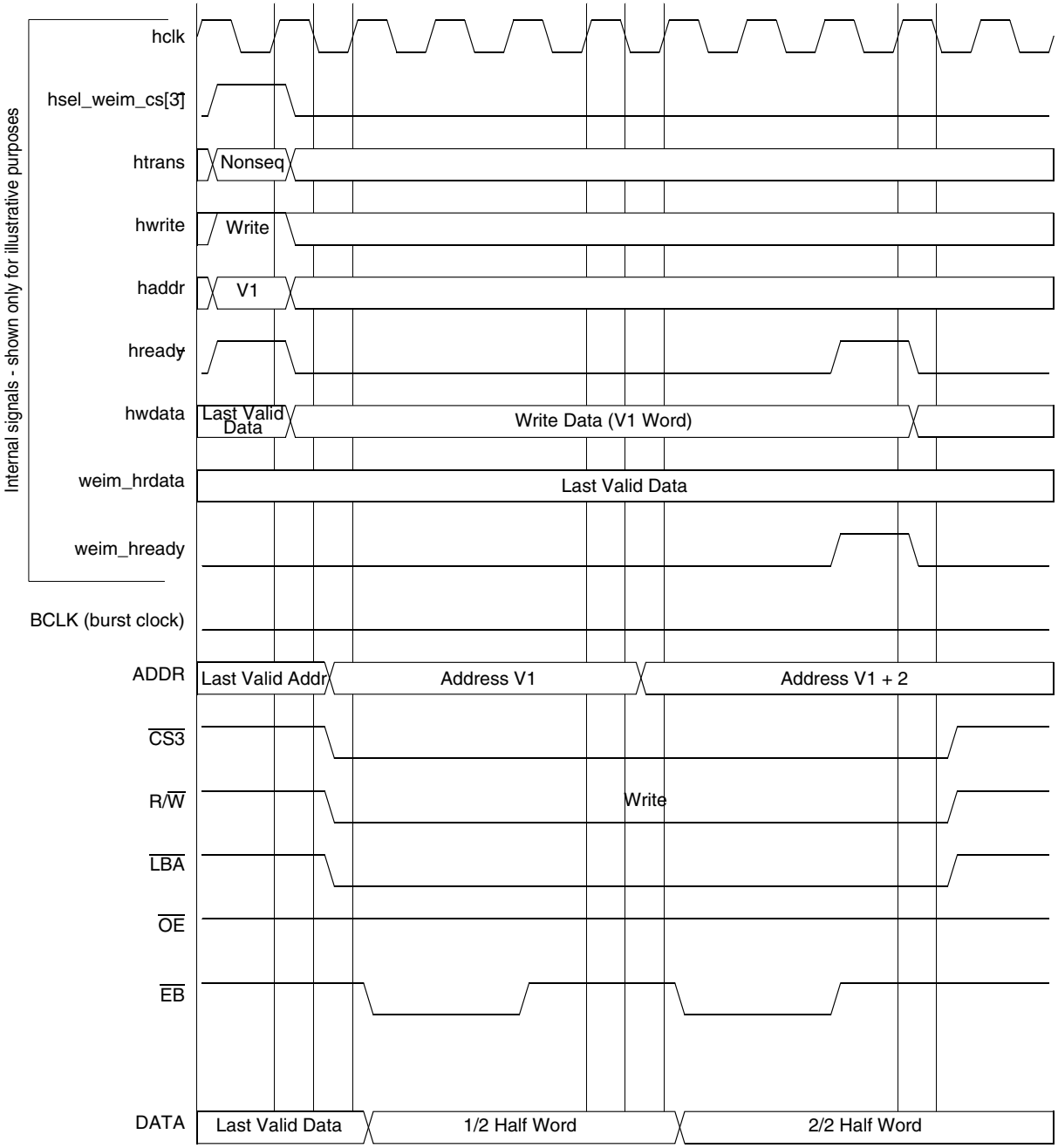
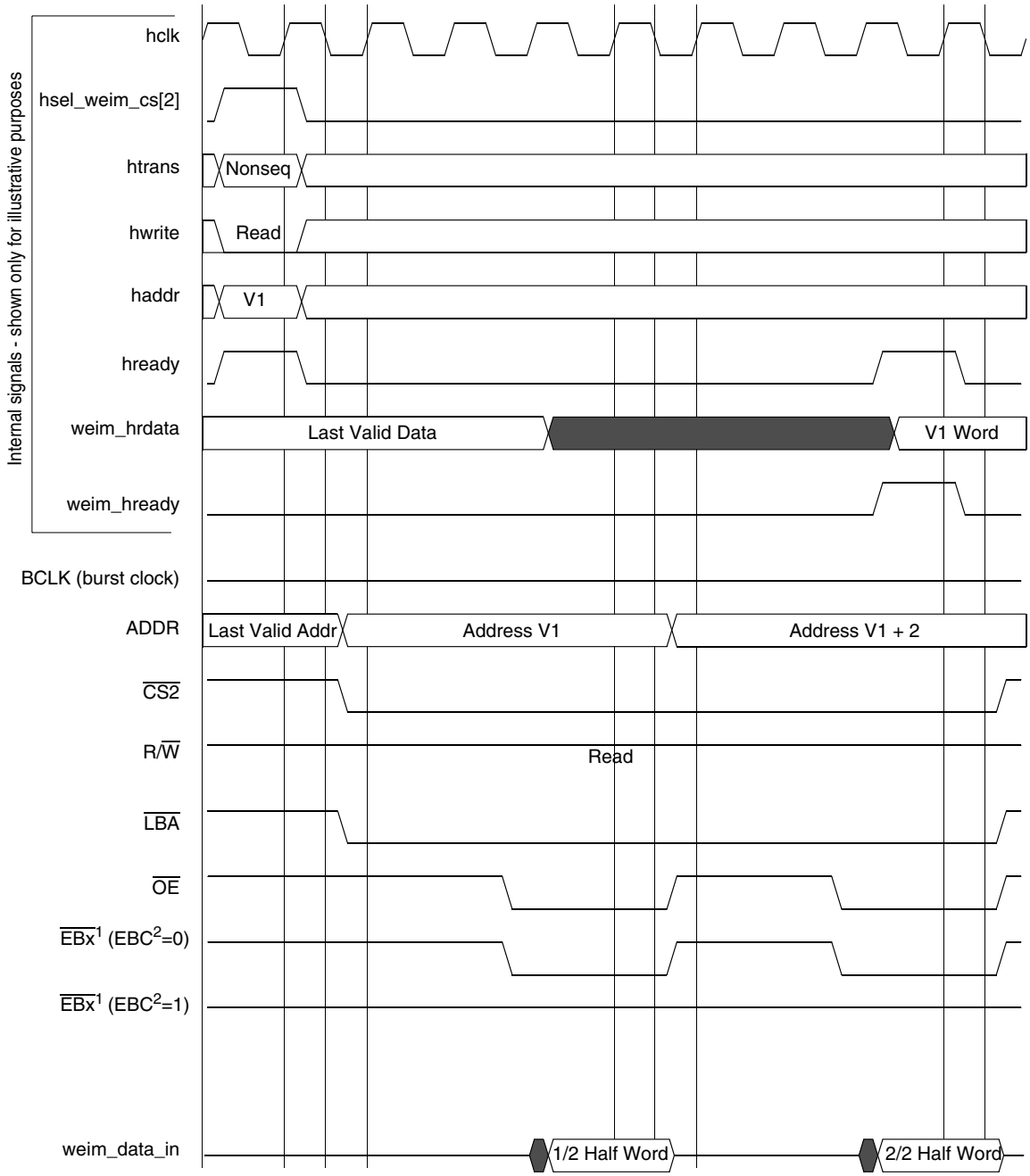
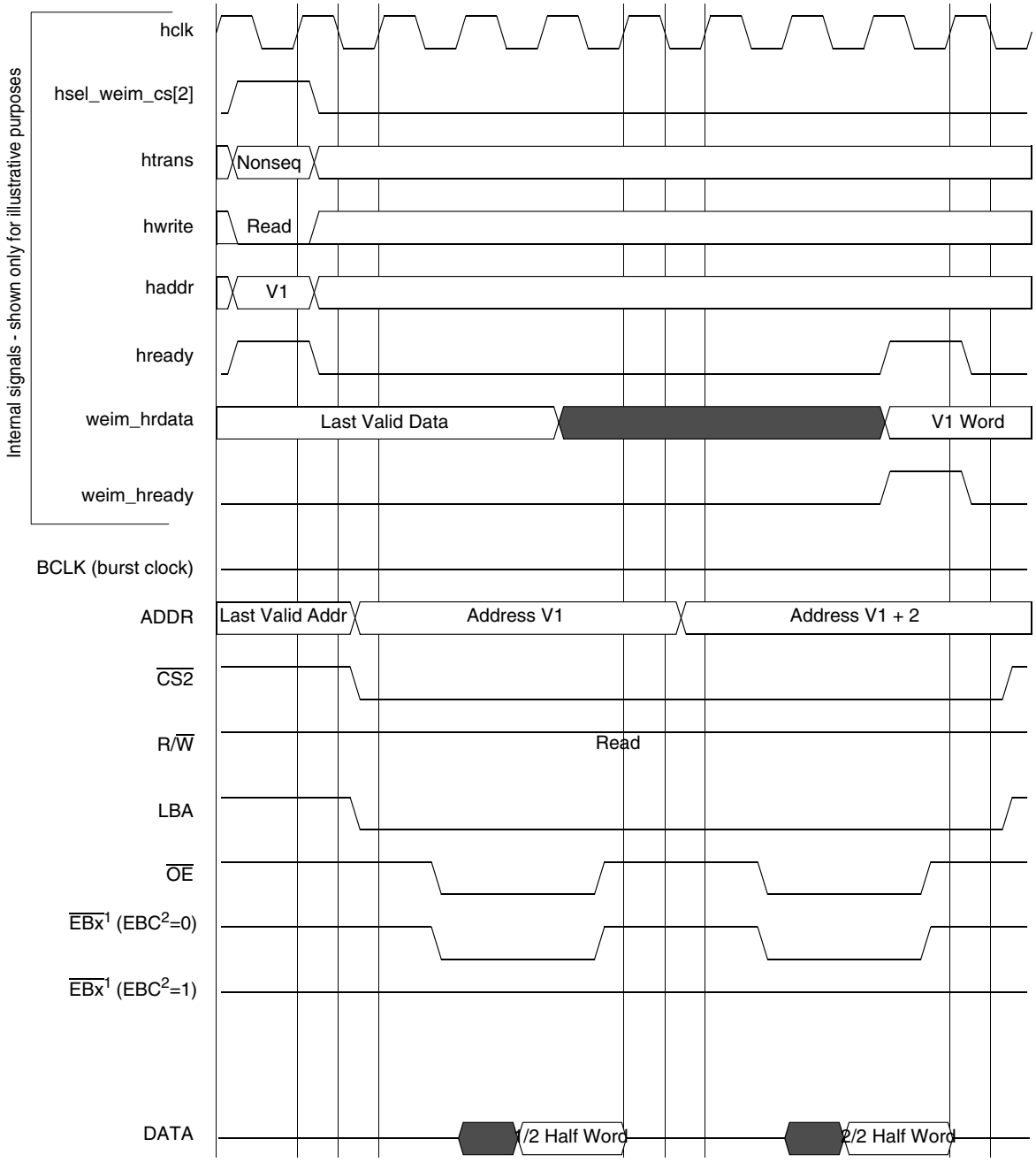


Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 16. WSC = 3, OEA = 4, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

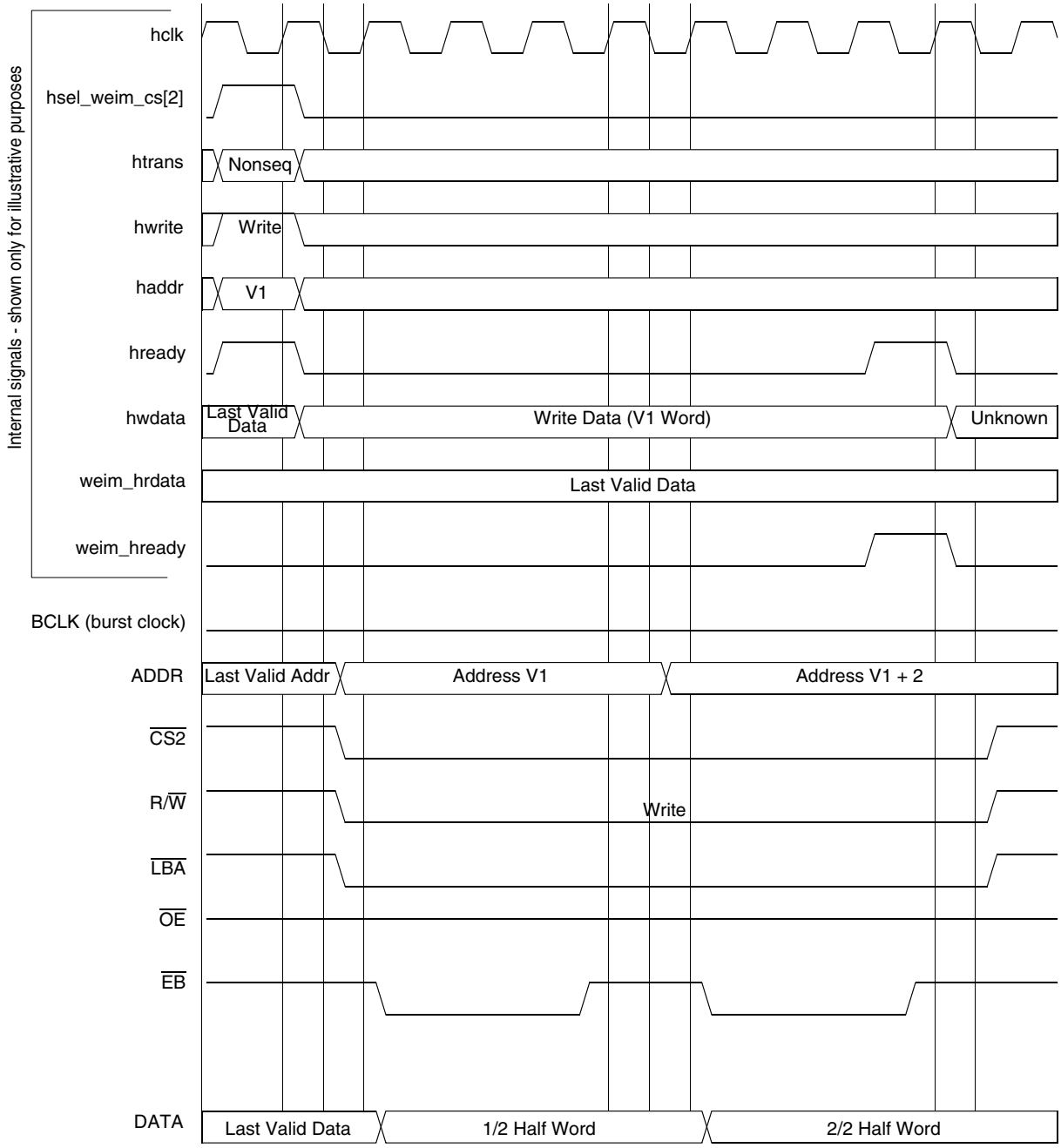
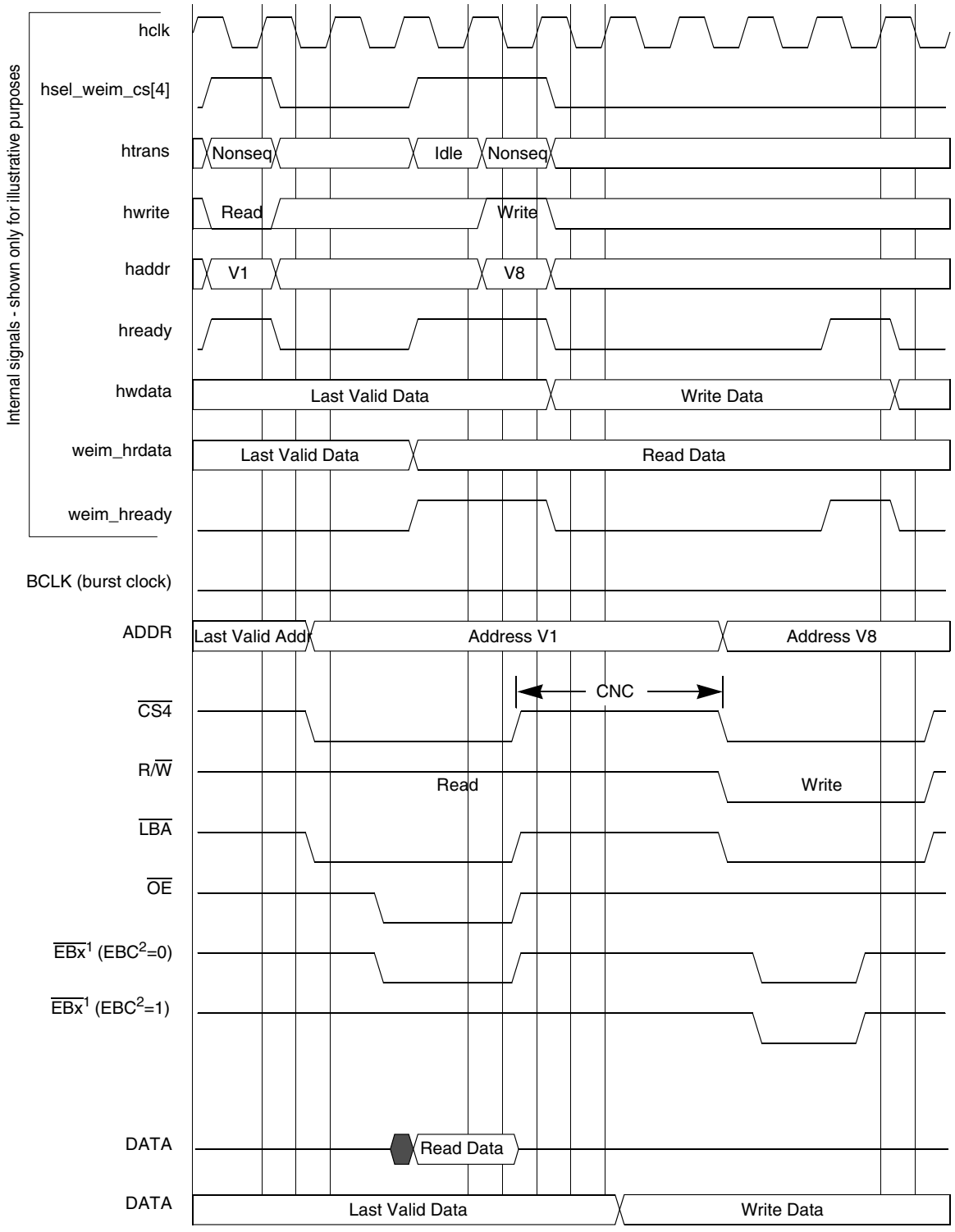
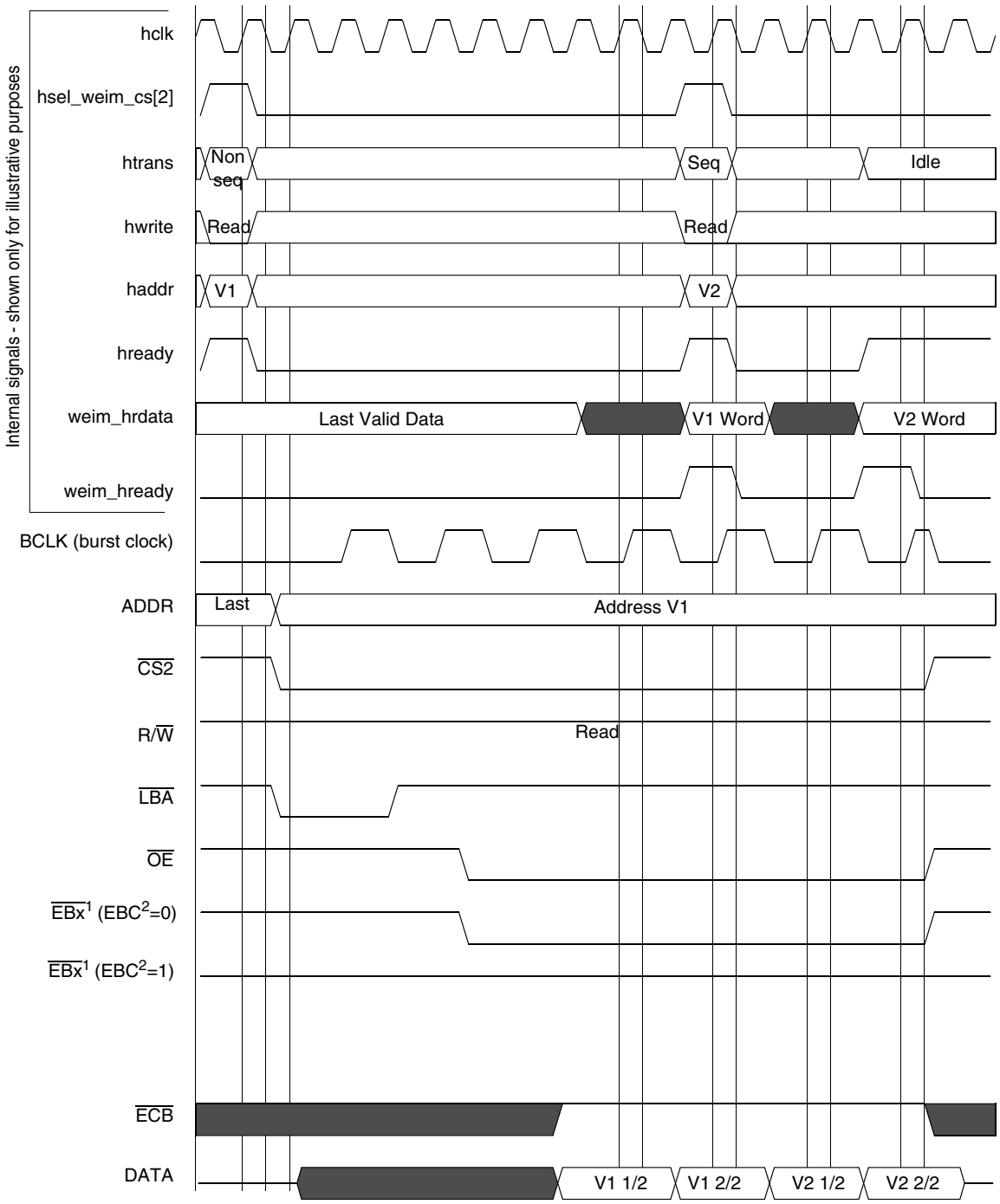


Figure 20. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 27. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 31. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF

4.6.2 Gain Calculations

The ideal mapping of input voltage to output digital sample is defined as follows:

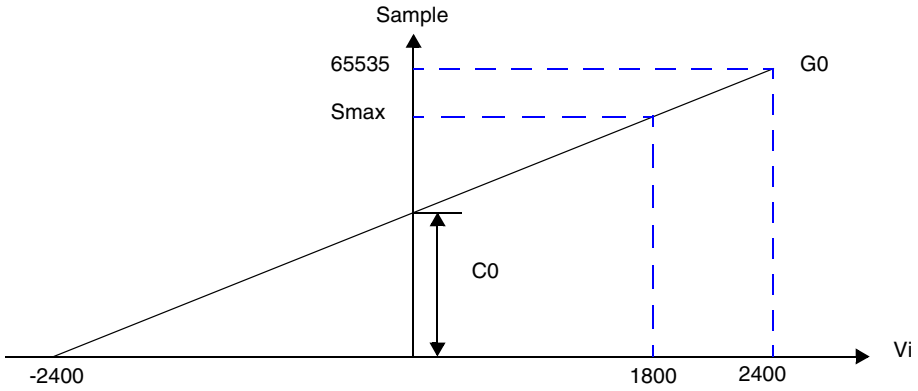


Figure 34. Gain Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

4.6.3 Offset Calculations

The ideal mapping of input voltage to output digital sample is defined as:

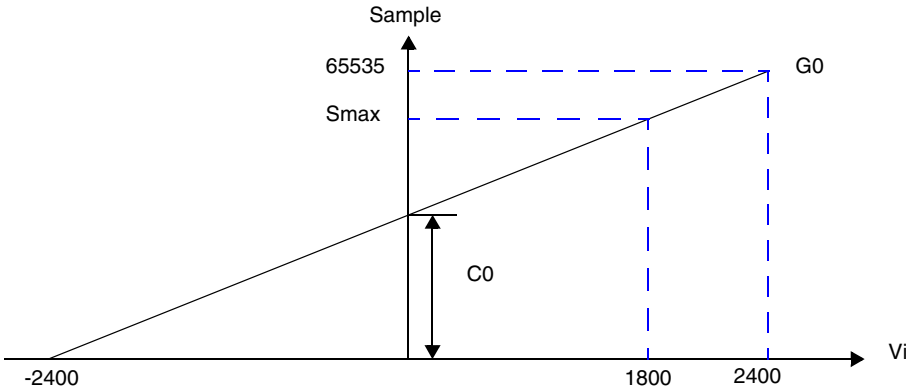


Figure 35. Offset Calculations

In general, the mapping function is:

$$S = G * V + C$$

Where V is input, S is output, G is the slope, and C is the y-intercept.

Nominal Gain $G_0 = 65535 / 4800 = 13.65mV^{-1}$
Nominal Offset $C_0 = 65535 / 2 = 32767$

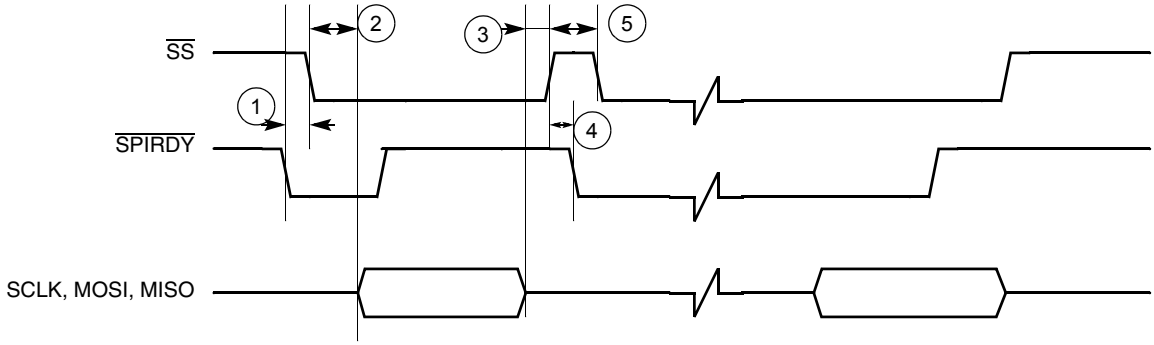


Figure 39. Master SPI Timing Diagram Using SPI_RDY Edge Trigger

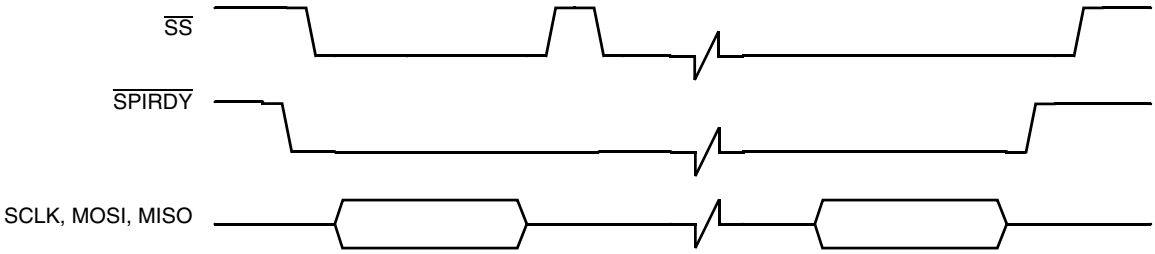


Figure 40. Master SPI Timing Diagram Using SPI_RDY Level Trigger

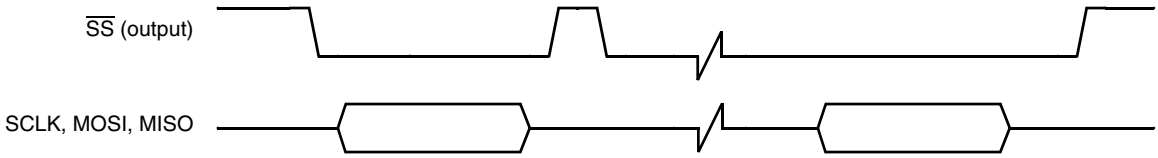


Figure 41. Master SPI Timing Diagram Ignore SPI_RDY Level Trigger

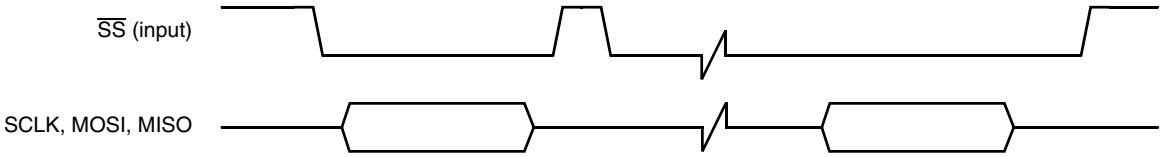


Figure 42. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT

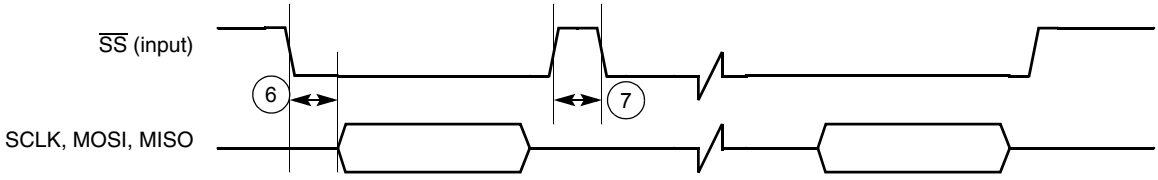


Figure 43. Slave SPI Timing Diagram FIFO Advanced by SS Rising Edge

Table 24. Timing Parameter Table for Figure 39 through Figure 43

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low	2T[1]	–	ns
2	$\overline{\text{SS}}$ output low to first SCLK edge	3 • Tsclk[2]	–	ns
3	Last SCLK edge to $\overline{\text{SS}}$ output high	2 • Tsclk	–	ns
4	$\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low	0	–	ns
5	$\overline{\text{SS}}$ output pulse width	Tsclk + WAIT [3]	–	ns
6	$\overline{\text{SS}}$ input low to first SCLK edge	T	–	ns
7	$\overline{\text{SS}}$ input pulse width	T	–	ns

1 T = CSPI system clock period (PERCLK2).

2 Tsclk = Period of SCLK.

3 WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

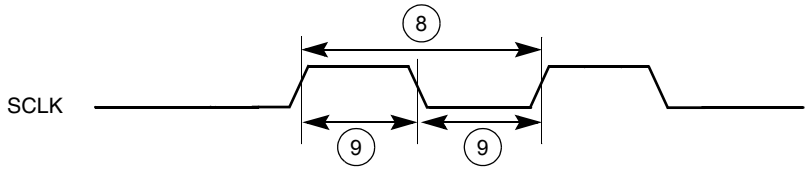


Figure 44. SPI SCLK Timing Diagram

Table 25. Timing Parameter Table for SPI SCLK

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
8	SCLK frequency	0	10	MHz
9	SCLK pulse width	100	–	ns

4.9 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *MC9328MX1 Reference Manual*.

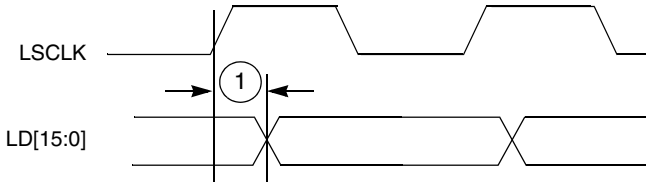


Figure 45. SCLK to LD Timing Diagram

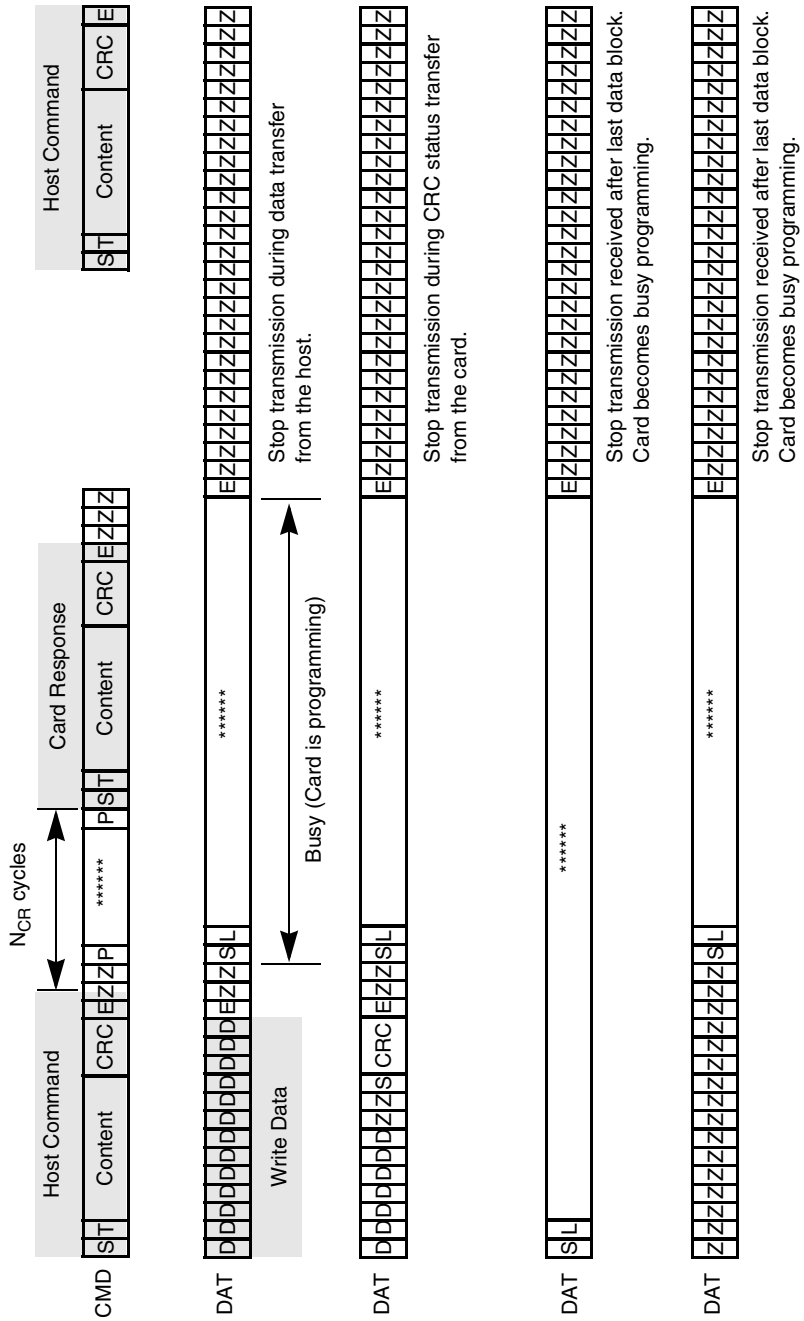


Figure 52. Stop Transmission During Different Scenarios

Table 30. Timing Values for Figure 48 through Figure 52

Parameter	Symbol	Minimum	Maximum	Unit
MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL)				
Command response cycle	NCR	2	64	Clock cycles
Identification response cycle	NID	5	5	Clock cycles
Access time delay cycle	NAC	2	TAAC + NSAC	Clock cycles

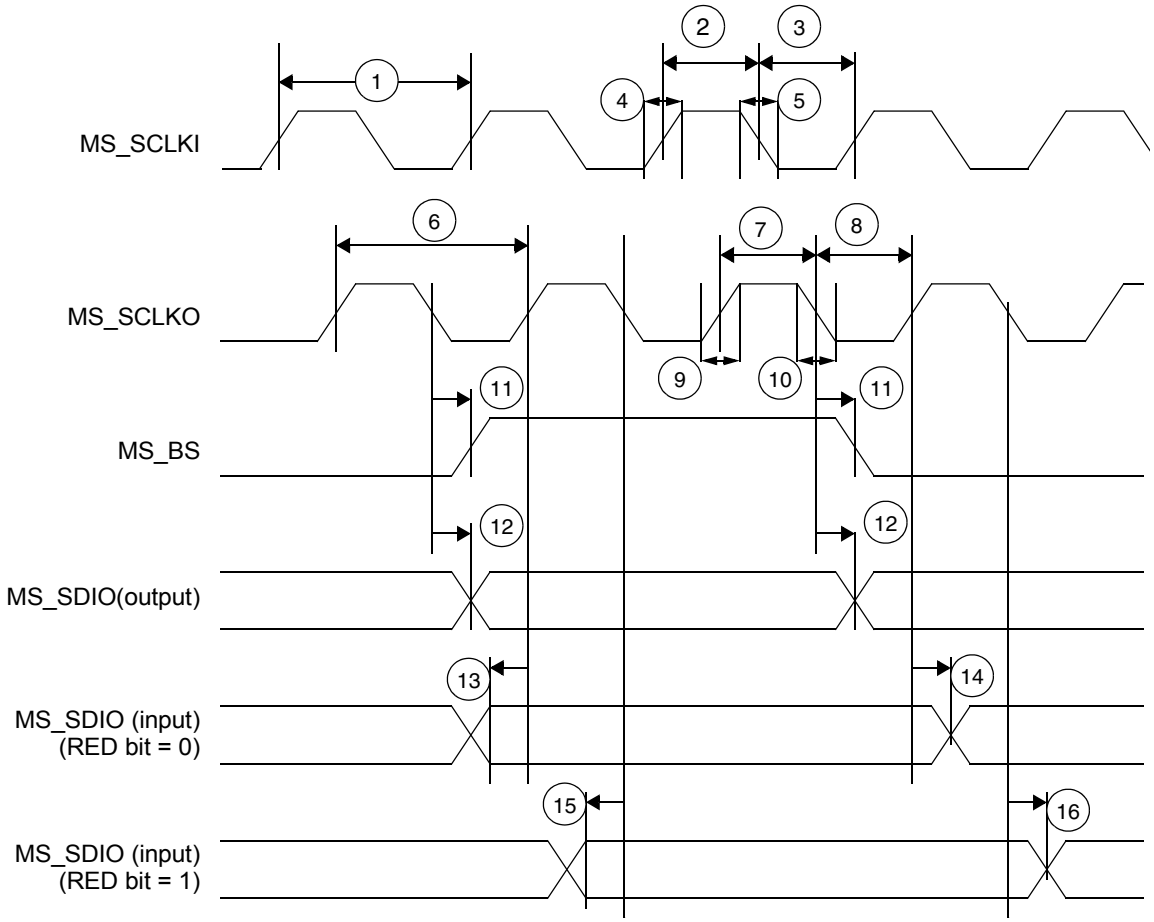


Figure 55. MSHC Signal Timing Diagram

Table 31. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	–	25	MHz
2	MS_SCLKI high pulse width	20	–	ns
3	MS_SCLKI low pulse width	20	–	ns
4	MS_SCLKI rise time	–	3	ns
5	MS_SCLKI fall time	–	3	ns
6	MS_SCLKO frequency[1]	–	25	MHz
7	MS_SCLKO high pulse width[1]	20	–	ns
8	MS_SCLKO low pulse width[1]	15	–	ns
9	MS_SCLKO rise time[1]	–	5	ns
10	MS_SCLKO fall time[1]	–	5	ns
11	MS_BS delay time[1]	–	3	ns

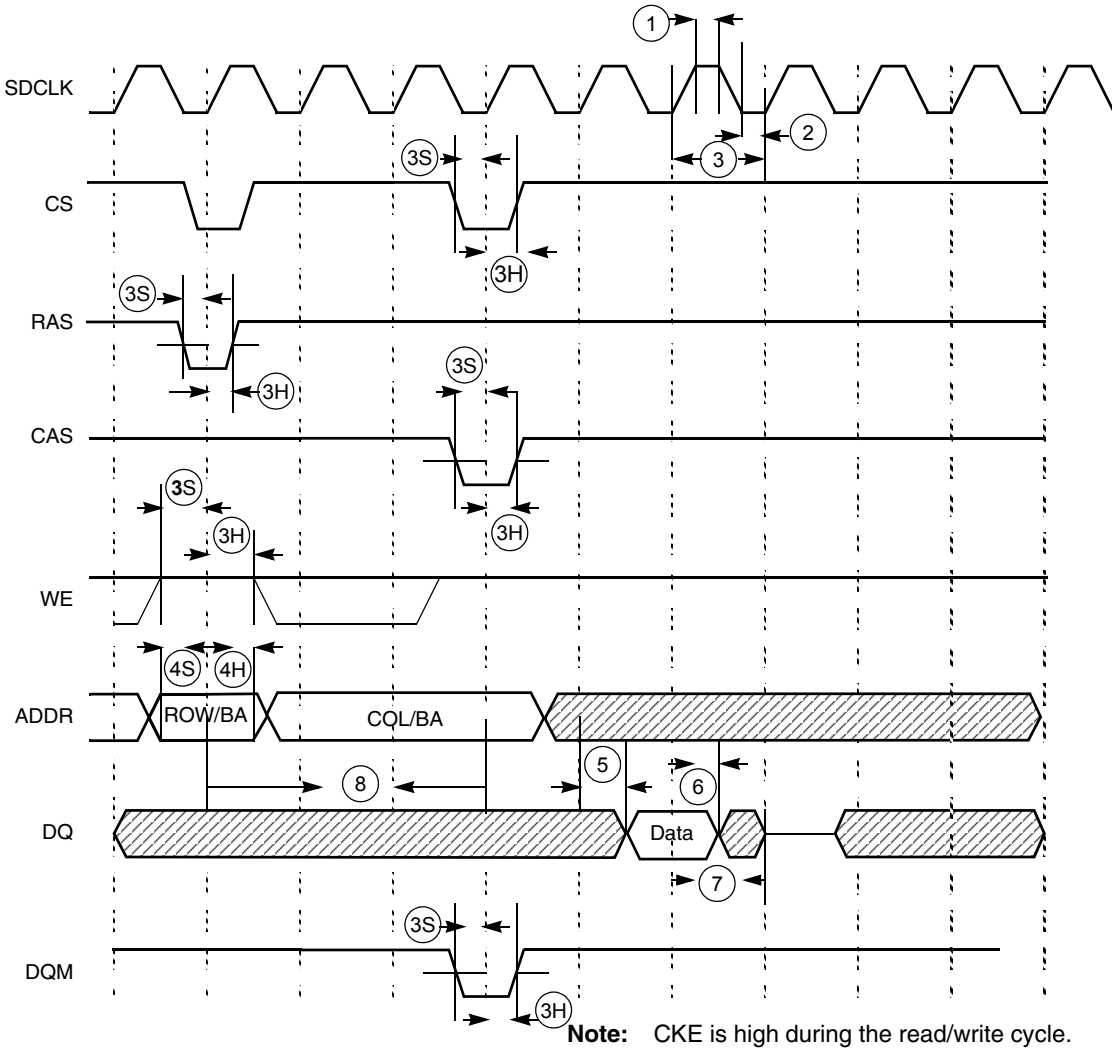
Table 32. PWM Output Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
3b	Clock rise time[1]	–	6.67	–	5/10	ns
4a	Output delay time[1]	5.7	–	5	–	ns
4b	Output setup time[1]	5.7	–	5	–	ns

[1] C_L of PWMO = 30 pF

4.13 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.



Note: CKE is high during the read/write cycle.

Figure 57. SDRAM Read Cycle Timing Diagram

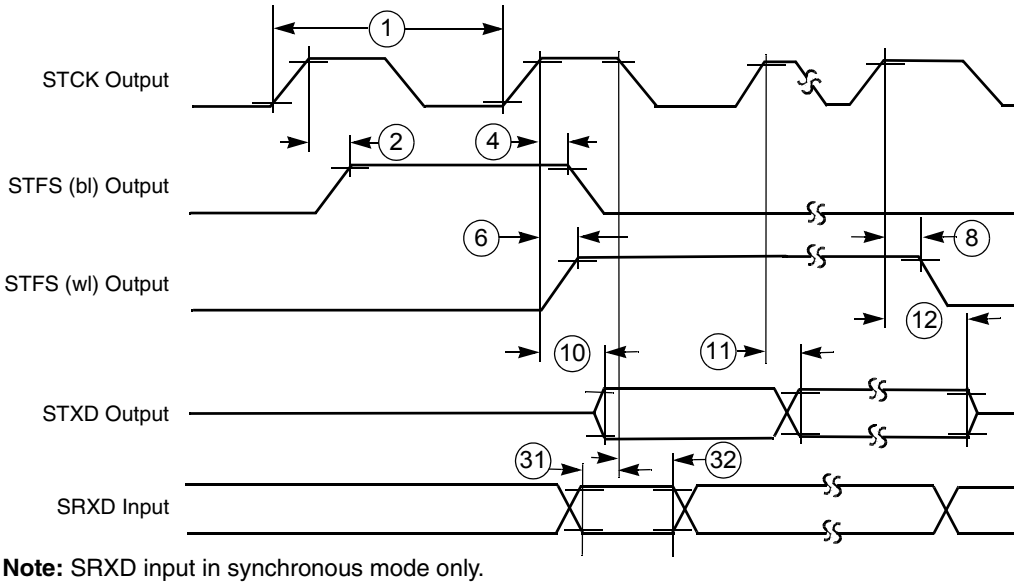
Table 38. I²C Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	Hold time (repeated) START condition	182	–	160	–	ns
2	Data hold time	0	171	0	150	ns
3	Data setup time	11.4	–	10	–	ns
4	HIGH period of the SCL clock	80	–	120	–	ns
5	LOW period of the SCL clock	480	–	320	–	ns
6	Setup time for STOP condition	182.4	–	160	–	ns

4.16 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 65 through Figure 67.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.



Note: SRXD input in synchronous mode only.

Figure 64. SSI Transmitter Internal Clock Timing Diagram

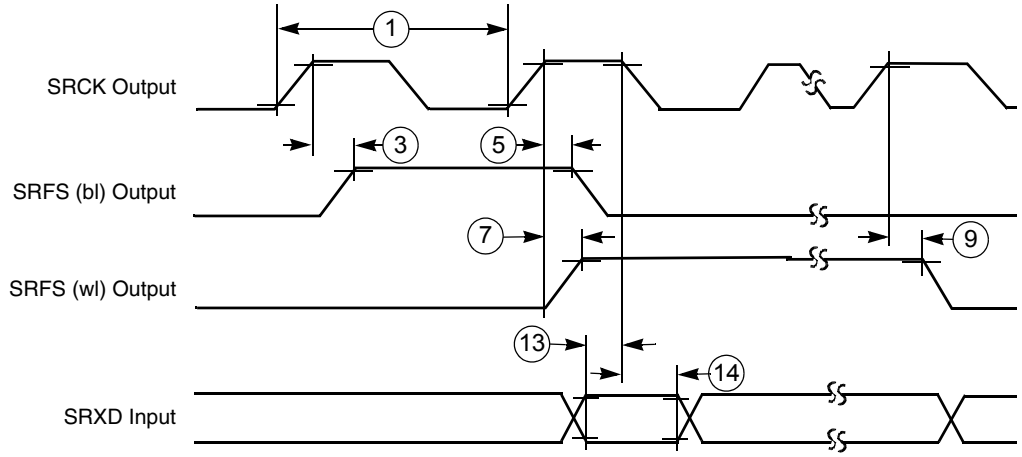
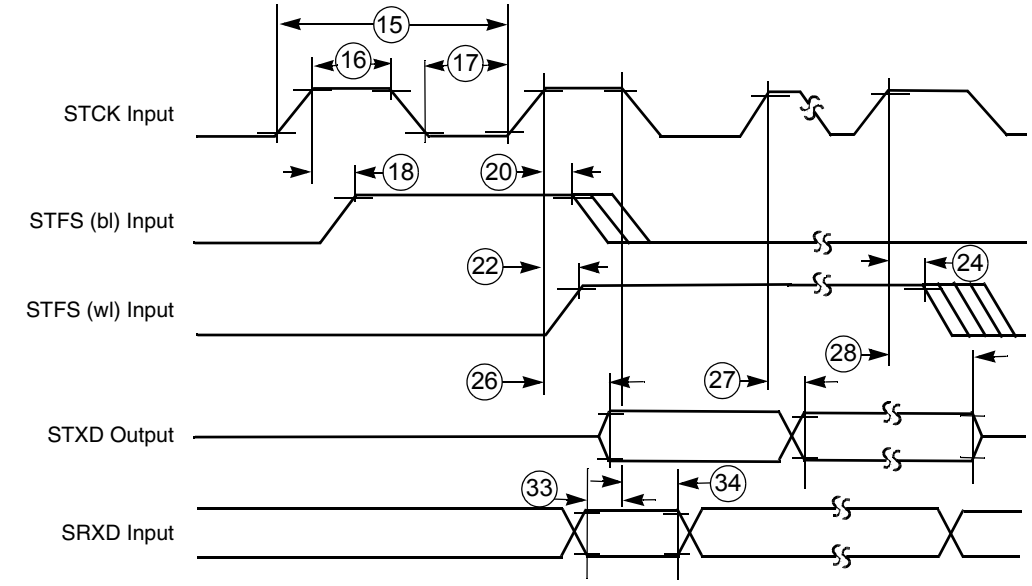


Figure 65. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 66. SSI Transmitter External Clock Timing Diagram

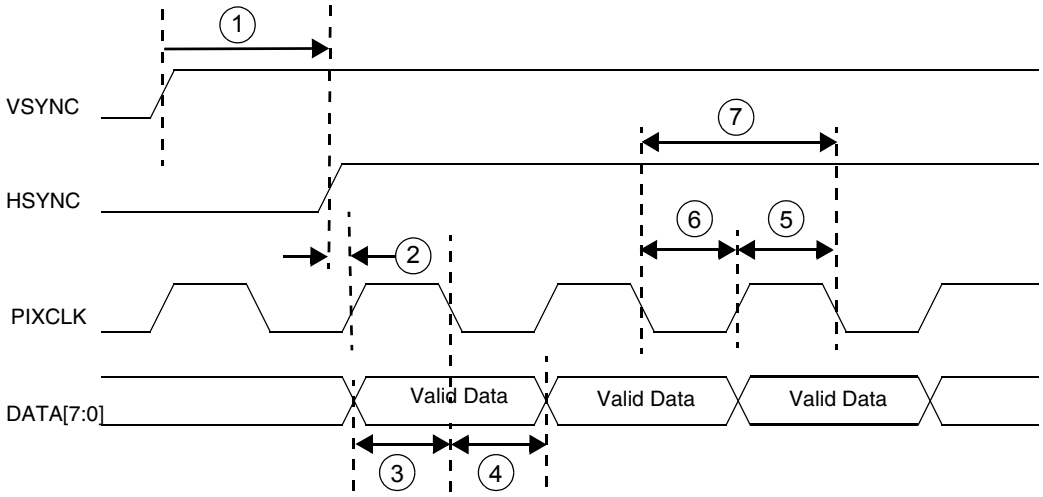


Figure 69. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge

Table 42. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

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