Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touch Panel
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-MAPBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx1vm20r2

- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode
- Analog Signal Processing (ASP) Module
- Bluetooth™ Accelerator (BTA)
- Multimedia Accelerator (MMA)
- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 256-pin MAPBGA Package

1.2 Target Applications

The i.MX1 processor is targeted for advanced information appliances, smart phones, Web browsers, based on the popular Palm OS platform, and messaging applications such as wireless cellular products, including the Accompli^{TM} 008 GSM/GPRS interactive communicator.

1.3 Ordering Information

Table 1 provides ordering information.

Table 1. Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
256-lead MAPBGA	200 MHz	0°C to 70°C	Pb-free	MC9328MX1VM20(R2)
		-30°C to 70°C	Pb-free	MC9328MX1DVM20(R2)
	150 MHz	0°C to 70°C	Pb-free	MC9328MX1VM15(R2)
		-30°C to 70°C	Pb-free	MC9328MX1DVM15(R2)
		-40°C to 85°C	Pb-free	MC9328MX1CVM15(R2)

1.4 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD2	R14	$\overline{TDO}$	O									Hiz[5]	
NVDD2	N15	TMS	I	69K								Pull-H	
NVDD2	L9	TCK	I	69K								Pull-H	
NVDD2	N16	TDI	I	69K								Pull-H	
NVDD2	P14	I2C_SCL	O				PA16	69K				Pull-H	PA16
NVDD2	P15	I2C_SDA	I/O				PA15	69K				Pull-H	PA15
NVDD2	N13	CSI_PIXCLK	I				PA14	69K				Pull-H	PA14
NVDD2	M13	CSI_HSYNC	I				PA13	69K				Pull-H	PA13
NVDD2	M14	CSI_VSYNC	I				PA12	69K				Pull-H	PA12
NVDD2	N14	CSI_D7	I				PA11	69K				Pull-H	PA11
NVDD2	M15	CSI_D6	I				PA10	69K				Pull-H	PA10
NVDD2	M16	CSI_D5	I				PA9	69K				Pull-H	PA9
NVDD2	J10	VSS	Static										
NVDD2	M12	CSI_D4	I				PA8	69K				Pull-H	PA8
NVDD2	L16	CSI_D3	I				PA7	69K				Pull-H	PA7
NVDD2	L15	CSI_D2	I				PA6	69K				Pull-H	PA6
NVDD2	L14	CSI_D1	I				PA5	69K				Pull-H	PA5
NVDD2	L13	CSI_D0	I				PA4	69K				Pull-H	PA4
NVDD2	L12	CSI_MCLK	O				PA3	69K				Pull-H	PA3
NVDD2	L11	PWMO	O				PA2	69K				Pull-H	PA2
NVDD2	L10	TIN	I				PA1	69K			SPI2_RxD	Pull-H	PA1
NVDD2	K15	TMR2OUT	O				PD31	69K	SPI2_TxD			Pull-H	PD31
NVDD2	K16	LD15	O				PD30	69K				Pull-H	PD30
NVDD2	K14	LD14	O				PD29	69K				Pull-H	PD29
NVDD2	K13	LD13	O				PD28	69K				Pull-H	PD28

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD2	K12	LD12	O				PD27	69K				Pull-H	PD27
QVDD3	J15	QVDD3	Static										
	J16	VSS	Static										
NVDD2	K9	NVDD2	Static										
NVDD2	J14	LD11	O				PD26	69K				Pull-H	PD26
NVDD2	K11	LD10	O				PD25	69K				Pull-H	PD25
NVDD2	H15	LD9	O				PD24	69K				Pull-H	PD24
NVDD2	J13	LD8	O				PD23	69K				Pull-H	PD23
NVDD2	J12	LD7	O				PD22	69K				Pull-H	PD22
NVDD2	J11	LD6	O				PD21	69K				Pull-H	PD21
NVDD2	H14	LD5	O				PD20	69K				Pull-H	PD20
NVDD2	H13	LD4	O				PD19	69K				Pull-H	PD19
NVDD2	H16	LD3	O				PD18	69K				Pull-H	PD18
NVDD2	H12	LD2	O				PD17	69K				Pull-H	PD17
NVDD2	G16	LD1	O				PD16	69K				Pull-H	PD16
NVDD2	H11	LD0	O				PD15	69K				Pull-H	PD15
NVDD2	G15	FLM/VSYNC	O				PD14	69K				Pull-H	PD14
NVDD2	G14	LP/HSYNC	O				PD13	69K				Pull-H	PD13
NVDD2	G13	ACD/OE	O				PD12	69K				Pull-H	PD12
NVDD2	G12	CONTRAST	O				PD11	69K		SPI2_SS2		Pull-H	PD11
NVDD2	F16	SPL_SPR	O		$\overline{\text{UART2\_DSR}}$	O	PD10	69K	SPI2_TxD			Pull-H	PD10
NVDD2	H10	PS	O		$\overline{\text{UART2\_RI}}$	O	PD9	69K			SPI2_RxD	Pull-H	PD9
NVDD2	G11	CLS	O		$\overline{\text{UART2\_DCD}}$	O	PD8	69K	SPI2_SS			Pull-H	PD8
NVDD2	F12	REV	O		$\overline{\text{UART2\_DTR}}$	I	PD7	69K	SPI2_CLK			Pull-H	PD7
NVDD2	F15	LSCLK	O				PD6	69K				Pull-H	PD6

Table 8. 32k/16M Oscillator Signal Timing (Continued)

Parameter	Minimum	RMS	Maximum	Unit
EXTAL16M input jitter (peak to peak) [1]	–	TBD	TBD	–
EXTAL16M startup time [1]	TBD	–	–	–

[1] The 16 MHz oscillator is not recommended for use in new designs.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MX1.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

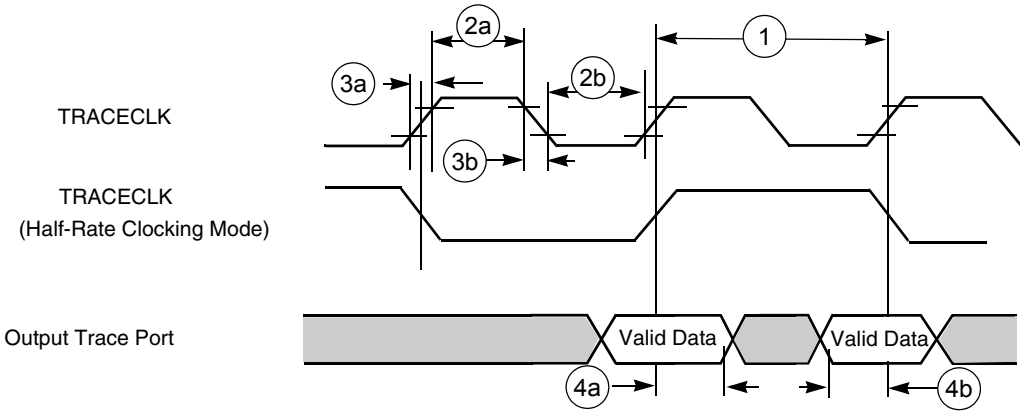


Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns
4a	Output hold time	2.28	–	2	–	ns
4b	Output setup time	3.42	–	3	–	ns

4.2 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 10. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
DPLL input clock freq range	Vcc = 1.8V	5	–	100	MHz
Pre-divider output clock freq range	Vcc = 1.8V	5	–	30	MHz
DPLL output clock freq range	Vcc = 1.8V	80	–	220	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Pre-multiplier lock-in time	–	–	–	312.5	µsec
Freq lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	250	280 (56 µs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	250 (50 µs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	300	350 (70 µs)	400	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	270	320 (64 µs)	370	T_{ref}
Freq jitter (p-p)	–	–	0.005 (0.01%)	0.01	$2 \bullet T_{dck}$

4.4.2.2 WAIT Read Cycle DMA Enabled

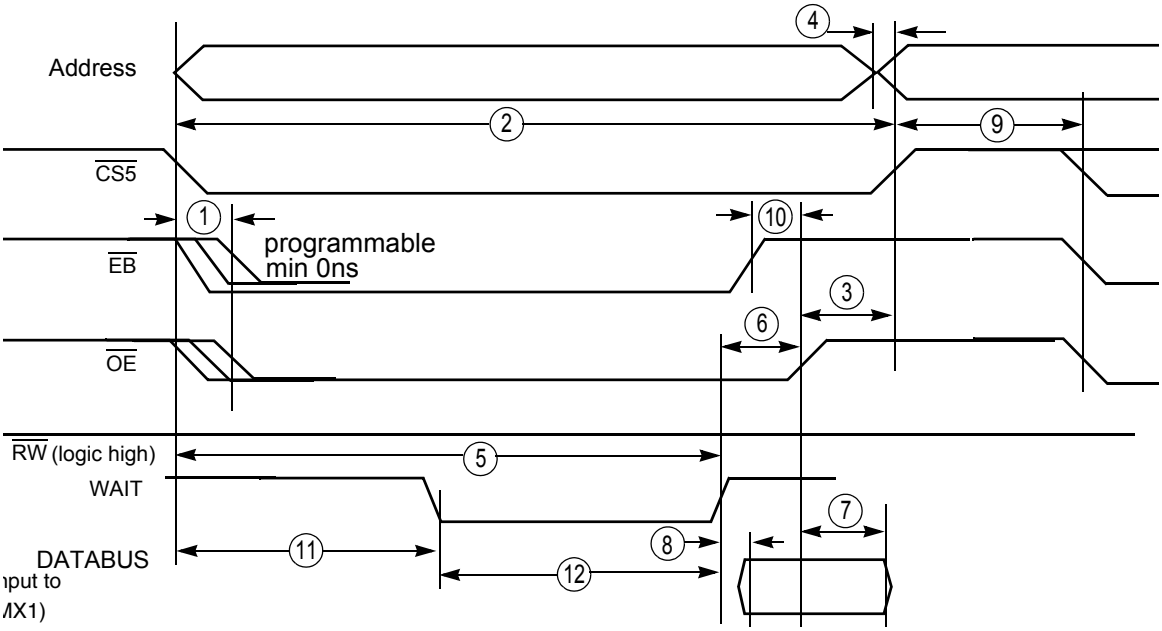


Figure 7. DTACK WAIT Read Cycle DMA Enabled

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated before $\overline{CS5}$ is negated	1.5T+0.24	1.5T+0.85	ns
4	Address inactived before $\overline{CS}$ negated	–	0.93	ns
5	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
6	Wait asserted to $\overline{OE}$ negated	2T+2.2	3T+7.17	ns
7	Data hold timing after $\overline{OE}$ negated	T-1.86	–	ns
8	Data ready after wait is asserted	–	T	ns
9	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
10	OE negate after EB negate	0.5	1.5	ns
11	Wait becomes low after CS5 asserted	0	1019T	ns

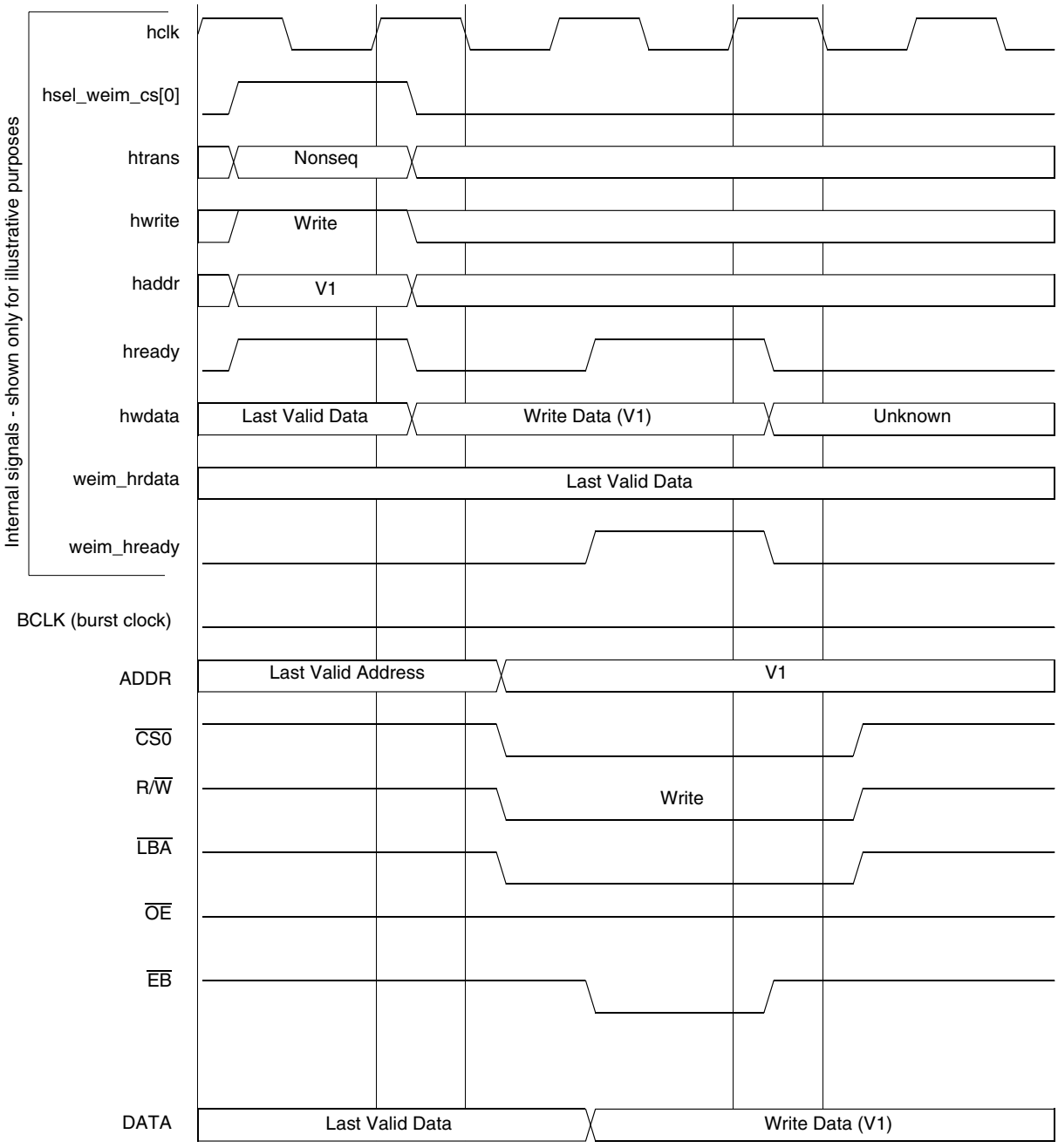
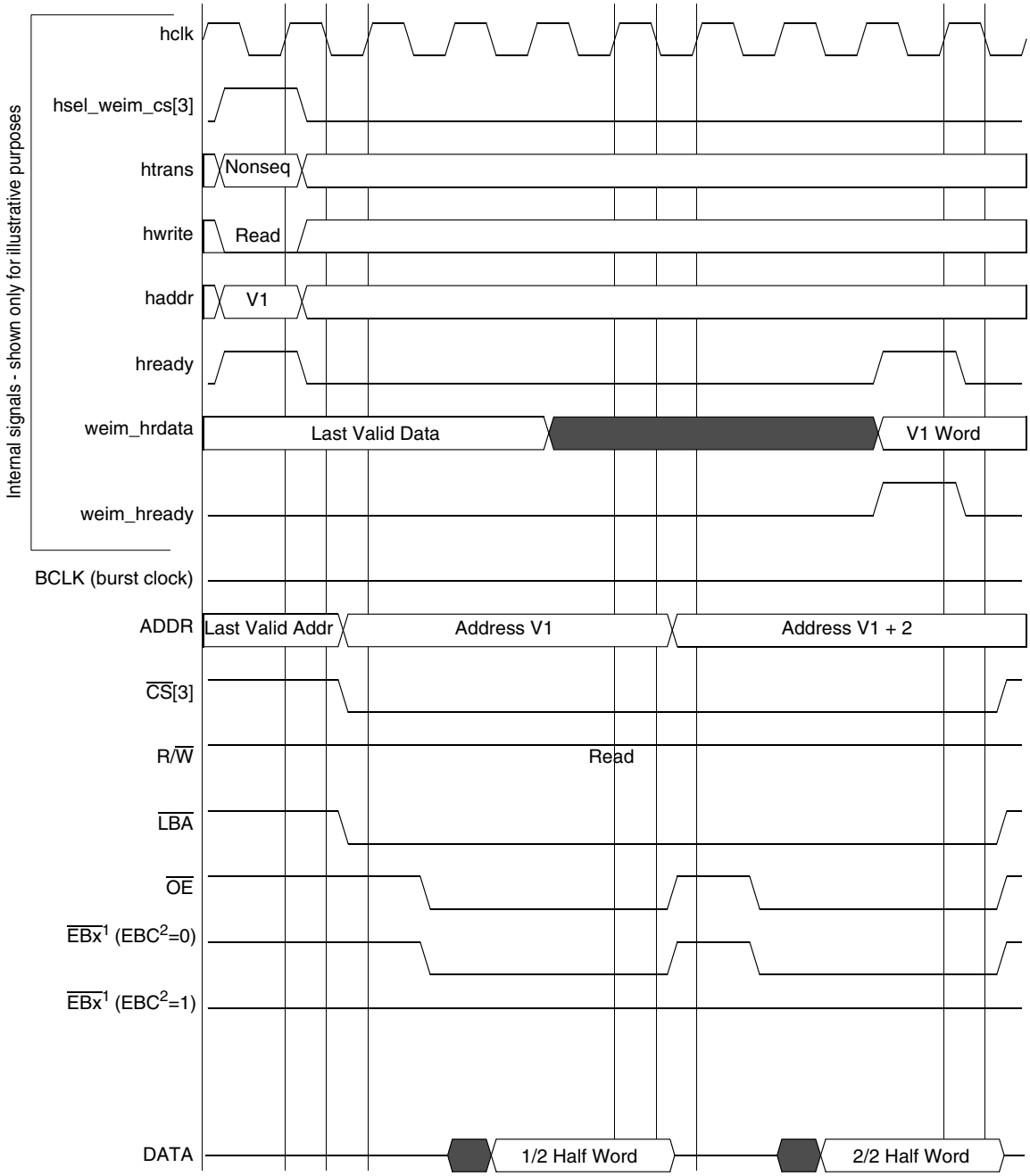
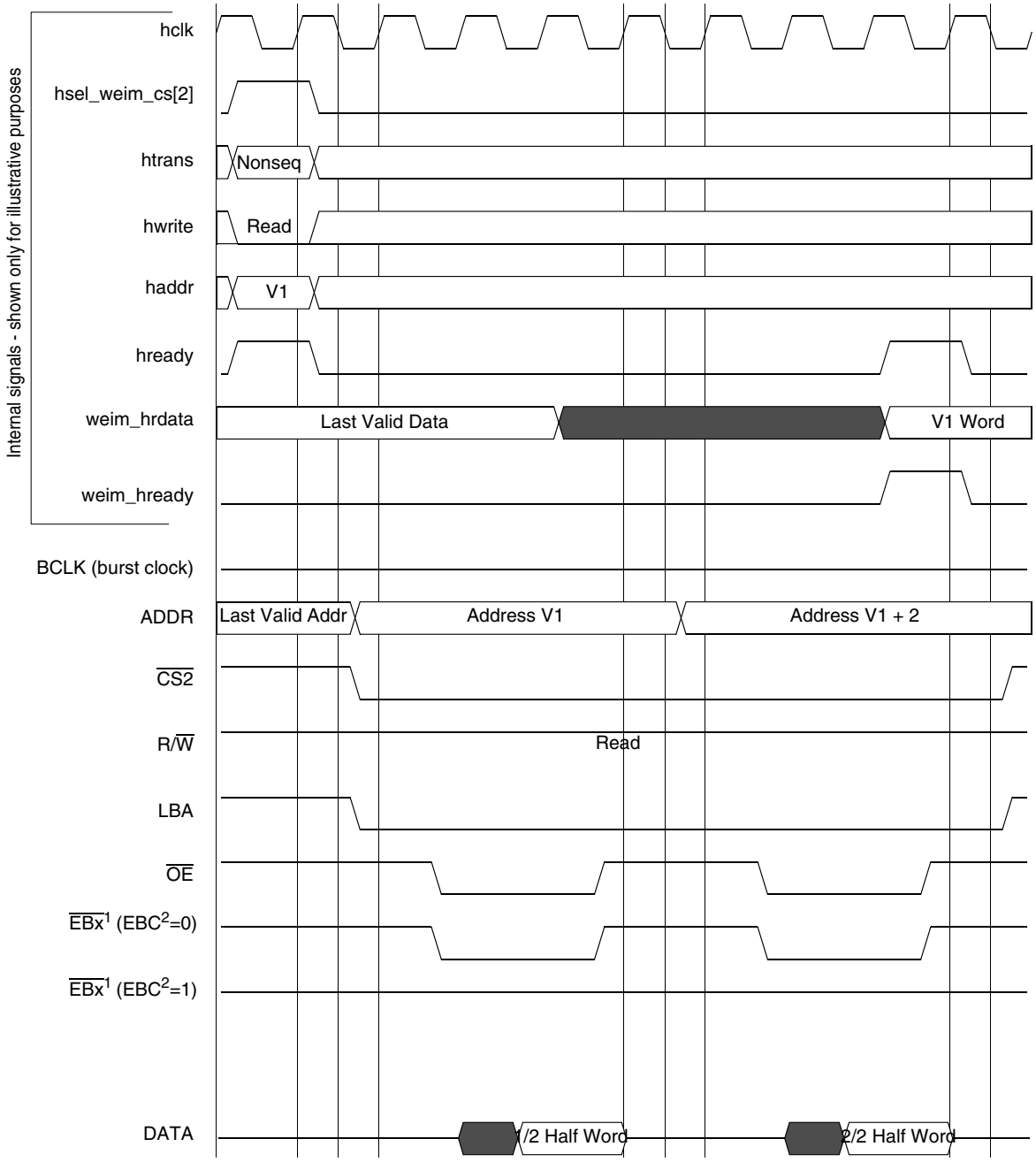


Figure 11. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

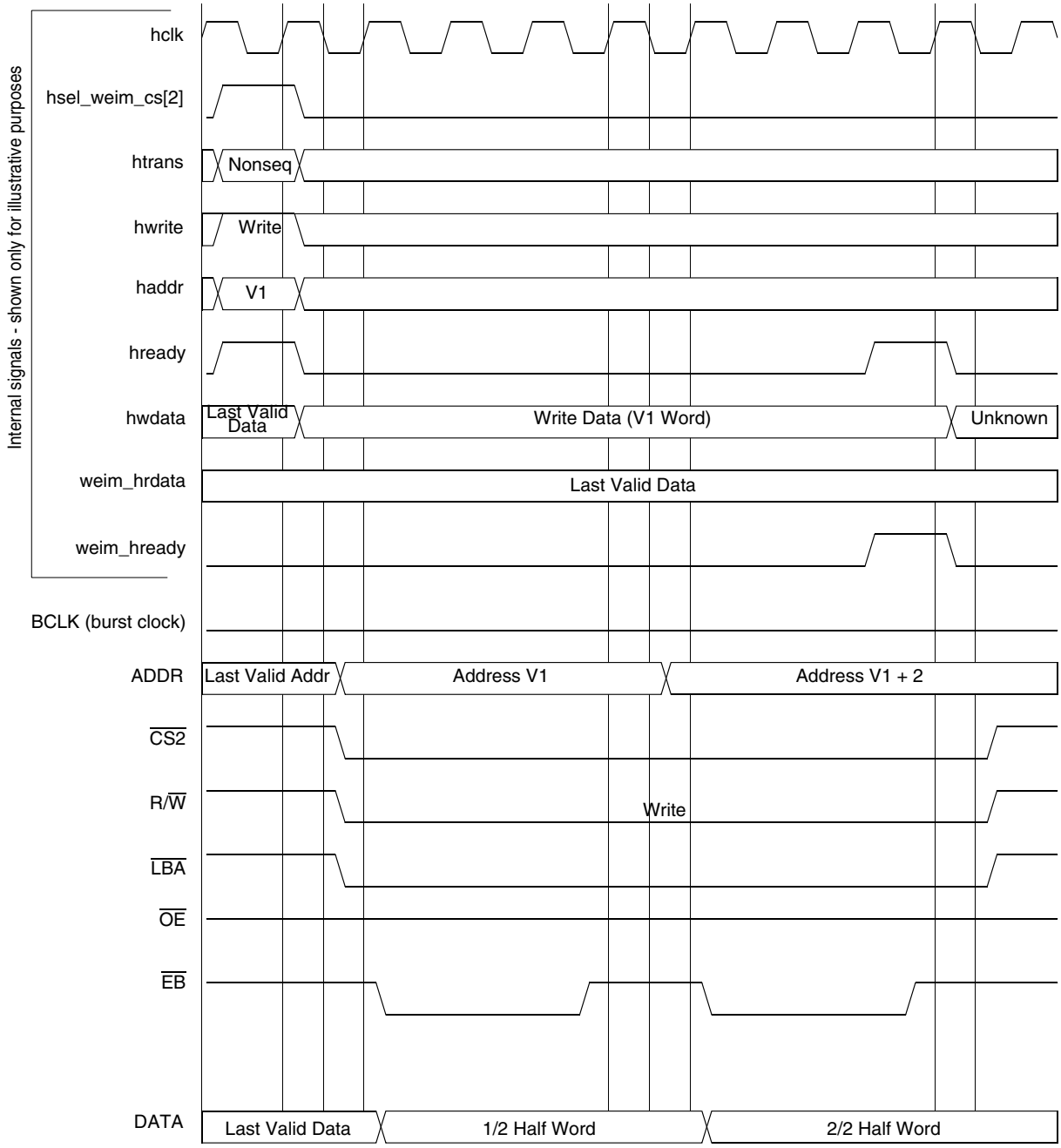


Figure 20. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

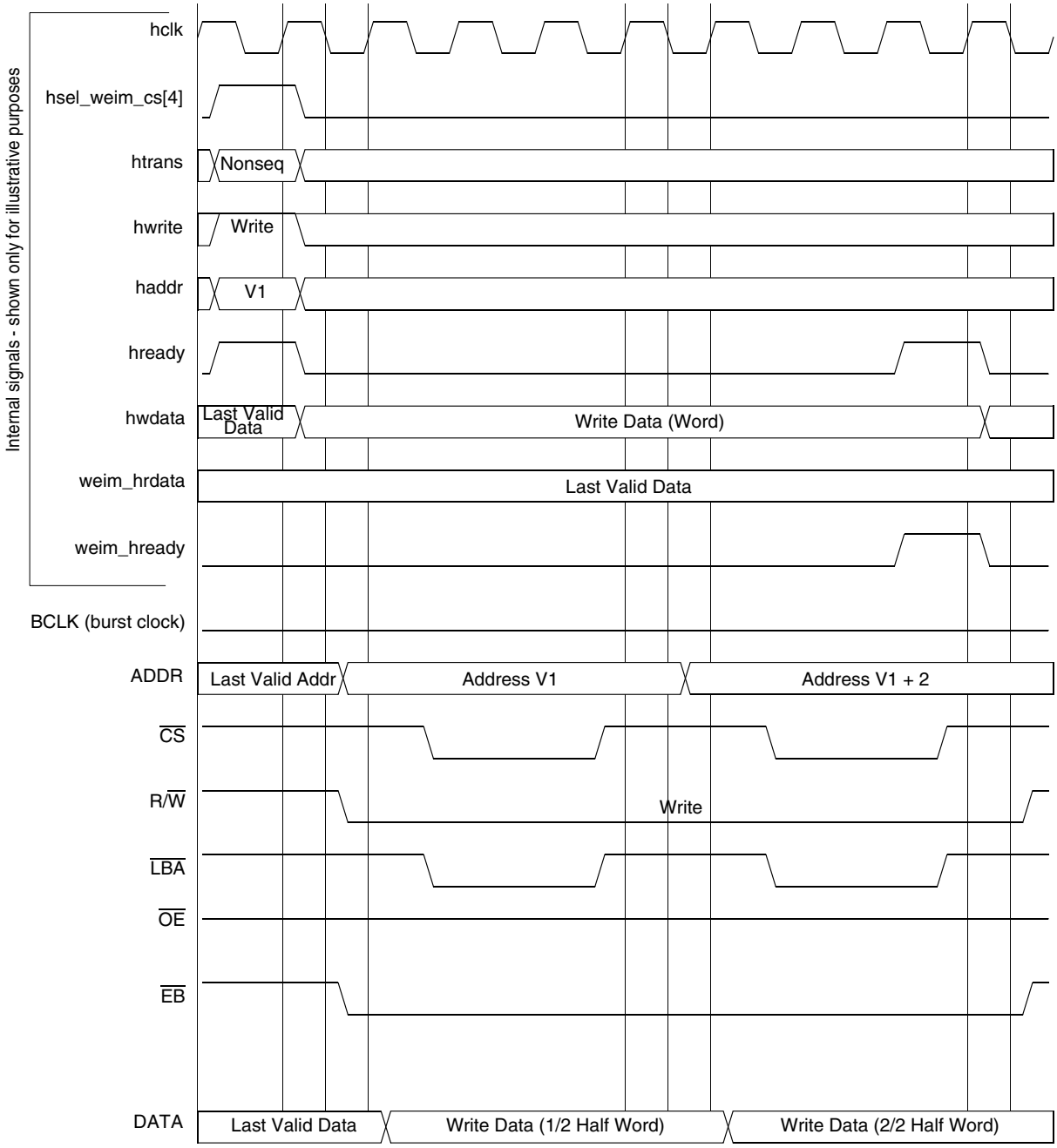
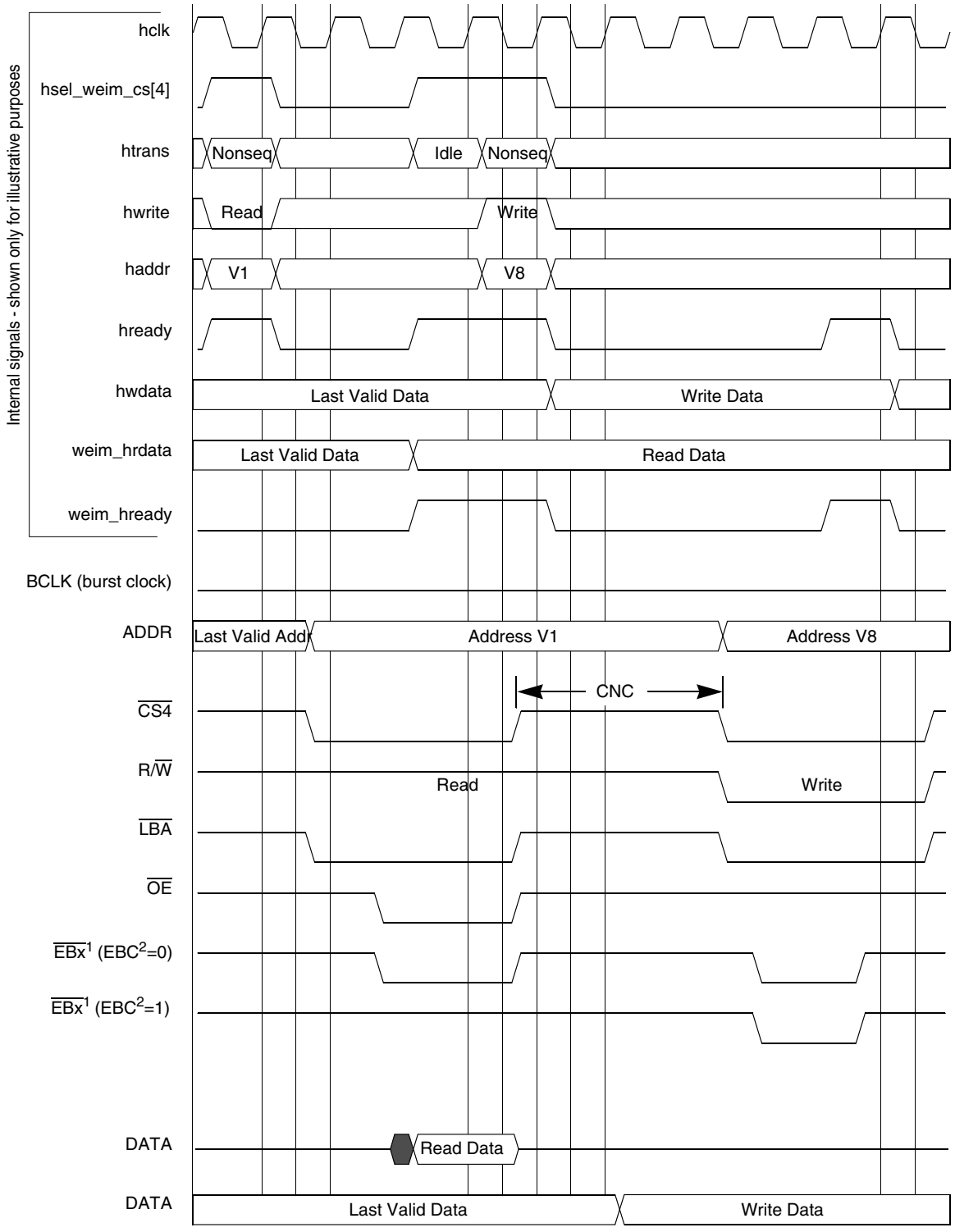
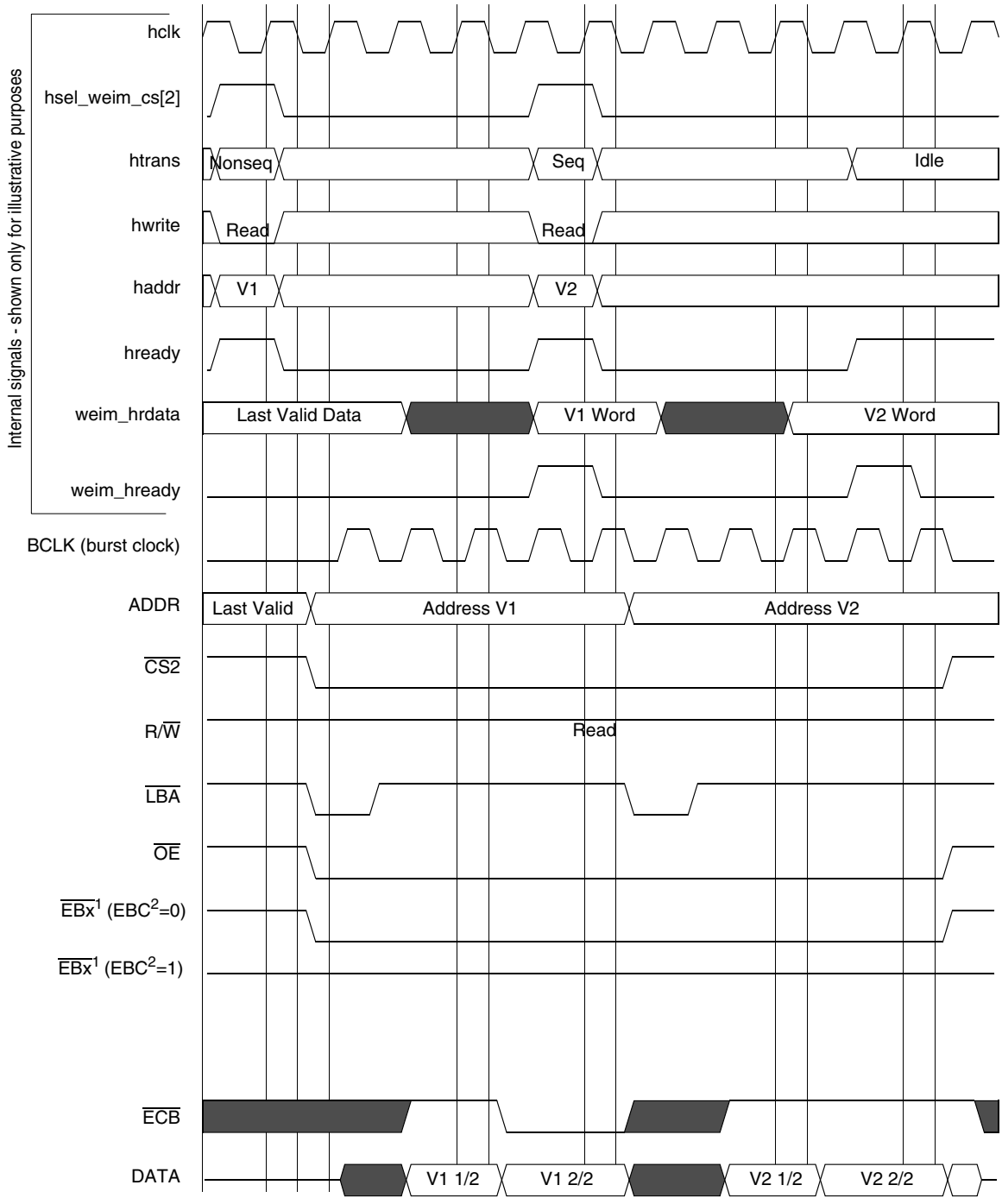


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



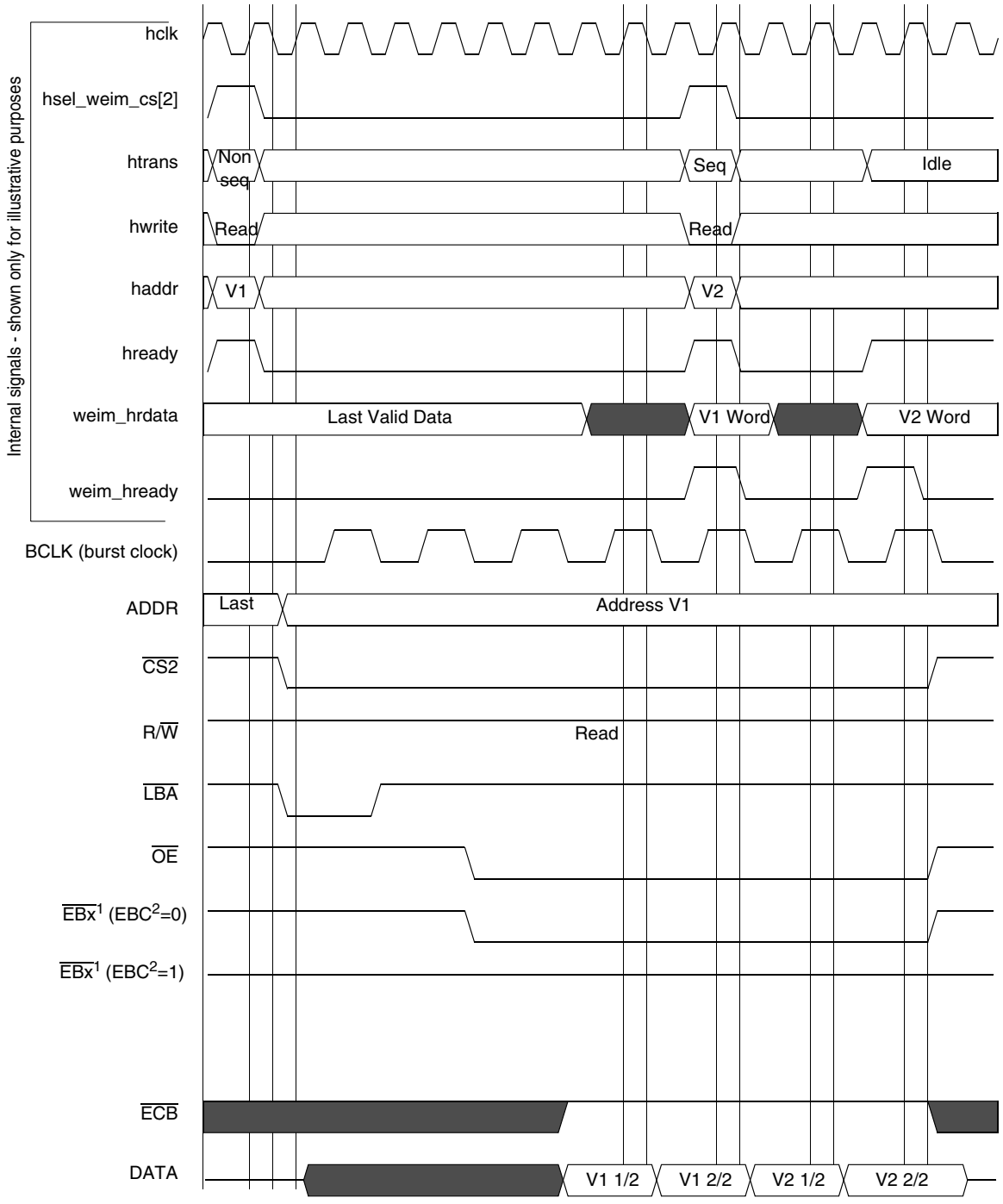
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 27. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

4.6.4 Gain Error Calculations

Gain error calculations are made using the information in this section.

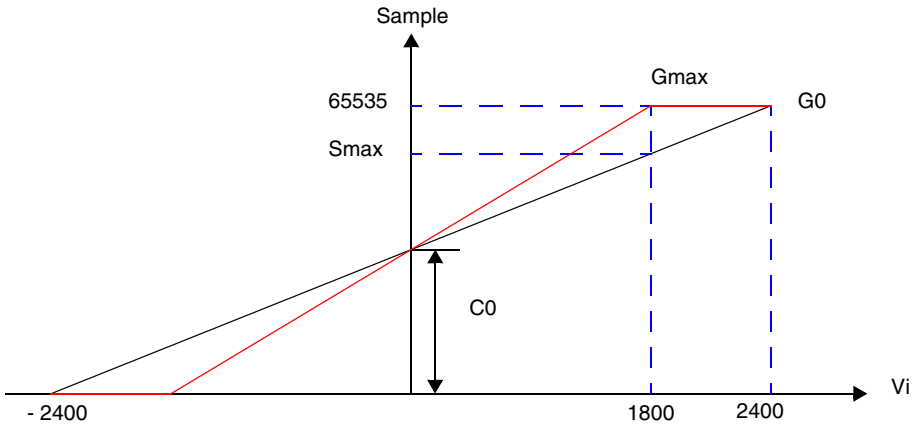


Figure 36. Gain Error Calculations

Assuming the offset remains unchanged, the mapping is rotated around y-intercept to determine the maximum gain allowed. This occurs when the sample at 1800mV has just reached the ceiling of the 16-bit range, 65535.

Maximum Offset $G_{max,}$

G_{max} $= (65535 - C_{0)} / 1800$
$= (65535 - 32767) / 1800$
$= 18.20$

Gain Error $G_{r,}$

G_r $= (G_{max} - G_0) / G_0 * 100\%$
$= (18.20 - 13.65) / 13.65 * 100\%$
$= 33\%$

4.7 Bluetooth Accelerator

CAUTION

On-chip accelerator hardware is not supported by software. An external Bluetooth chip interfaced to a UART is recommended.

The Bluetooth Accelerator (BTA) radio interface supports the Wireless RF Transceiver, MC13180 using an SPI interface. This section provides the data bus timing diagrams and SPI interface timing diagrams shown in Figure 37 and Figure 38, and the associated parameters shown in Table 22 and Table 23.

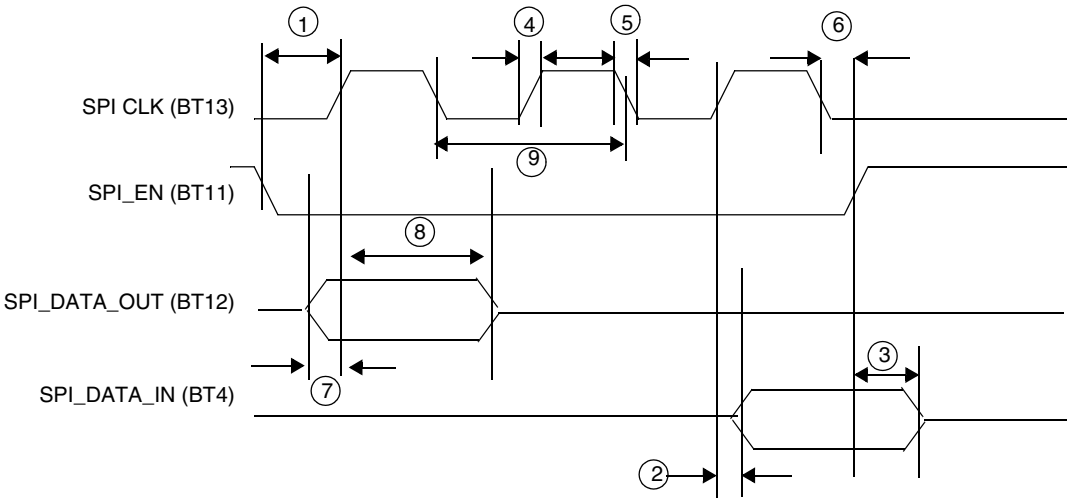


Figure 38. SPI Interface Timing Diagram Using MC13180

Table 23. SPI Interface Timing Parameter Table Using MC13180

Ref No.	Parameter	Minimum	Maximum	Unit
1	SPI_EN setup time relative to rising edge of SPI_CLK	15	–	ns
2	Transmit data delay time relative to rising edge of SPI_CLK	0	15	ns
3	Transmit data hold time relative to rising edge of SPI_EN	0	15	ns
4	SPI_CLK rise time	0	25	ns
5	SPI_CLK fall time	0	25	ns
6	SPI_EN hold time relative to falling edge of SPI_CLK	15	–	ns
7	Receive data setup time relative to falling edge of SPI_CLK[1]	15	–	ns
8	Receive data hold time relative to falling edge of SPI_CLK[1]	15	–	ns
9	SPI_CLK frequency, 50% duty cycle required[1]	–	20	MHz

[1] The SPI_CLK clock frequency and duty cycle, setup and hold times of receive data can be set by programming SPI_Control (0x00216138) register together with system clock.

4.8 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI 1 module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI\_RDY}$ signal (input). The SPI1 Sample Period Control Register (PERIODREG1) and the SPI2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either SPI 1 or SPI 2. When the SPI 1 module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, $\overline{SS}$ becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 39 through Figure 43 show the timing relationship of the master SPI using different triggering mechanisms.

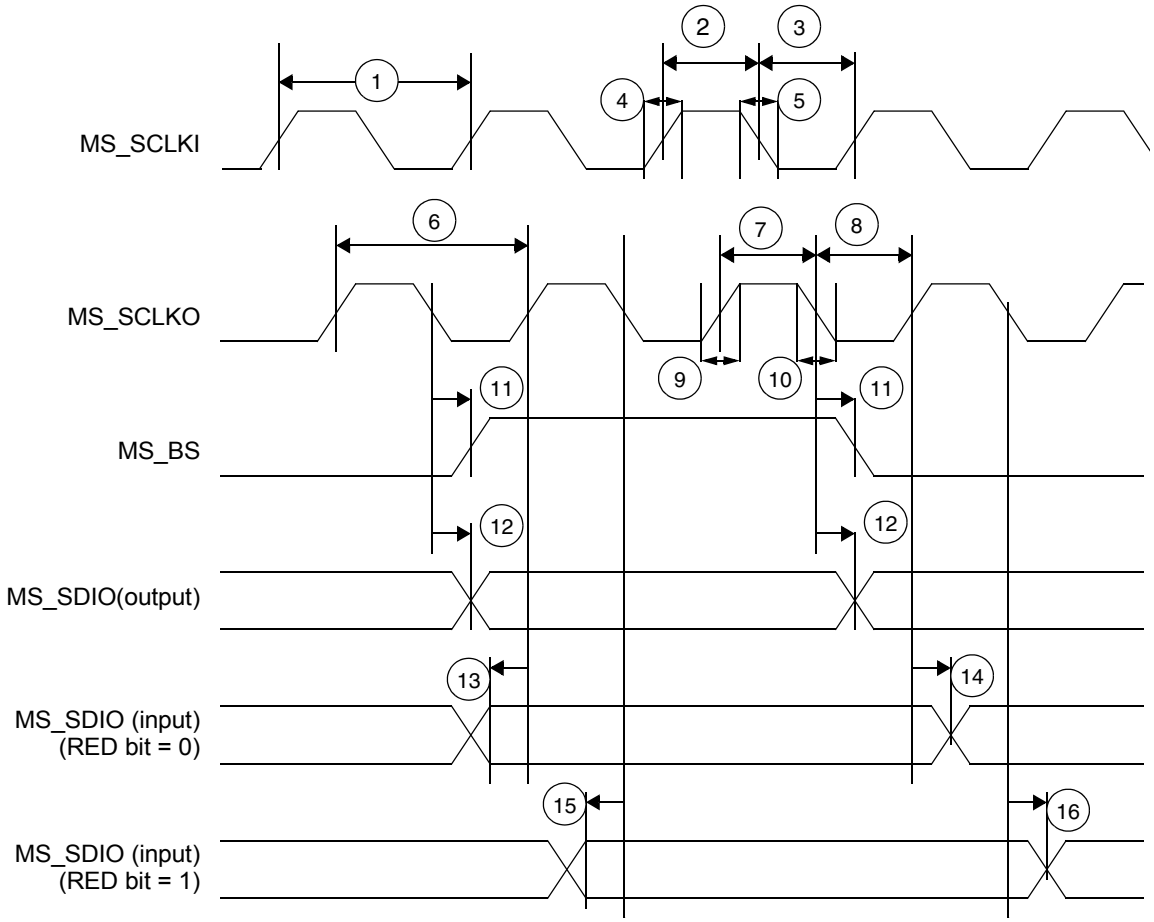


Figure 55. MSHC Signal Timing Diagram

Table 31. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	–	25	MHz
2	MS_SCLKI high pulse width	20	–	ns
3	MS_SCLKI low pulse width	20	–	ns
4	MS_SCLKI rise time	–	3	ns
5	MS_SCLKI fall time	–	3	ns
6	MS_SCLKO frequency[1]	–	25	MHz
7	MS_SCLKO high pulse width[1]	20	–	ns
8	MS_SCLKO low pulse width[1]	15	–	ns
9	MS_SCLKO rise time[1]	–	5	ns
10	MS_SCLKO fall time[1]	–	5	ns
11	MS_BS delay time[1]	–	3	ns

Table 33. SDRAM Read Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	3.42	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	2.28	–	2	–	ns
4S	Address setup time	3.42	–	3	–	ns
4H	Address hold time	2.28	–	2	–	ns
5	SDRAM access time (CL = 3)	–	6.84	–	6	ns
5	SDRAM access time (CL = 2)	–	6.84	–	6	ns
5	SDRAM access time (CL = 1)	–	22	–	22	ns
6	Data out hold time	2.85	–	2.5	–	ns
7	Data out high-impedance time (CL = 3)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 2)	–	6.84	–	6	ns
7	Data out high-impedance time (CL = 1)	–	22	–	22	ns
8	Active to read/write command period (RC = 1)	t_{RCD}[1]	–	t_{RCD1}	–	ns

[1] t_{RCD} = SDRAM clock cycle time. This settings can be found in the *MC9328MX1 reference manual*.

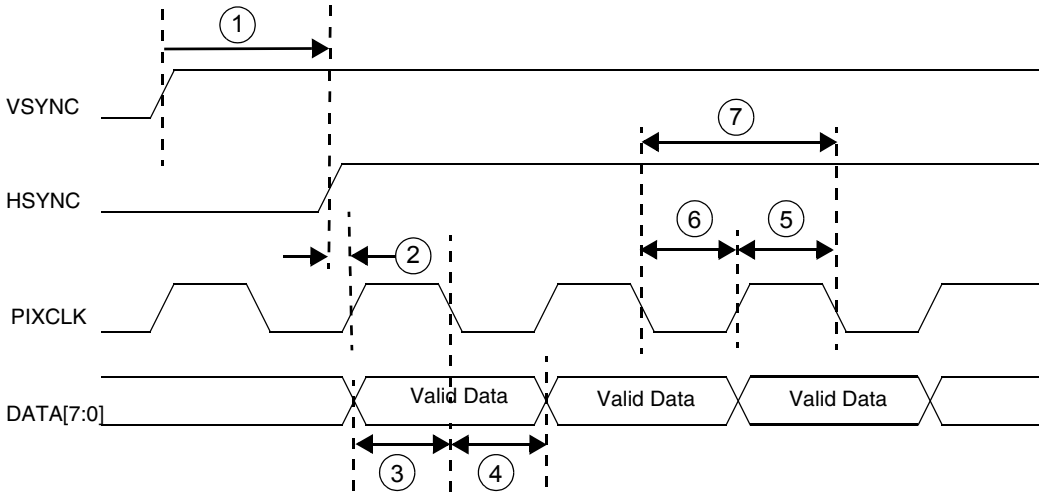


Figure 69. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge

Table 42. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

5 Pin-Out and Package Information

Table 44 illustrates the package pin assignments for the 256-pin MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 11.

Table 44. i.MX1 256 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NVSS	SD_DAT3	SD_CLK	NVSS	USBD_ AFE	NVDD4	NVSS	UART1_ RTS	UART1_ RXD	NVDD3	BT5	BT3	QVDD4	RVP	UIP	N.C.	A
B	A24	SD_DAT1	SD_CMD	SIM_TX	USBD_ ROE	USBD_VP	SSI_RXCLK	SSI_TXCLK	SPI1_ SCLK	BT11	BT7	BT1	QVSS	RVM	UIN	N.C.	B
C	A23	D31	SD_DAT0	SIM_PD	USBD_ RCV	UART2_ CTS	UART2_ RXD	SSI_ RXFS	UART1_ TXD	BTRFGND	BT8	BTRFVDD	N.C.	AVDD2[1]	VSS	R1B	C
D	A22	D30	D29	SIM_SVEN	USBD_ SUSPND	USBD_ VPO	USBD_ VMO	SSI_RXDAT	SPI1_ SPI_RDY	BT13	BT6	N.C.	N.C.	N.C.	R1A	R2B	D
E	A20	A21	D28	D26	SD_DAT2	USBD_VM	UART2_ RTS	SSI_TXDAT	SPI1_SS	BT12	BT4	N.C.	N.C.	PY2	PX2	R2A	E
F	A18	D27	D25	A19	A16	SIM_RST	UART2_ TXD	SSI_TXFS	SPI1_ MISO	BT10	BT2	REV	PY1	PX1	LSCLK	SPL_SPR	F
G	A15	A17	D24	D23	D21	SIM_RX	SIM_CLK	UART1_ CTS	SPI1_ MOSI	BT9	CLS	CONTRAST	ACD/OE	LP/ HSYNC	FLM/ VSYNC	LD1	G
H	A13	D22	A14	D20	NVDD1	NVDD1	NVSS	QVSS	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3	H
J	A12	A11	D18	D19	NVDD1	NVDD1	NVSS	NVDD1	NVSS	NVSS	LD6	LD7	LD8	LD11	QVDD3	QVSS	J
K	A10	D16	A9	D17	NVDD1	NVSS	NVSS	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TMR2OUT	LD15	K
L	A8	A7	D13	D15	D14	NVDD1	NVSS	CAS	TCK	TIN	PWMO	CSI_MCLK	CSI_D0	CSI_D1	CSI_D2	CSI_D3	L
M	A5	D12	D11	A6	SDCLK	NVSS	RW	MA10	RAS	RESET_IN	BIG_ ENDIAN	CSI_D4	CSI_ HSYNC	CSI_VSYNC	CSI_D6	CSI_D5	M
N	A4	EB1	D10	D7	A0	D4	PA17	D1	DQM1	RESET_SF[2]	RESET_ OUT	BOOT2	CSI_ PIXCLK	CSI_D7	TMS	TDI	N
P	A3	D9	EB0	CS3	D6	ECB	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	TRST	I2C_SCL	I2C_SDA	XTAL32K	P
R	EB2	EB3	A1	CS4	D8	D5	LBA	BCLK[3]	D0	DQM0	SDCKE0	POR	BOOT1	TDO	QVDD2	EXTAL32K	R
T	NVSS	A2	OE	CS5	CS2	CS1	CS0	MA11	DQM2	SDWE	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	QVSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

1 ASP signals are clamped by AVDD2 to prevent ESD (Electrostatic Discharge) damage. AVDD2 must be greater than QVDD to keep diodes reversed-biased.

2 This signal is not used and should be floated in an actual application.

3 burst clock