Renesas Electronics America Inc - UPD70F3750GK-GAK-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	67
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3750gk-gak-ax

(12/13)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value	HE3	HF3	HG3	HJ3
				1	8	16					
FFFFFA55H	UARTD5 option control register 1	UD5OPT1	R/W		√		00H	–	–	–	**Note**
FFFFFA56H	UARTD5 receive data register	UD5RX	R		√		FFH	–	–	–	**Note**
FFFFFA57H	UARTD5 transmit data register	UD5TX	R/W		√		FFH	–	–	–	**Note**
FFFFFC00H	External interrupt falling edge specification register 0	INTF0		√	√		00H	√	√	√	√
FFFFFC02H	External interrupt falling edge specification register 1	INTF1		√	√		00H	–	–	√	√
FFFFFC06H	External interrupt falling edge specification register 3	INTF3				√	0000H	–	–	√	√
FFFFFC06H	External interrupt falling edge specification register 3L	INTF3L		√	√		00H	√	√	√	√
FFFFFC07H	External interrupt falling edge specification register 3H	INTF3H		√	√		00H	–	–	√	√
FFFFFC08H	External interrupt falling edge specification register 4	INTF4		√	√		00H	–	–	–	**Note**
FFFFFC0CH	External interrupt falling edge specification register 6L	INTF6L		√	√		00H	–	–	–	√
FFFFFC10H	External interrupt falling edge specification register 8	INTF8		√	√		00H	–	–	–	√
FFFFFC13H	External interrupt falling edge specification register 9H	INTF9H		√	√		00H	√	√	√	√
FFFFFC20H	External interrupt rising edge specification register 0	INTR0		√	√		00H	√	√	√	√
FFFFFC22H	External interrupt rising edge specification register 1	INTR1		√	√		00H	–	–	√	√
FFFFFC26H	External interrupt rising edge specification register 3	INTR3				√	0000H	–	–	√	√
FFFFFC26H	External interrupt rising edge specification register 3L	INTR3L		√	√		00H	√	√	√	√
FFFFFC27H	External interrupt rising edge specification register 3H	INTR3H		√	√		00H	–	–	√	√
FFFFFC28H	External interrupt rising edge specification register 4	INTR4		√	√		00H	–	–	–	**Note**
FFFFFC2CH	External interrupt rising edge specification register 6L	INTR6L		√	√		00H	–	–	–	√
FFFFFC30H	External interrupt rising edge specification register 8	INTR8		√	√		00H	–	–	–	√
FFFFFC33H	External interrupt rising edge specification register 9H	INTR9H		√	√		00H	√	√	√	√
FFFFFC40H	Pull-up resistor option register 0	PU0		√	√		00H	√	√	√	√
FFFFFC42H	Pull-up resistor option register 1	PU1		√	√		00H	–		√	√
FFFFFC46H	Pull-up resistor option register 3	PU3				√	0000H	–	√	√	√
FFFFFC46H	Pull-up resistor option register 3L	PU3L		√	√		00H	√	√	√	√
FFFFFC47H	Pull-up resistor option register 3H	PU3H		√	√		00H	–	√	√	√
FFFFFC48H	Pull-up resistor option register 4	PU4		√	√		00H	√	√	√	√
FFFFFC4AH	Pull-up resistor option register 5	PU5		√	√		00H	√	√	√	√
FFFFFC4CH	Pull-up resistor option register 6	PU6				√	0000H	–	–	–	√
FFFFFC4CH	Pull-up resistor option register 6L	PU6L		√	√		00H	–	–	–	√
FFFFFC4DH	Pull-up resistor option register 6H	PU6H		√	√		00H	–	–	–	√
FFFFFC50H	Pull-up resistor option register 8	PU8		√	√		00H	–	–	–	√
FFFFFC52H	Pull-up resistor option register 9	PU9				√	0000H	√	√	√	√
FFFFFC52H	Pull-up resistor option register 9L	PU9L		√	√		00H	√	√	√	√
FFFFFC53H	Pull-up resistor option register 9H	PU9H		√	√		00H	√	√	√	√
FFFFFC73H	Port 9 function control register H	PF9H		√	√		00H	√	√	√	√
FFFFFD00H	CSIB0 control register 0	CB0CTL0		√	√		01H	√	√	√	√
FFFFFD01H	CSIB0 control register 1	CB0CTL1		√	√		00H	√	√	√	√
FFFFFD02H	CSIB0 control register 2	CB0CTL2			√		00H	√	√	√	√
FFFFFD03H	CSIB0 status register	CB0STR		√	√		00H	√	√	√	√
FFFFFD04H	CSIB0 receive data register	CB0RX	R			√	0000H	√	√	√	√
FFFFFD04H	CSIB0 receive data register L	CB0RXL			√		00H	√	√	√	√

Note Supported only in the μPD70F3757

(3) Port mode control register 9 (PMC9)

(a) V850ES/HE3, V850ES/HF3

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

PMC9 (PMC9H)

15	14	13	12	11	10	9	8
PMC915	PMC914	PMC913	0	0	0	PMC99	PMC98

(PMC9L)

7	6	5	4	3	2	1	0
PMC97	PMC96	0	0	0	0	PMC91	PMC90

PMC915	Specification of P915 pin operation mode
0	I/O port
1	INTP6 input/SCL00 I/O

PMC914	Specification of P914 pin operation mode
0	I/O port
1	INTP5 input/SDA00 I/O

PMC913	Specification of P913 pin operation mode
0	I/O port
1	INTP4 input/PCL output

PMC99	Specification of P99 pin operation mode
0	I/O port
1	$\overline{\text{SCKB1}}$ I/O/TIAB00 input/TOAB00 output

PMC98	Specification of P98 pin operation mode
0	I/O port
1	SOB1 output/TIAB03 input/TOAB03 output

PMC97	Specification of P97 pin operation mode
0	I/O port
1	SIB1 input/TIAA20 input/TOAA20 output

PMC96	Specification of P96 pin operation mode
0	I/O port
1	TIAA21 input/TOAA21 output

PMC91	Specification of P91 pin operation mode
0	I/O port
1	KR7 input/RXDD1 input

PMC90	Specification of P90 pin operation mode
0	I/O port
1	KR6 input/TXDD1 output

Remarks 1. √: Operable

×: Stopped

2. f_X: Main clock oscillation frequency

f_{PLLI}: PLL input clock frequency

f_{XT}: Subclock frequency

f_{RL}: Low-speed internal oscillation clock frequency

f_{RH}: High-speed internal oscillation clock frequency

f_{PLLO}: PLL output clock frequency

f_{SSCGO}: SSCG output clock frequency

f_{PCL}: PCL output clock frequency

f_{XX}: Main clock frequency

f_{CLK}: Internal system clock frequency

f_{CPU}: CPU clock frequency

6.4.3 Clock output function

The clock output function is used to output the internal system clock (f_{CLK}) from the CLKOUT pin.

The internal system clock (f_{CLK}) is selected by using the PCC.CK3 to PCC.CK0 bits.

The CLKOUT pin functions alternately as the PCM1 pin and functions as a clock output pin if so specified by the control register of port CM.

The status of the CLKOUT pin is the same as the internal system clock (f_{CLK}) in Table 6-2 and the pin can output the clock when it is in the operable status. It outputs a low level in the stopped status. However, the CLKOUT pin is in the port mode (PCM1 pin: input mode) after reset and until it is set in the output mode. Therefore, the status of the pin is Hi-Z.

Table 7-7 show the timer modes that can be used in the tuned operation mode and Table 7-8 shows the differences of timer output function between unit operation and tuned operation (√: Settable, ×: Not settable).

Table 7-7. Timer Modes Usable in Tuned Operation Mode

Master Timer	Slave Timer	Free-Running Timer Mode	PWM Mode	Triangular Wave PWM Mode
TAA0	TAA1	√	√	×
TAA2	TAA3	√	√	×
TAB0	TAA4	√	√	×
TAB1	TAB2	√	√	√

Table 7-8. Timer Output Functions

Tuned Channel	Timer	Pin	Free-Running Timer Mode		PWM Mode		Triangular Wave PWM Mode	
			Tuning OFF	Tuning ON	Tuning OFF	Tuning ON	Tuning OFF	Tuning ON
Ch0	TAA0 (master)	TOAA00	PPG	←	Toggle	←	N/A	←
		TOAA01	PPG	←	PWM	←	N/A	←
	TAA1 (slave)	TOAA10	PGP	←	Toggle	PWM	N/A	←
		TOAA11	PPG	←	PWM	←	N/A	←
Ch1	TAA2 (master)	TOAA20	PPG	←	Toggle	←	N/A	←
		TOAA21	PPG	←	PWM	←	N/A	←
	TAA3 (slave)	TOAA30	PPG	←	Toggle	PWM	N/A	←
		TOAA31	PPG	←	PWM	←	N/A	←
Ch2	TAB0 (master)	TOAB00	PPG	←	Toggle	←	Toggle	N/A
		TOAB01 to TOAB03	PPG	←	PWM	←	Triangular wave PWM	N/A
	TAA4 (slave)	TOAA40	PPG	←	Toggle	PWM	N/A	←
		TOAA41	PPG	←	PWM	←	N/A	←
Ch3	TAB1 (master)	TOAB10	PPG	←	Toggle	←	Toggle	←
		TOAB11 to TOAB13	PPG	←	PWM	←	Triangular wave PWM	←
	TAB2 (slave)	TOAB20	PPG	←	Toggle	PWM	Toggle	Triangular wave PWM
		TOAB21 to TOAB23	PPG	←	PWM	←	Triangular wave PWM	←

Remark The timing of transmitting data from the compare register of the master timer to the compare register of the slave timer is as follows.

- PPG: CPU write timing
- Toggle, PWM, triangular wave PWM: Timing at which timer counter and compare register match TOAAn0 and TOABm0

(1) Setting in free-running timer mode (compare function)

[Initial setting]

Master timer: TAA0CTL0.TAA0CE = 0 (operation disabled)
Slave timer: TAA1CTL0.TAA1CE = 0 (operation disabled)

[Initial setting of master timer (TAA0)]

- TAA0CTL1.TAA0MD2 to TAA0CTL1.TAA0MD0 = 101 (setting of free-running timer mode)
- TAA0OPT0.TAA0CCS1 and TAA0OPT0.TAA0CCS0 = 00 (setting of capture/compare select bit to "compare".)
- TAA0CTL1.TAA0CKS2 to TAA0CTL1.TAA0CKS0 (setting of count clock (any))
- TAA0CCR1 and TAA0CCR0 registers are set.

[Initial setting of slave timer (TAA1)]

- TAA1CTL1.TAA1SYE = 1 (setting of timer-tuned operation)
- TAA1CTL1.TAA1MD2 to TAA1CTL1.TAA1MD0 = 101 (setting of free-running timer mode)
- TAA1OPT0.TAA1CCS1 and TAA1OPT0.TAA1CCS0 = 00 (setting of capture/compare select bit to "compare".)
- TAA1CCR0 and TAA1CCR1 registers are set.

Remark Initial setting of the master timer and slave timer may be performed in any order.

[Starting counting]

<1> Set TAA0CTL0.TAA0CE of the master timer to 1.
<2> Start counting.
<3> Changing the setting of the register during operation
  - The compare register can be rewritten (anytime write).

[End condition]

- Set TAA0CTL0.TAA0CE of the master timer to 0.

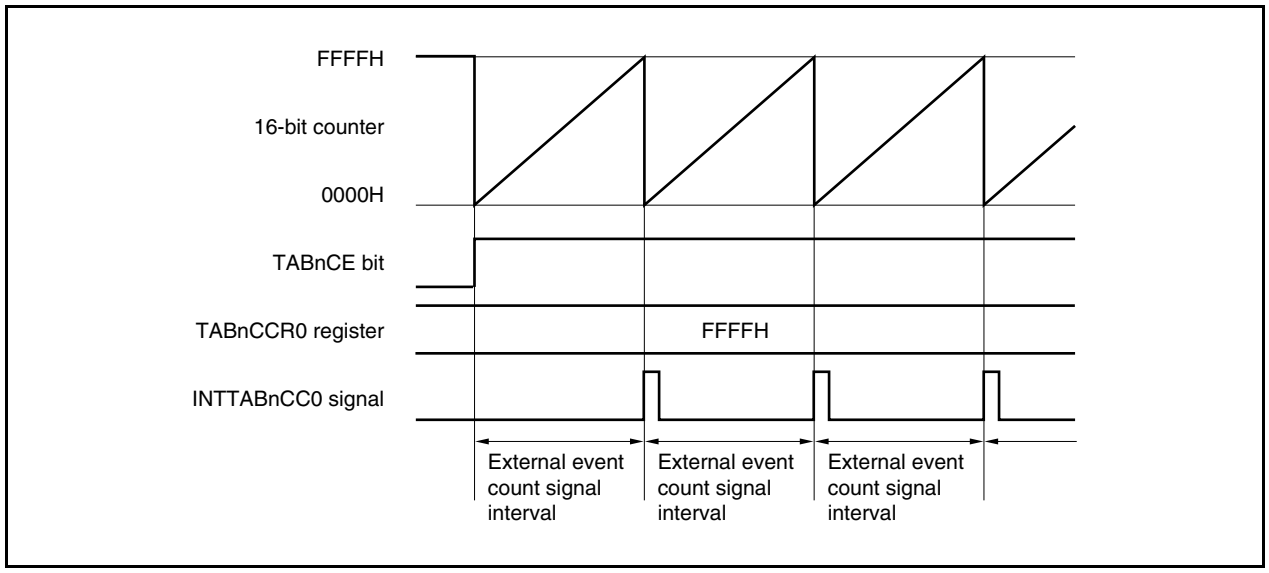
(2) Operation timing in external event count mode

Cautions 1. In the external event count mode, do not set the TABnCCR0 register to 0000H.

2. In the external event count mode, use of the timer output is disabled. If performing timer output using external event count input, set the interval timer mode, and select the operation enabled by the external event count input for the count clock (TABnCTL1.TABnMD2 to TABnCTL1.TABnMD0 bits = 000, TABnCTL1.TABnEEE bit = 1).

(a) Operation if TABnCCR0 register is set to FFFFH

If the TABnCCR0 register is set to FFFFH, the 16-bit counter counts to FFFFH each time the valid edge of the external event count signal has been detected. The 16-bit counter is cleared to 0000H in synchronization with the next count-up timing, and the INTTABnCC0 signal is generated. At this time, the TABnOPT0.TABnOVF bit is not set.



8.6 Timer-Tuned Operation Function

Timer AA and timer AB have a timer-tuned operation function.
The timers that can be synchronized are listed in Table 8-9.

Table 8-9. Tuned Operation Function of Timers

Master Timer	Slave Timer
TAA0	TAA1
TAA2	TAA3
TAB0	TAA4
TAB1	TAB2

For details of the timer-tuned operation function, see **7.6 Timer-Tuned Operation Function**.

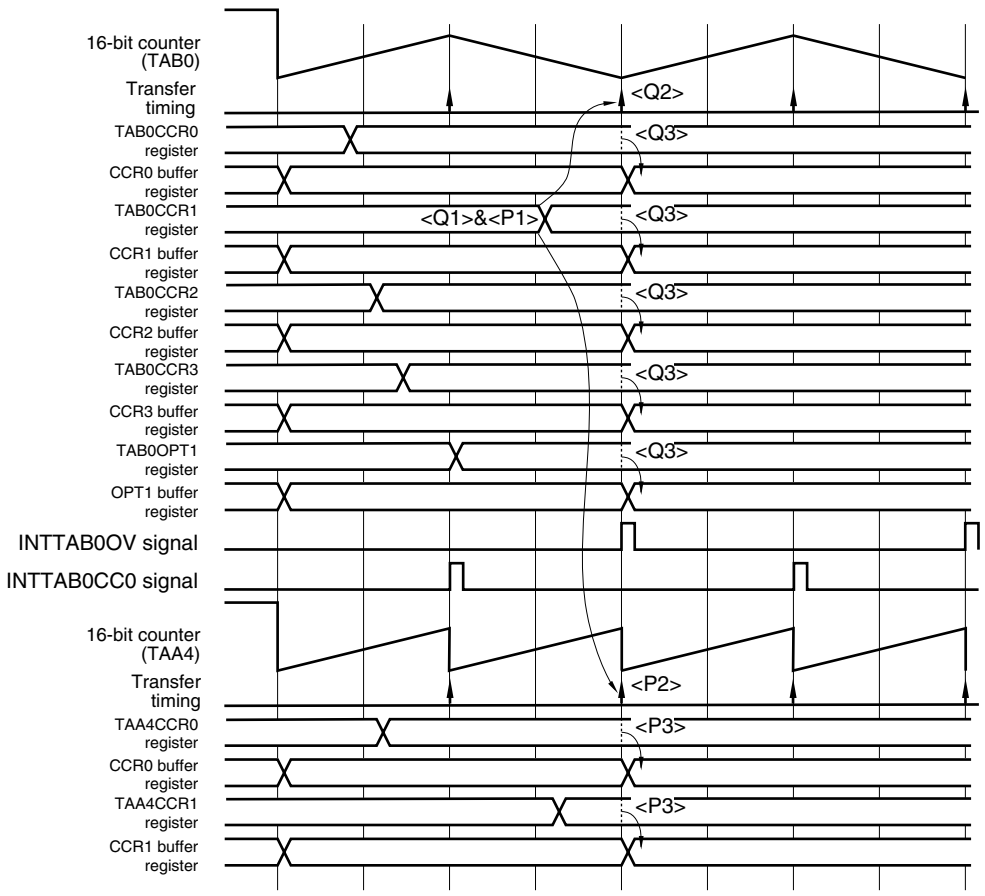
10.2 Configuration

The motor control function consists of the following hardware.

Item	Configuration
Timer register	Dead-time counters 1 to 3
Compare register	TAB0 dead-time compare register (TAB0DTC register)
Control registers	TAB0 option register 0 (TAB0OPT0) TAB0 option register 1 (TAB0OPT1) TAB0 option register 2 (TAB0OPT2) TAB0 I/O control register 3 (TAB0IOC3) High-impedance output control registers 0, 1 (HZA0CTL0, HZA0CTL1)

- 6-phase PWM output can be produced with dead time by using the output of TAB0 (TOAB01, TOAB02, TOAB03)
- The output level of the 6-phase PWM output can be set individually.
- The 16-bit timer/counter of TAB0 counts up/down triangular waves. When the timer/counter underflows and when a cycle match occurs, an interrupt is generated. Interrupt generation, however, can be suppressed up to 31 times.
- TAA4 can execute counting at the same time as TAB0 (timer tuning operation function). TAA4 can be set in four ways as it can generate two types of A/D trigger sources (INTTAA4CC0 and INTTAA4CC1), and two types of interrupts: on underflow interrupt (INTTAB0OV) and cycle match interrupt (INTTAB0CC0).

Figure 10-26. Basic Operation in Batch Mode



[Operation of TAB0]

<Q1> Write the TAB0CCR1 register

<Q2> The target timing is the first transfer timing after a write to the TAB0CCR1 register.

<Q3> The values are transferred all at once at the transfer timing.

[Operation of TAA4]

<P1> Write the TAB0CCR1 register

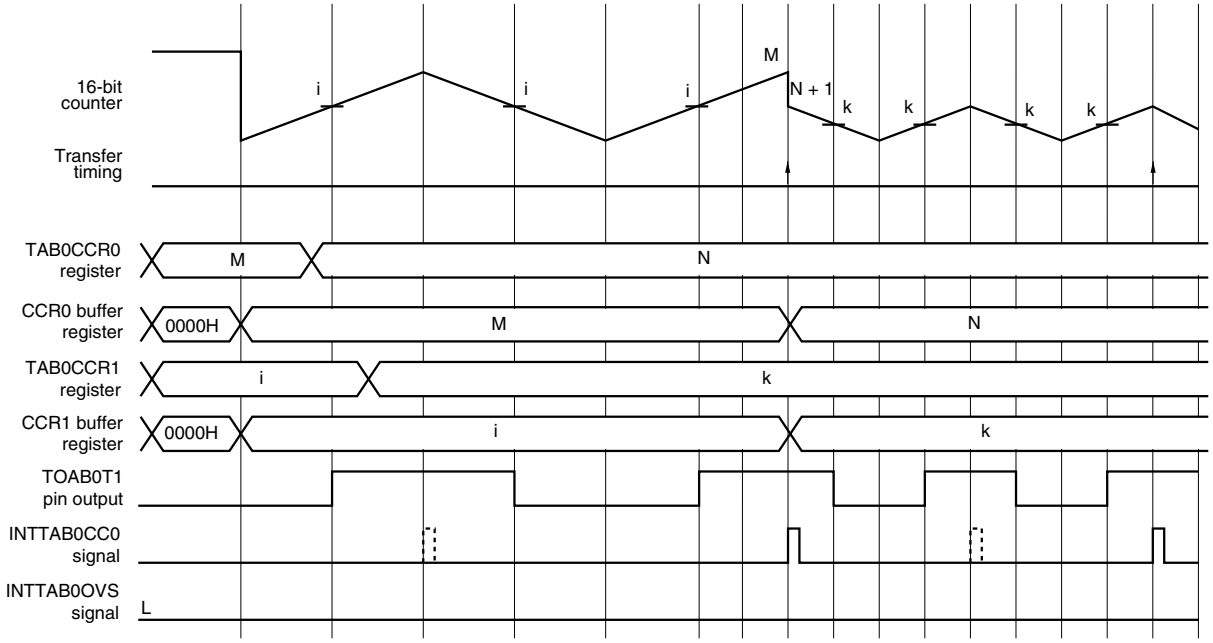
<P2> The target timing is the first transfer timing after a write to the TAB0CCR1 register.

<P3> The values are transferred all at once at the transfer timing.

(b) Rewriting TAB0CCR0 register

When rewriting the TAB0CCR0 register in the intermittent batch mode, the output waveform differs depending on where the occurrence of the crest or valley interrupt is specified by the interrupt culling setting. The following figure illustrates the change of the output waveform when interrupts are culled.

Figure 10-32. Rewriting TAB0CCR0 Register (When Crest Interrupt Is Set)



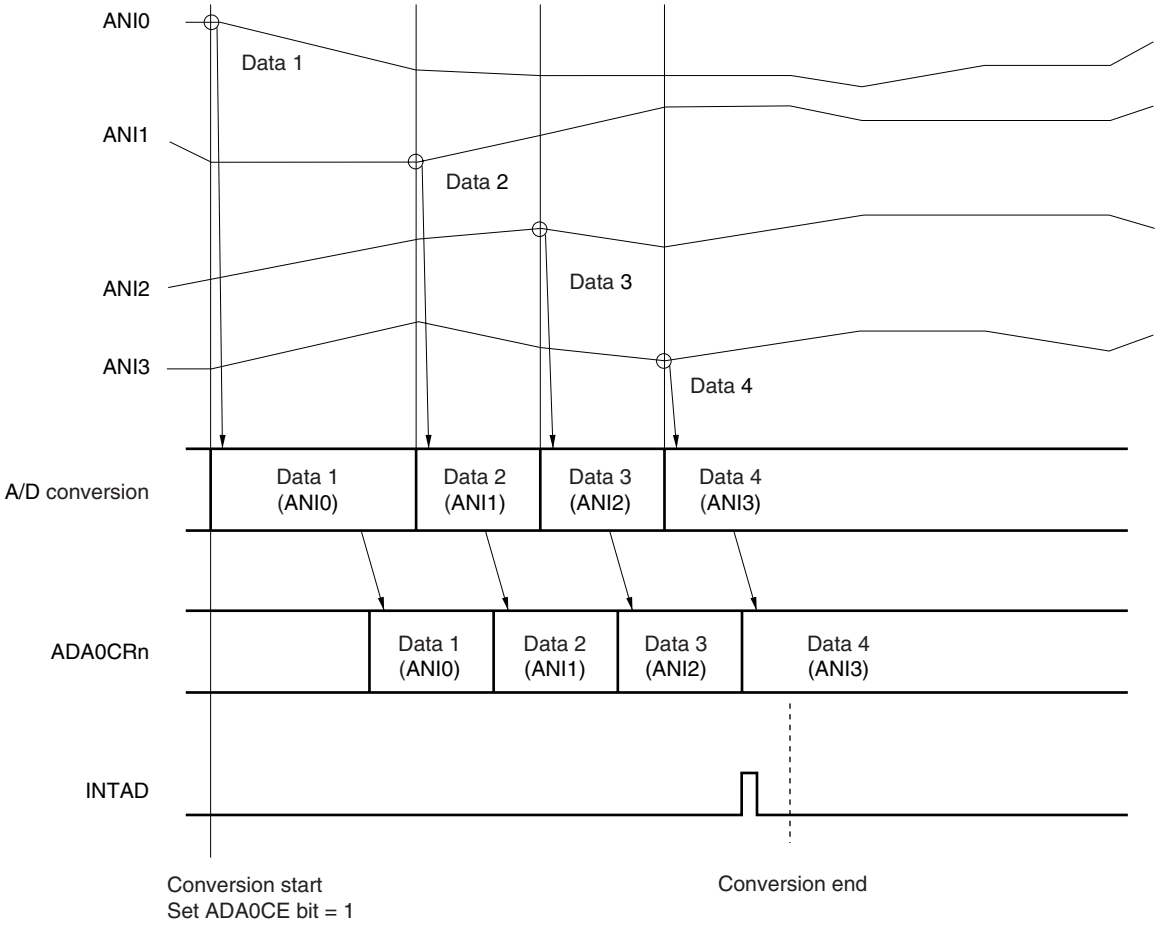
The transfer timing is generated when the crest interrupt occurs, the cycle of counting up and counting down changes, and an asymmetrical triangular wave is output.

Remarks 1. This is an example of the operation when the TAB0OPT1.TAB0ICE bit = 1, TAB0OPT1.TAB0IOE bit = 0, TAB0OPT1.TAB0ID4 to TAB0OPT1.TAB0ID0 bits = 00001.

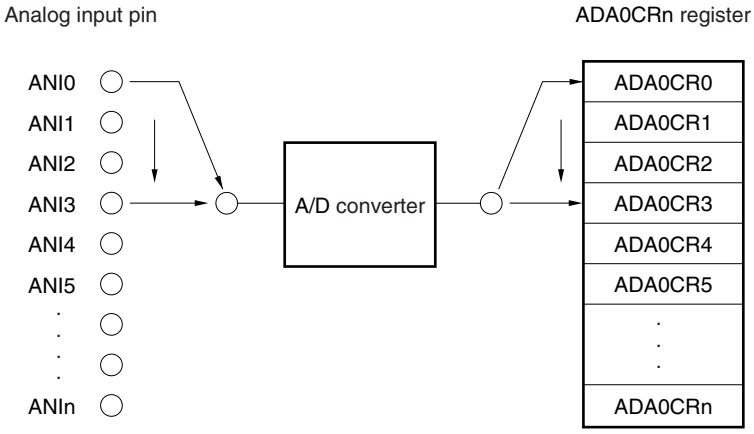
2. : Culled interrupt

Figure 13-6. Timing Example of One-Shot Scan Mode Operation (ADA0S Register = 03H)

(a) Timing example



(b) Block diagram



(1) V850ES/HE3, V850ES/HF3

After reset: FFFFH R/W Address: IMR3 FFFFF106H, IMR3L FFFFF106H, IMR3H FFFFF107H

	15	14	13	12	11	10	9	8
IMR3 (IMR3H[Note])	1	1	1	1	1	1	1	1
	7	6	5	4	3	2	1	0
IMR3L	1	1	WTMK	WTIMK	KRMK	DMAMK3	DMAMK2	DMAMK1

After reset: FFFFH R/W Address: IMR2 FFFFF104H, IMR2L FFFFF104H, IMR2H FFFFF105H

	15	14	13	12	11	10	9	8
IMR2 (IMR2H[Note])	DMAMK0	1	1	1	1	ADMK	IIC0MK	UD1TMK
	7	6	5	4	3	2	1	0
IMR2L	UD1RMK	UD1SMK	UD0TMK	UD0RMK	UD0SMK	CB1TMK	CB1RMK	CB0TMK

After reset: FFFFH R/W Address: IMR1 FFFFF102H, IMR1L FFFFF102H, IMR1H FFFFF103H

	15	14	13	12	11	10	9	8
IMR1 (IMR1H[Note])	CB0RMK	TM0EQMK0	TAA4CCMK1	TAA4CCMK0	TAA4OVMK	TAA3CCMK1	TAA3CCMK0	TAA3OVMK
	7	6	5	4	3	2	1	0
IMR1L	TAA2CCMK1	TAA2CCMK0	TAA2OVMK	TAA1CCMK1	TAA1CCMK0	TAA1OVMK	TAA0CCMK1	TAA0CCMK0

After reset: FFFFH R/W Address: IMR0 FFFFF100H, IMR0L FFFFF100H, IMR0H FFFFF101H

	15	14	13	12	11	10	9	8
IMR0 (IMR0H[Note])	TAA0OVMK	TAB0CCMK3	TAB0CCMK2	TAB0CCMK1	TAB0CCMK0	TAB0OVMK	PMK7	PMK6
	7	6	5	4	3	2	1	0
IMR0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIHMK	LVILMK

xxMKn	Setting of interrupt mask flag
0	Interrupt servicing enabled
1	Interrupt servicing disabled

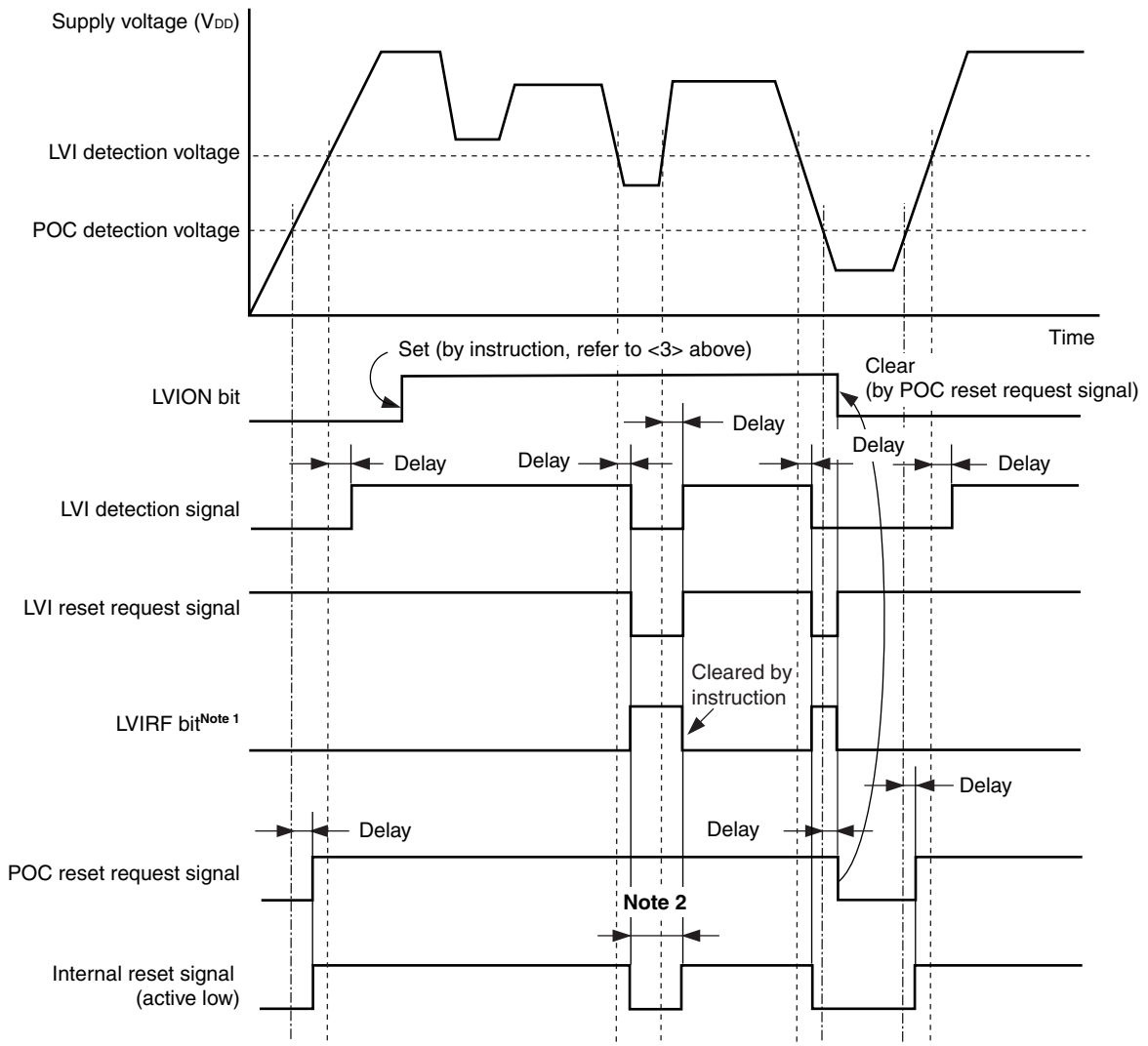
Note To read bits 8 to 15 of the IMR0 to IMR3 registers in 8-bit or 1-bit units, specify them as bits 0 to 7 of IMR0H to IMR3H registers.

Caution Set bits 15 to 6 of the IMR3 register, and bits 14 to 11 of the IMR2 register to 1. If the setting of these bits is changed, the operation is not guaranteed.

Remark xx: Identification name of each peripheral unit (see **Table 18-5 Interrupt Control Registers (xxICn)**).

n: Peripheral unit number (see **Table 18-5 Interrupt Control Registers (xxICn)**)

Figure 24-2. Operation Timing of Low-Voltage Detector (LVIMD Bit = 1)



Notes 1. The LVIRF bit is bit 0 of the reset source flag register (RESF). For details of RESF, see **CHAPTER 21 RESET FUNCTIONS**.

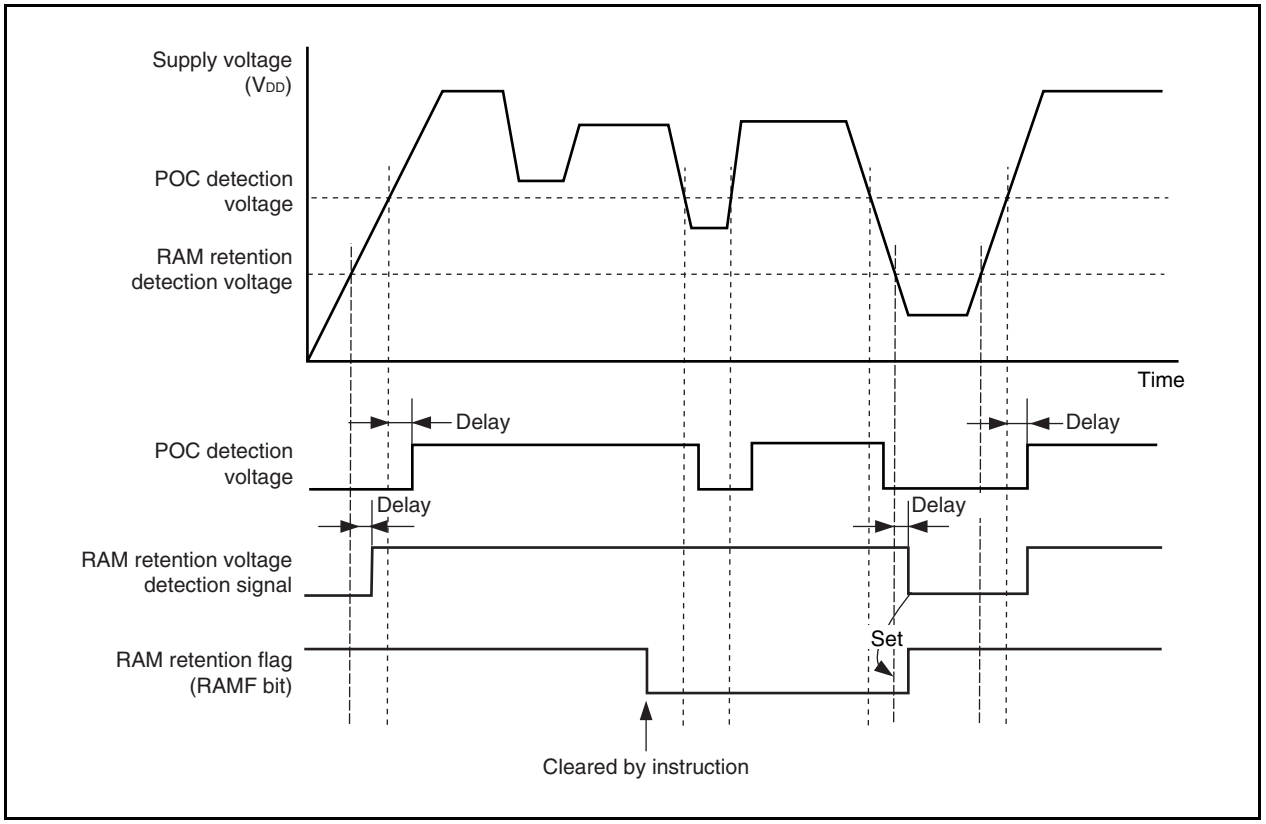
2. During the period in which the supply voltage is the set voltage or lower, the internal reset signal is retained (internal reset state).

24.5 RAM Retention Voltage Detection Operation

The supply voltage and detection voltage are compared. When the supply voltage drops below the detection voltage (including on power application), the RAMS.RAMF bit is set to 1.

When the POC function is not used and when the RAM retention voltage detection function is used, be sure to input an external reset signal if the detected voltage falls below the operating voltage.

Figure 24-4. Operation Timing of RAM Retention Voltage Detection Function



28.1.3 Maskable functions

Reset, NMI, INTWDT2, $\overline{\text{WAIT}}$, and $\overline{\text{HLDRQ}}$ (V850ES/HJ3 only) signals can be masked.

The maskable functions with the debugger (ID850QB) and the corresponding V850ES/Hx3 functions are listed below.

Table 28-2. Maskable Functions

Maskable Functions with ID850QB	Corresponding V850ES/Hx3 Functions
NMI0	NMI pin input
NMI1	Non-maskable interrupt request signal (INTWDT2) generation
NMI2	–
HLDRQ	$\overline{\text{HLDRQ}}$ pin input (V850ES/HJ3 only)
RESET	Reset signal generation by $\overline{\text{RESET}}$ pin input, low-voltage detector, clock monitor, or watchdog timer (WDT2) overflow
STOP	–
WAIT	$\overline{\text{WAIT}}$ pin input (V850ES/HJ3 only)
DBINT	–

28.1.4 Register

(1) On-chip debug mode register (OCDM)

The OCDM register is used to specify whether a pin provided with an on-chip debug function is used as an on-chip debug pin or as an ordinary port/peripheral function pin. It also is used to disconnect the internal pull-down resistor of the P05/INTP2/$\overline{\text{DRST}}$ pin.

After POC reset, the default value of the OCDM0 bit is “0” and the normal operation mode is set. To set the on-chip debug mode, therefore, the value of the OCDM0 bit must be changed to “1” by pin reset. If POC reset is generated during on-chip debugging, communication with MINICUBE is stopped. Therefore, reset by POC cannot be emulated.

This register is a special register and can be written only in a combination of specific sequences (see **3.4.7 Special registers**).

The OCDM register can be written only while a low level is input to the $\overline{\text{DRST}}$ pin.

This register can be read or written in 8-bit or 1-bit units.

29.2 Capacitance

(T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	f_X = 1 MHz, Unmeasured pins returned to 0 V.			10	pF

29.3 Operating Conditions

(T_A = –40 to +85°C, V_{DD} = EV_{DD}, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C = 4.7 μF)

Internal System Clock Frequency	Conditions	Supply Voltage		Unit
		V_{DD}, EV_{DD}	AV_{REF0}	
4 MHz ≤ f_{XX} ≤ 32 MHz		4.0 to 5.5	4.0 to 5.5	V
4 MHz ≤ f_{XX} ≤ 20 MHz	AD converter operating	3.7 to 5.5	4.0 to 5.5	V
	AD converter stop	3.7 to 5.5	3.7 to 5.5	V
f_{XT} = 32.768 kHz		3.7 to 5.5	3.7 to 5.5	V
f_{RL} = 240 kHz (TYP.)		3.7 to 5.5	3.7 to 5.5	V
f_{RH} = 8 MHz (TYP.)	AD converter operating	3.7 to 5.5	4.0 to 5.5	V
	AD converter stop	3.7 to 5.5	3.7 to 5.5	V

<R> **29.6.3 Supply current**

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = 3.7 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Normal operation mode[Note 2]	PLL operating	f_{XX} = 32 MHz (f_X = 8 MHz)	All peripheral function operating		39	51	mA
					All peripheral function stopped		32		mA
			PLL operating	f_{XX} = 20 MHz (f_X = 10 MHz)	All peripheral function operating		27	37	mA
					All peripheral function stopped		22		mA
			PLL stopped	f_{XX} = 16 MHz (f_X = 16 MHz)	All peripheral function operating		21	30	mA
					All peripheral function stopped		19		mA
	I_{DD2}	HALT mode[Note 2]	PLL operating	f_{XX} = 32 MHz (f_X = 8 MHz)	All peripheral function operating		24	34	mA
					All peripheral function stopped		18		mA
			PLL operating	f_{XX} = 20 MHz (f_X = 10 MHz)	All peripheral function operating		16	23	mA
					All peripheral function stopped		12		mA
			PLL stopped	f_{XX} = 16 MHz (f_X = 16 MHz)	All peripheral function operating		13	20	mA
					All peripheral function stopped		9		mA
	I_{DD3}	IDLE1 mode	PLL stopped[Note 3]	f_{XX} = 16 MHz (f_X = 16 MHz)	TAA, UARTD operating		2.4	3.6	mA
					All peripheral function stopped		1.6		mA
				f_{XX} = 8 MHz (f_X = 8 MHz)	TAA, UARTD operating		1.6	2.5	mA
					All peripheral function stopped		1.3		mA
			f_{XX} = High-speed internal oscillation (f_{RH})[Note 4]		TAA, UARTD operating		1.5	2.3	mA
					All peripheral function stopped		1.1		mA
	I_{DD4}	IDLE2 mode	PLL stopped[Note 3]	f_{XX} = 16 MHz (f_X = 16 MHz)			0.8	1.2	mA
				f_{XX} = 8 MHz (f_X = 8 MHz)			0.5	0.8	mA
			f_{XX} = High-speed internal oscillation (f_{RH})[Note 4]				0.2	0.5	mA
	I_{DD5}	Subclock operation mode[Notes 4, 5]	Crystal resonator (f_{XT} = 32.768 kHz)				80	400	μA
	I_{DD6}	Sub-IDLE mode[Notes 4, 5]	Crystal resonator (f_{XT} = 32.768 kHz)				20	190	μA
	I_{DD7}	STOP mode[Notes 4, 6]	Low-speed internal oscillator (f_{RL}) operating				18.5	100	μA
			Low-speed internal oscillator (f_{RL}) stopped				10.5	85	μA

Notes 1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. During SSCG operation, TYP. value + 2.5 mA, MAX. value + 4 mA

3. High-speed internal oscillator (f_{RH}) stopped.

4. When the main clock oscillator (f_{XX}) is stopped.

5. Low-speed internal oscillator (f_{RL}) operating, high-speed internal oscillator (f_{RH}) stopped.

6. When the subclock oscillator (f_{XT}) is not used.

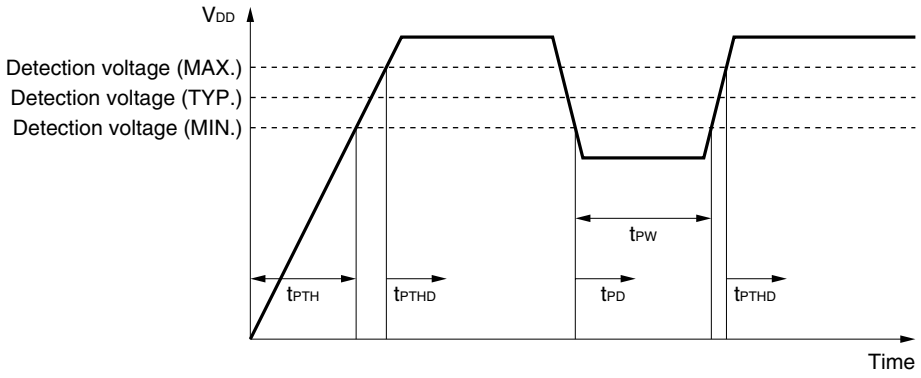
(9) POC circuit characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		3.3	3.5	3.7	V
Power supply startup time	t_{PTH}	V_{DD} = 0 V → 3.3 V	0.002			ms
Response delay time 1 Note 1	t_{PTHD}	After V_{DD} reaches 3.7 V on power application			2.0	ms
Response delay time 2 Note 2	t_{PD}	After V_{DD} drops below 3.3 V on power drop			1.0	ms
Minimum V_{DD} width	t_{PW}		0.2			ms

Notes 1. The time required to release a reset after the detection voltage is detected.

2. The time required to output a reset after the detection voltage is detected.



32.2 Capacitance

(T_A = 25°C, V_{DD} = EV_{DD} = BV_{DD} = AV_{REF0} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

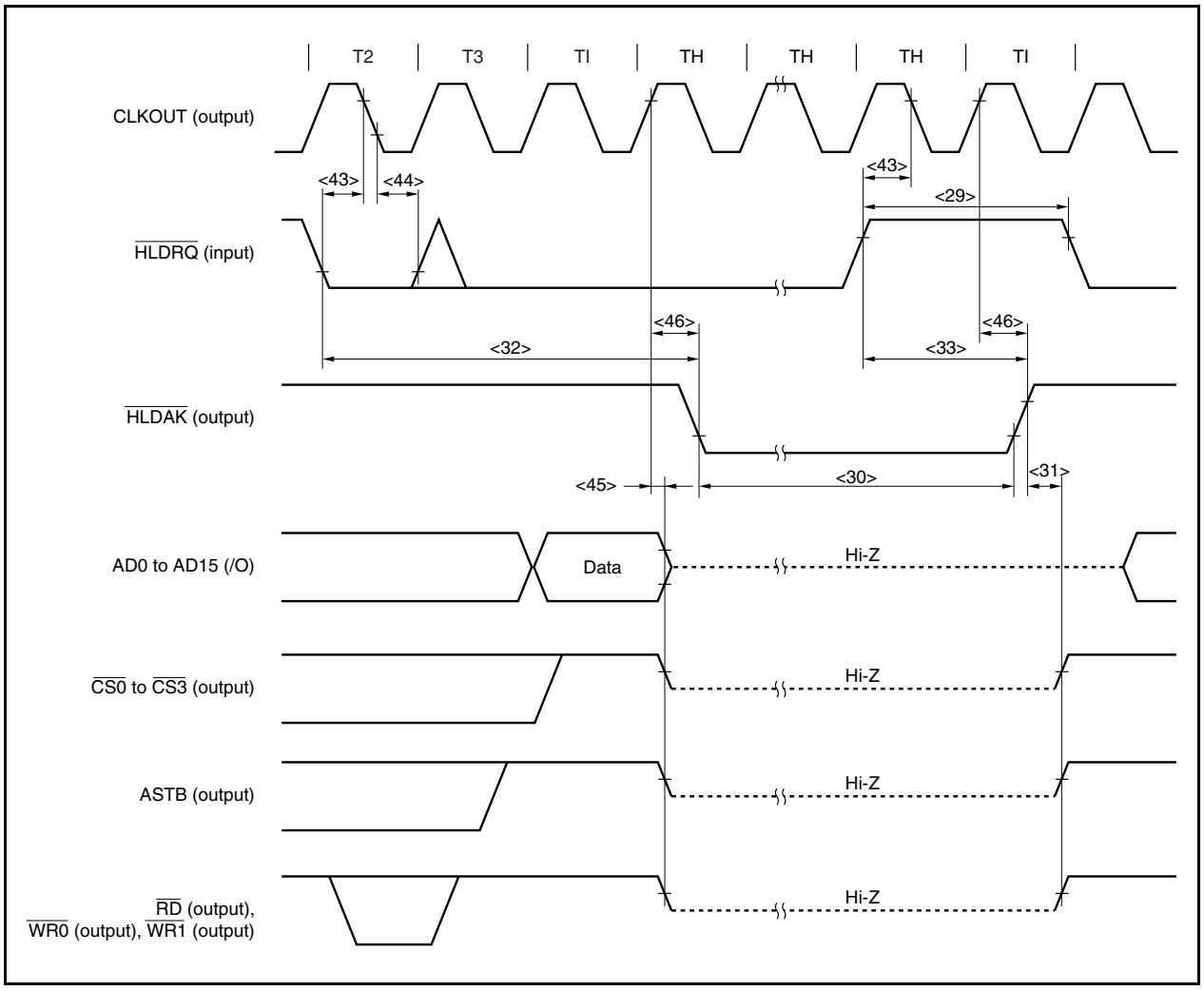
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	f_X = 1 MHz, Unmeasured pins returned to 0 V.			10	pF

32.3 Operating Conditions

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD}, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C = 4.7 μF)

Internal System Clock Frequency	Conditions	Supply Voltage		Unit
		V_{DD} = EV_{DD} = BV_{DD}	AV_{REF0}	
4 MHz ≤ f_{XX} ≤ 32 MHz		4.0 to 5.5	4.0 to 5.5	V
4 MHz ≤ f_{XX} ≤ 20 MHz	AD converter operating	3.7 to 5.5	4.0 to 5.5	V
	AD converter stop	3.7 to 5.5	3.7 to 5.5	V
32 kHz ≤ f_{XT} ≤ 35 kHz		3.7 to 5.5	3.7 to 5.5	V
f_{RL} = 240 kHz (TYP.)		3.7 to 5.5	3.7 to 5.5	V
f_{RH} = 8 MHz (TYP.)	AD converter operating	3.7 to 5.5	4.0 to 5.5	V
	AD converter stop	3.7 to 5.5	3.7 to 5.5	V

Bus hold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T3
TI
TH
TH
TH
TI
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<44>
<43>
<29>
HLDRQ (input)
<46>
<46>
<32>
<33>
HLDAK (output)
<45>
<30>
<31>
AD0 to AD15 (/O)
Data
Hi-Z
CS0 to CS3 (output)
Hi-Z
ASTB (output)
Hi-Z
RD (output),
WR0 (output), WR1 (output)
Hi-Z