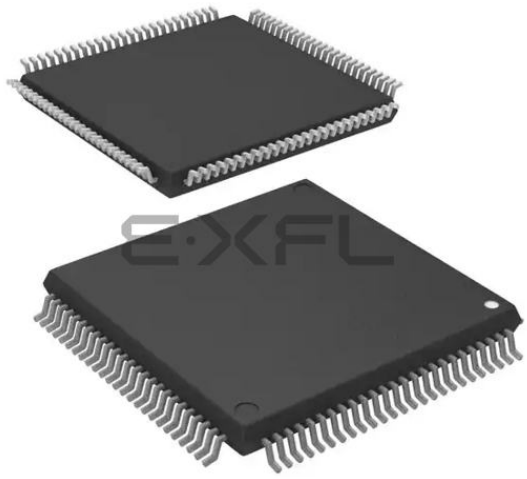
Renesas Electronics America Inc - UPD70F3752GC-UEU-AX Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

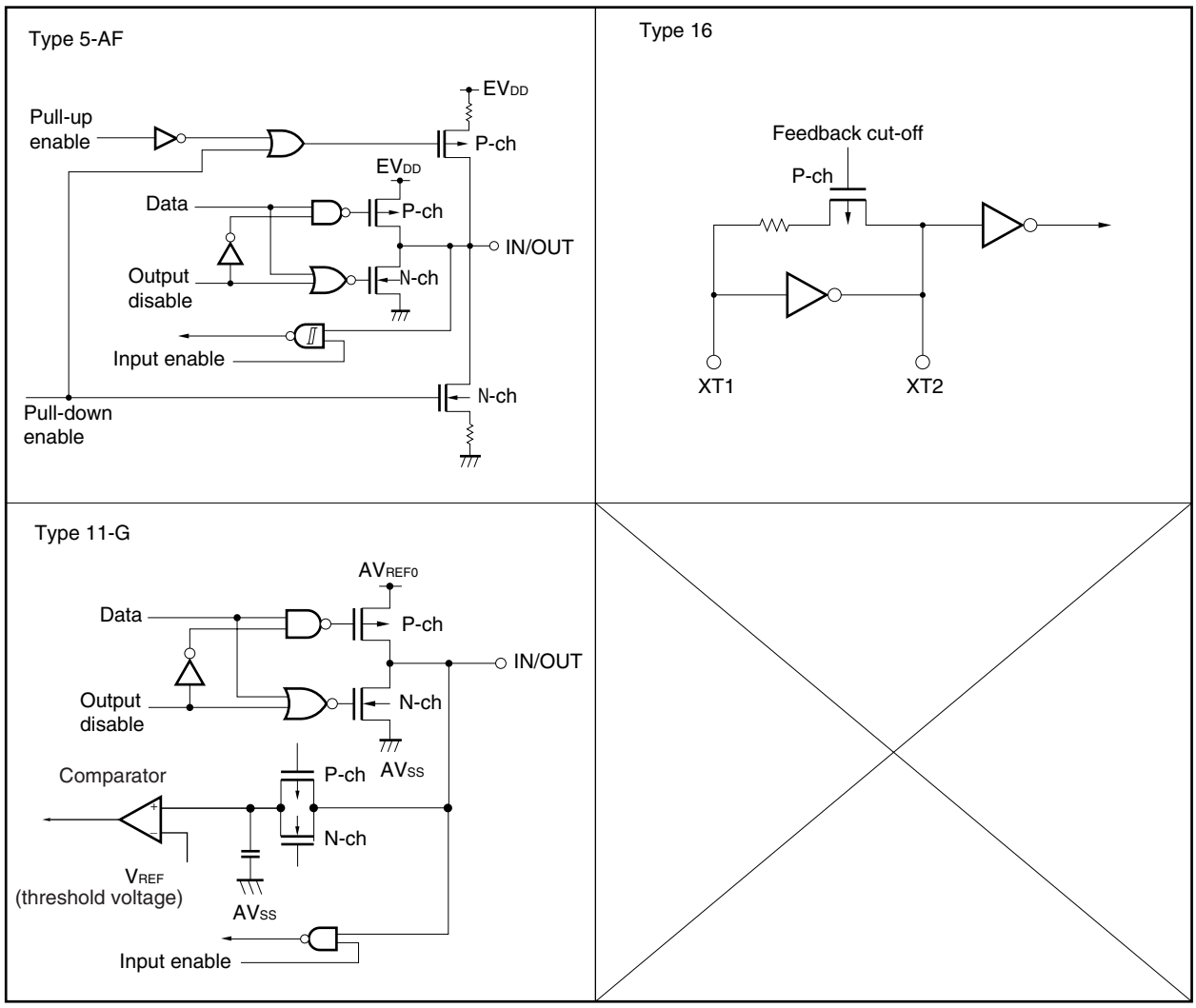
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3752gc-ueu-ax

Pin identification

AD0 to AD15:	Address/data bus	$\overline{\text{RESET}}$:	Reset
ADTRG:	AD trigger input	RXDD0 to RXDD5:	Receive data
ANI0 to ANI23:	Analog input	$\overline{\text{SCKB0}}$ to $\overline{\text{SCKB2}}$:	Serial clock
ASTB:	Address strobe	SCL00:	Serial clock
AV_{REF0}:	Analog V_{DD}	SDA00:	Serial data
AV_{SS}:	Analog V_{SS}	SIB0 to SIB2:	Serial input
BV_{DD}:	Power supply for bus interface	SOB0 to SOB2:	Serial output
BV_{SS}:	Ground for bus interface	TIAA00, TIAA01,	
CLKOUT:	Clock output	TIAA10, TIAA11,	
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$:	Chip select	TIAA20, TIAA21,	
DCK:	Debug clock	TIAA30, TIAA31,	
DDI:	Debug data input	TIAA40, TIAA41,	
DDO:	Debug data output	TIAB00, TIAB01,	
DMS:	Debug mode select	TIAB02, TIAB03,	
$\overline{\text{DRST}}$:	Debug reset	TIAB10, TIAB11,	
EV_{DD}:	Power supply for external pin	TIAB12, TIAB13,	
EV_{SS}:	Ground for external pin	TIAB20, TIAB21,	
FLMD0, FLMD1:	Flash programming mode	TIAB22, TIAB23:	Timer input
$\overline{\text{HLDAK}}$:	Hold acknowledge	TOAA00, TOAA01,	
$\overline{\text{HLDRQ}}$:	Hold request	TOAA10, TOAA11,	
INTP0 to INTP14:	External interrupt input	TOAA20, TOAA21,	
KR0 to KR7:	Key return	TOAA30, TOAA31,	
NMI:	Non-maskable interrupt request	TOAA40, TOAA41,	
P00 to P06:	Port 0	TOAB00, TOAB01,	
P10, P11:	Port 1	TOAB02, TOAB03,	
P30 to P39:	Port 3	TOAB10, TOAB11,	
P40 to P42:	Port 4	TOAB12, TOAB13,	
P50 to P55:	Port 5	TOAB20, TOAB21,	
P60 to P615:	Port 6	TOAB22, TOAB23,	
P70 to P715:	Port 7	TOAB0B1, TOAB0B2,	
P80, P81:	Port 8	TOAB0B3, TOAB0T1,	
P90 to P915:	Port 9	TOAB0T2, TOAB0T3:	Timer output
P120 to P127:	Port 12	TXDD0 to TXDD5:	Transmit data
PCD0 to PCD3:	Port CD	V_{DD}:	Power supply
PCL:	Programmable clock output	V_{SS}:	Ground
PCM0 to PCM5:	Port CM	$\overline{\text{WAIT}}$:	Wait
PCS0 to PCS7:	Port CS	$\overline{\text{WR0}}$:	Write strobe low level data
PCT0 to PCT7:	Port CT	$\overline{\text{WR1}}$:	Write strobe high level data
PDL0 to PDL15:	Port DL	X1, X2:	Crystal for main clock
$\overline{\text{RD}}$	Read	XT1, XT2:	Crystal for subclock
REGC:	Regulator control		

Figure 2-1. Pin I/O Circuit Types (2/2)



5.4.2 Bus size setting function

Each external memory area selected by $\overline{CSn}$ can be set by using the BSC register. However, the bus size can be set to 8 bits and 16 bits only.

The external memory area of the V850ES/HJ3 is selected by $\overline{CS0}$ to $\overline{CS3}$.

(1) Bus size configuration register (BSC)

The BSC register can be read or written in 16-bit units.

Reset sets this register to 5555H.

Caution Write to the BSC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the BSC register are complete.

After reset: 5555H R/W Address: FFFFF066H

	15	14	13	12	11	10	9	8
BSC	0	1	0	1	0	1	0	1

7	6	5	4	3	2	1	0
0	BS30	0	BS20	0	BS10	0	BS00
	$\overline{CS3}$		$\overline{CS2}$		$\overline{CS1}$		$\overline{CS0}$

BSn0	Data bus width of CSn space (n = 0 to 3)
0	8 bits
1	16 bits

Caution Be sure to set bits 14, 12, 10, and 8 to “1”, and set bits 15, 13, 11, 9, 7, 5, 3, and 1 to “0”.

(4) SSCG control register (SSCGCTL)

The SSCGCTL register is an 8-bit register that controls the spread spectrum clock generator (SSCG).

This register can be read or written in 8-bit or 1-bit units.

After reset: 00H R/W Address: FFFFF3F0H

	7	6	5	4	3	2	<1>	<0>
SSCGCTL	0	0	0	0	0	0	SELSSCG	SSCGON

SELSSCG	Selection of clock to be output from multiplication block
0	PLL output ($f_{PLL} = f_{PLLO}$)
1	SSCG output ($f_{PLL} = f_{SSCGO}$)

SSCGON	SSCG function operation enable/disable
0	SSCG stopped
1	SSCG operating

Cautions 1. Write the SSCGCTL register bits when both PLL and SSCG stop (PLLCTL.PLLON bit = 0) or are in the lock status.

2. The SELSSCG bit can be set to 1 only when the SSCGON bit = 1. When the SSCGON bit is set to 0, the SELSSCG bit is automatically set to 0 (PLL output).

3. If the PLLCTL.PLLON bit is set to 0 or the main clock is stopped while the SSCGON bit = 1, SSCG stops operating.

4. When SSCG starts operating, time until SSCG is locked is required.

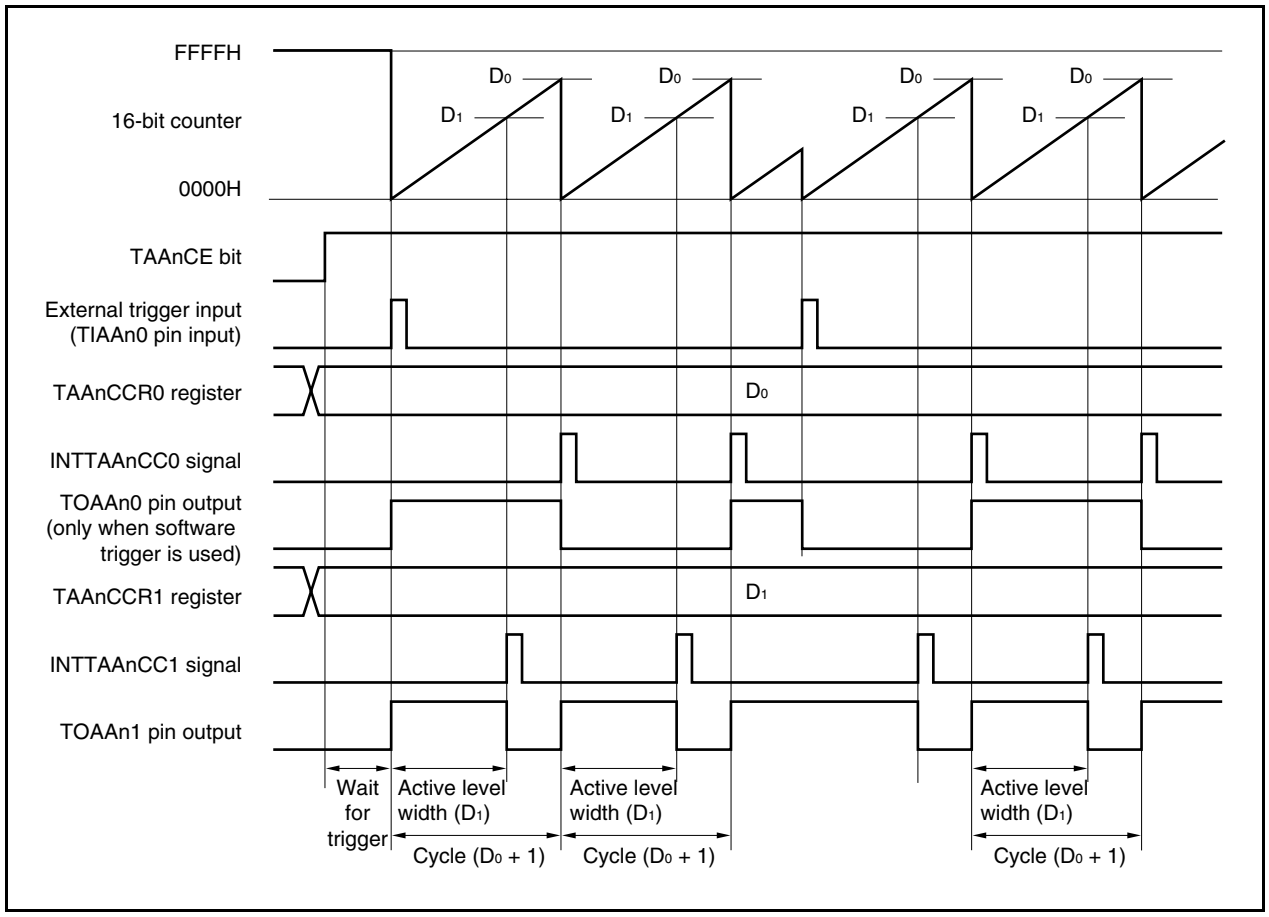
- **If the SSCGON bit is changed from 0 to 1 when the PLLCTL.PLLON bit = 1, make sure by software that the lockup time of SSCG (1 ms or more) elapses.**
- **If the PLLCTL.PLLON bit is changed from 0 to 1 after the SSCGON bit has been set to 1, set SSCG lockup time (1 ms or more) to the PLLS register (this is because the lockup time of SSCG is longer than that of PLL).**
- **Set a value two times the SSCG lockup time (1 ms or more) to the OSTS register.**

The relationship between the PLL/SSCG mode and PLLCTL.PLLON/SSCGCTL.SSCGON bit is shown below.

Table 6-3. Operation Condition of PLL/SSCG Mode

PLLCTL.PLLON Bit	SSCGCTL.SSCGON Bit	PLL Mode	SSCG Mode
0	0	Stops	Stops
0	1		
1	0	Operates	Stops
1	1		Operates

Figure 7-17. Basic Timing in External Trigger Pulse Output Mode



16-bit timer/event counter AA waits for a trigger when the TAAnCE bit is set to 1. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting at the same time, and outputs a PWM waveform from the TOAAn1 pin. If the trigger is generated again while the counter is operating, the counter is cleared to 0000H and restarted. (The output of the TOAAn0 pin is inverted. The TOAAn1 pin outputs a high level regardless of the status (high/low) when a trigger occurs.)

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TAAnCCR1 register) × Count clock cycle
Cycle = (Set value of TAAnCCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TAAnCCR1 register)/(Set value of TAAnCCR0 register + 1)

The compare match request signal INTTAAnCC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTAAnCC1 is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

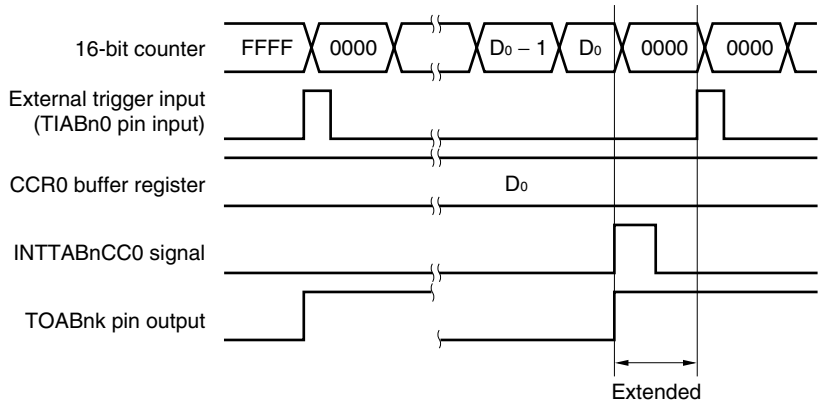
The value set to the TAAnCCRm register is transferred to the CCRm buffer register when the count value of the 16-bit counter matches the value of the CCRm buffer register and the 16-bit counter is cleared to 0000H.

The valid edge of an external trigger input signal, or setting the software trigger (TAAnCTL1.TAAnEST bit) to 1 is used as the trigger.

Remark n = 0 to 4, m = 0, 1

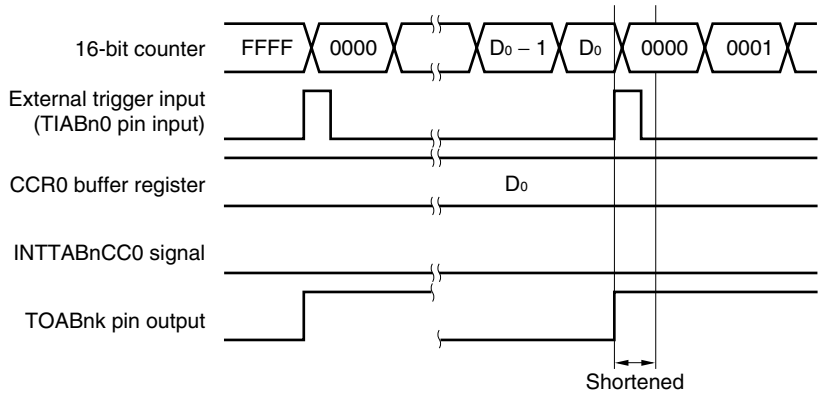
(d) Conflict between trigger detection and match with CCR0 buffer register

If the trigger is detected immediately after the INTTABnCC0 signal is generated, the 16-bit counter is cleared to 0000H and continues counting up. Therefore, the active period of the TOABnk pin is extended by time from generation of the INTTABnCC0 signal to trigger detection.



Remark k = 1 to 3

If the trigger is detected immediately before the INTTABnCC0 signal is generated, the INTTABnCC0 signal is not generated. The 16-bit counter is cleared to 0000H, the TOABnk pin is asserted, and the counter continues counting. Consequently, the inactive period of the PWM waveform is shortened.



Remark k = 1 to 3

8.6 Timer-Tuned Operation Function

Timer AA and timer AB have a timer-tuned operation function.
The timers that can be synchronized are listed in Table 8-9.

Table 8-9. Tuned Operation Function of Timers

Master Timer	Slave Timer
TAA0	TAA1
TAA2	TAA3
TAB0	TAA4
TAB1	TAB2

For details of the timer-tuned operation function, see **7.6 Timer-Tuned Operation Function**.

(2) Batch rewrite mode (transfer mode)

This mode is set by clearing the TAB0OPT0.TAB0CMS bit to 0, the TAB0OPT1.TAB0ID4 to TAB0OPT1.TAB0ID0 bits to 00000, and the TAB0OPT2.TAB0RDE bit to 0.

In this mode, the values written to each compare register are transferred to the internal buffer register all at once at the transfer timing and compared with the counter value.

(a) Rewriting procedure

If data is written to the TAB0CCR1 register, the values set to the TAB0CCR0 to TAB0CCR3, TAB0OPT1, TAA4CCR0, and TAA4CCR1 registers are transferred all at once to the internal buffer register at the next transfer timing. Therefore, write to the TAB0CCR1 register last. Writing to the register is prohibited after the TAB0CCR1 register has been written and before the transfer timing is generated (until the crest (match between the 16-bit counter value and TAB0CCR0 register value) or the valley (match between the 16-bit counter value and 0001H)). The operation procedure is as follows.

<1> Rewriting the TAB0CCR0, TAB0CCR2, TAB0CCR3, TAB0OPT1, TAA4CCR0, and TAA4CCR1 registers
(Do not rewrite registers that do not have to be rewritten.)

<2> Rewriting the TAB0CCR1 register
(Rewrite the same value to the register even when it is not necessary to rewrite the TAB0CCR1 register.)

<3> Holding the next rewriting pending until the transfer timing is generated
(Rewrite the register next time after the INTTAB0OV or INTTAB0CC0 interrupt has occurred.)

<4> Return to <1>.

CHAPTER 11 WATCH TIMER FUNCTIONS

11.1 Functions

The watch timer has the following functions.

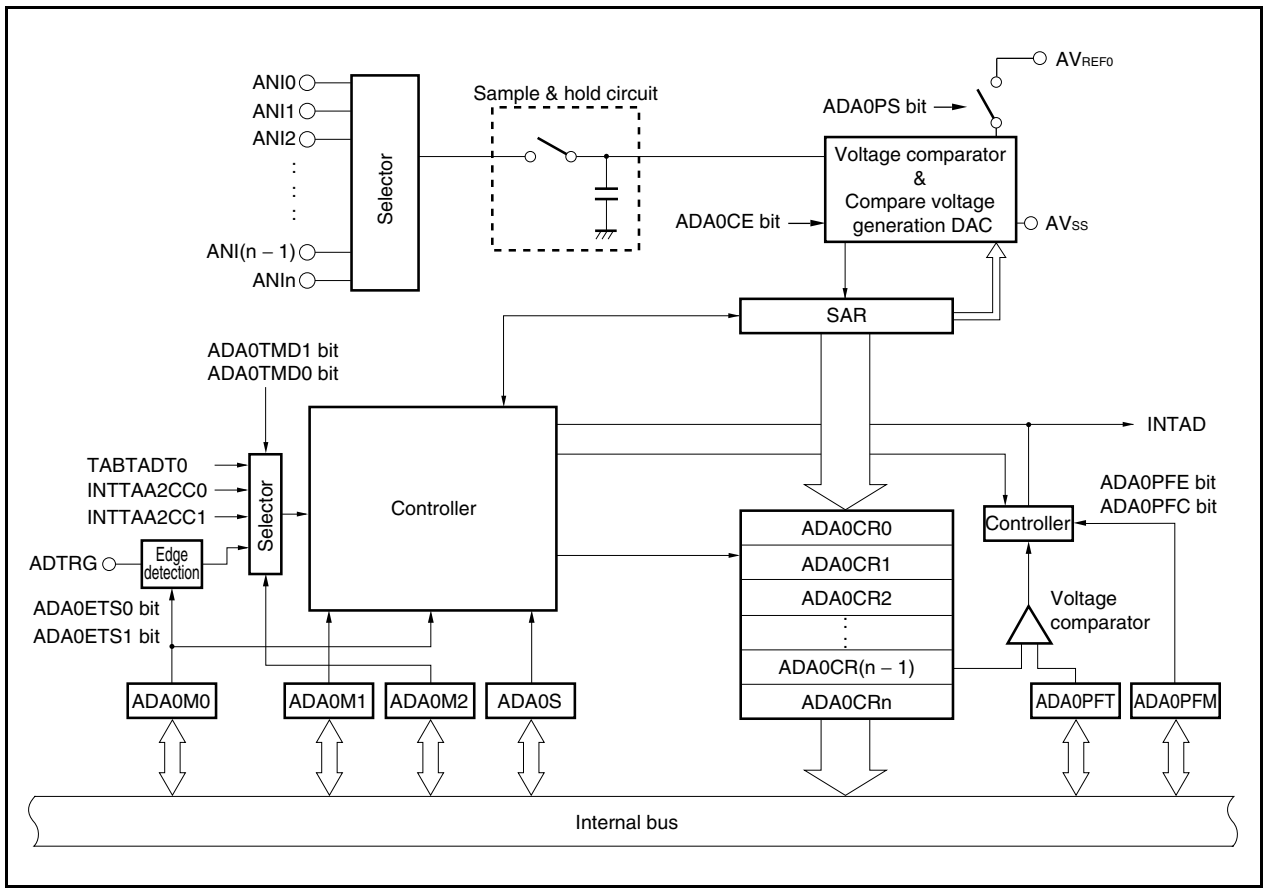
- Watch timer: An interrupt request signal (INTWT) is generated at intervals of 0.5 or 0.25 seconds by using the main clock or subclock.
- Interval timer: An interrupt request signal (INTWTI) is generated at set intervals.

The watch timer and interval timer functions can be used at the same time.

13.3 Configuration

The block diagram of the A/D converter is shown below.

Figure 13-1. Block Diagram of A/D Converter



The A/D converter includes the following hardware.

Table 13-1. Configuration of A/D Converter

Item	Configuration
Analog inputs	m channels (ANIn pins)
Registers	Successive approximation register (SAR) A/D conversion result register n (ADA0CRn) A/D conversion result register nH (ADCRnH): Only higher 8 bits can be read
Control registers	A/D converter mode registers 0 to 2 (ADA0M0 to ADA0M2) A/D converter channel specification register 0 (ADA0S) Power fail compare mode register (ADA0PFM) Power fail compare threshold value register (ADA0PFT)

(6) UARTDn status register (UDnSTR)

The UDnSTR register is an 8-bit register that displays the UARTDn transfer status and reception error contents. This register can be read or written in 8-bit or 1-bit units, but the UDnTSF bit is a read-only bit, while the UDnPE, UDnFE, and UDnOVE bits can be read and written. However, these bits can only be cleared by writing 0; they cannot be set by writing 1 (even if 1 is written to them, the value is retained).

The initialization conditions are shown below.

Register/Bit	Initialization Conditions
UDnSTR register	• Reset • UDnCTL0.UDnPWR bit = 0
UDnSSF bit	• UDnRXE bit of UDnCTL0 register = 0 • UDnSRS bit of UDnOPT1 register = 0
UDnDCE bit	• UDnDCS bit of UDnOPT1 register = 0 • UDnTXE bit of UDnCTL0 register = 0
UDnTSF bit	• UDnCTL0.UDnTXE bit = 0
UDnPE, UDnFE, UDnOVE bits	• 0 write • UDnCTL0.UDnRXE bit = 0

Caution To clear the status flag, use a 1-bit manipulation instruction, or write the inverted value of a read value by using an 8-bit manipulation instruction and clear all the bits that have been set when read at once.

(3/4)

STT0	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in STOP mode): Generates a start condition (for starting as master). The SDA00 line is changed from high level to low level while the SCL00 line is high level and then the start condition is generated. Next, after the rated amount of time has elapsed, the SCL00 line is changed to low level (wait status). When a third party is communicating • When communication reservation function is enabled (IICF0.IICRSV0 bit = 0) Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released. • When communication reservation function is disabled (IICRSV0 bit = 1) The IICF0.STCF0 bit is set to 1 and the information set (1) to the STT0 bit is cleared. No start condition is generated. In the wait state (when master device): Generates a restart condition after releasing the wait.

Cautions concerning set timing

For master reception: Cannot be set to 1 during transfer. Can be set to 1 only when the ACKE0 bit has been cleared to 0 and slave has been notified of final reception.

For master transmission: A start condition may not be generated normally during the $\overline{\text{ACK}}$ period. Set to 1 during the wait period that follows output of the ninth clock.

- Cannot be set to 1 at the same time as the SPT0 bit.
- When the STT0 bit is set to 1, setting the STT0 bit to 1 again is disabled until the setting is cleared to 0.

Condition for clearing (STT0 bit = 0)	Condition for setting (STT0 bit = 1)
• When the STT0 bit is set to 1 in the communication reservation disabled status • Cleared when start condition is generated by master device • When the LREL0 bit = 1 (exit from communications) • When the IICE0 bit = 1 → 0 (operation stop) • Reset	• Set by instruction

Remark The STT0 bit is 0 if it is read after data setting.

(7) IIC division clock selection registers 0 (OCKS0)

The OCKS0 register controls the I²C00 division clock.

This register controls the I²C00 division clock via the OCKS0 register.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: OCKS0 FFFFF340H

	7	6	5	4	3	2	1	0
OCKS0	0	0	0	OCKSEN0	OCKSTH0	0	OCKS01	OCKS00

OCKSEN0	Operation setting of I²C division clock
0	Disable I²C division clock operation
1	Enable I²C division clock operation

OCKSTH0	OCKS01	OCKS00	Selection of I²C division clock
0	0	0	$f_{XX}/2$
0	0	1	$f_{XX}/3$
0	1	0	$f_{XX}/4$
0	1	1	$f_{XX}/5$
1	×	×	f_{XX}

(8) IIC shift register 0 (IIC0)

The IIC0 shift register is used for serial transmission/reception (shift operations) that is synchronized with the serial clock.

This register can be read or written in 8-bit units, but data should not be written to the IIC0 shift register during a data transfer.

Access (read/write) the IIC0 shift register only during the wait period. Accessing this register in communication states other than the wait period is prohibited. However, for the master device, the IIC0 shift register can be written once only after the transmission trigger bit (IICC0.STT0 bit) has been set to 1.

When the IIC0 shift register is written during wait, the wait is cancelled and data transfer is started.

Reset sets this register to 00H.

After reset: 00H R/W Address: IIC0 FFFFFD80H

	7	6	5	4	3	2	1	0
IIC0								

(2) DMA destination address registers 0 to 3 (DDA0 to DDA3)

The DDA0 to DDA3 registers set the DMA destination address (26 bits each) for DMA channel n (n = 0 to 3).

These registers are divided into two 16-bit registers, DDAnH and DDAnL.

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DDA0H FFFFF086H, DDA1H FFFFF08EH, DDA2H FFFFF096H, DDA3H FFFFF09EH, DDA0L FFFFF084H, DDA1L FFFFF08CH, DDA2L FFFFF094H, DDA3L FFFFF09CH

DDAnH (n = 0 to 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IR	0	0	0	0	0	DA25	DA24	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16

DDAnL (n = 0 to 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

IR	Specification of DMA transfer destination
0	External memory or on-chip peripheral I/O
1	Internal RAM

DA25 to DA16	Set an address (A25 to A16) of DMA transfer destination (default value is undefined). During DMA transfer, the next DMA transfer destination address is held. When DMA transfer is completed, the DMA transfer source address set first is held.

DA15 to DA0	Set an address (A15 to A0) of DMA transfer destination (default value is undefined). During DMA transfer, the next DMA transfer destination address is held. When DMA transfer is completed, the DMA transfer source address set first is held.

Cautions 1. Be sure to set bits 14 to 10 of the DDAnH register to "0".

2. Set the DDAnH and DDAnL registers at the following timing when DMA transfer is disabled (DCHCn.Enn bit = 0).

- **Period from after reset to start of first DMA transfer**
- **Period from after channel initialization by DCHCn.INITn bit to start of DMA transfer**
- **Period from after completion of DMA transfer (DCHCn.TCn bit = 1) to start of the next DMA transfer**

3. When the value of the DDAn register is read, two 16-bit registers, DDAnH and DDAnL, are read. If reading and updating conflict, a value being updated may be read (see 17.13 Cautions).

4. Following reset, set the DSAnH, DSAnL, DDAnH, DDAnL, and DBCn registers before starting DMA transfer. If these registers are not set, the operation when DMA transfer is started is not guaranteed.

(7) External interrupt falling, rising edge specification register 9H (INTF9H, INTR9H)

The INTF9H and INTR9H registers are 8-bit registers that specify detection of the falling and rising edges of the external interrupt pins (INTP4 to INTP6).

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When the function is changed from the external interrupt function (alternate function) to the port function, an edge may be detected. Therefore, clear the INTF9n and INTR9n bits to 0, and then set the port mode.

After reset: 00H R/W Address: INTF9H FFFFFC13H, INTR9H FFFFFC33H

	15	14	13	12	11	10	9	8
INTF9H	INTF915	INTF914	INTF913	0	0	0	0	0
	INTP6	INTP5	INTP4					
	15	14	13	12	11	10	9	8
INTR9H	INTR915	INTR914	INTR913	0	0	0	0	0
	INTP6	INTP5	INTP4					

Remark For the valid edge specification combinations, see **Table 18-12**.

Table 18-12. Valid Edge Specification

INTF9n	INTR9n	Valid Edge Specification (n = 13 to 15)
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both rising and falling edges

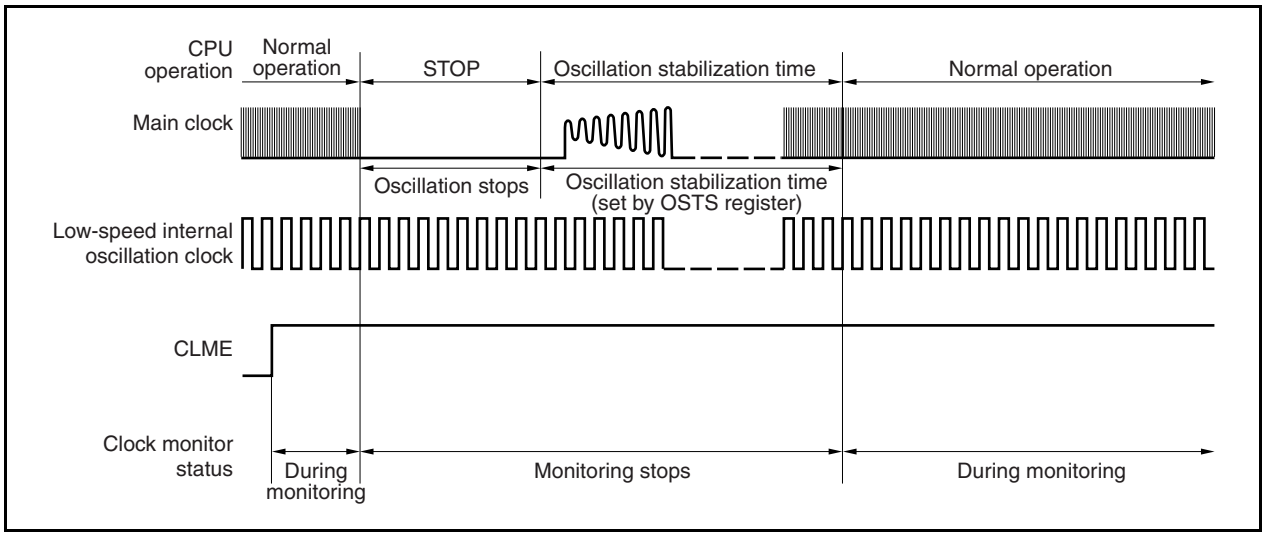
Caution Be sure to set the INTF9n and INTR9n bits to 00 if the corresponding pin is not used as the INTP4 to INTP6 pins.

Remark n = 13 to 15: Control of INTP4 to INTP6 pins

(3) Operation in STOP mode or after STOP mode is released

If the STOP mode is set with the CLM.CLME bit = 1, the monitor operation is stopped in the STOP mode and while the oscillation stabilization time is being counted. After the oscillation stabilization time, the monitor operation is automatically started.

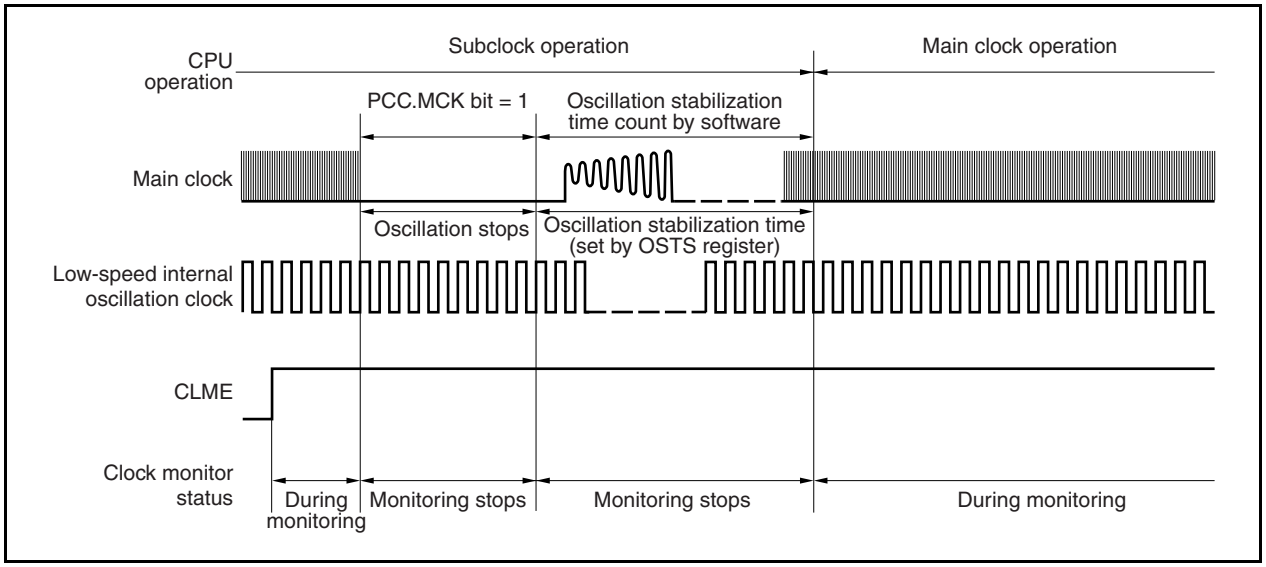
Figure 22-4. Operation in STOP Mode or After STOP Mode Is Released



(4) Operation when main clock is stopped (arbitrary)

During subclock operation (PCC.CLS bit = 1) or when the main clock is stopped by setting the PCC.MCK bit to 1, the monitor operation is stopped until the main clock operation is started (PCC.CLS bit = 0). The monitor operation is automatically started when the main clock operation is started.

Figure 22-5. Operation When Main Clock Is Stopped (Arbitrary)



(5) Operation while CPU is operating on low-speed internal oscillation clock (CCLS.CCLSF bit = 1)

The monitor operation is not started when the CCLSF bit is 1, even if the CLME bit is set to 1.

(6) Operation while CPU is operating on high-speed internal oscillation clock (MCM.MCS bit = 0)

The monitor operation is not started when the MCM.MCS bit is 0, even if the CLM.CLME bit is set to 1.

Table 26-2. Basic Functions

Function	Functional Outline	Support (√: Supported, ×: Not supported)	
		On-Board/Off-Board Programming	On-Board/Off-Board Programming
Blank check	The erasure status of the entire memory is checked.	√	√
Chip erasure	The contents of the entire memory area are erased all at once.	√	×[Note]
Block erasure	The contents of specified memory blocks are erased.	√	√
Program	Writing to specified addresses, and a verify check to see if write level is secured are performed.	√	√
Verify/checksum	Data read from the flash memory is compared with data transferred from the flash programmer.	√	× (Can be read by user program)
Read	Data written to the flash memory is read.	√	×
Security setting	Use of the chip erase command, block erase command, program command, and read command is prohibited, and rewriting of the boot area is prohibited.	√	× (Supported only when setting is changed from enable to disable)

Note Chip erasure can be executed by specifying the entire memory area by using the block erase function.

The following table lists the security functions. The chip erase command prohibit, block erase command prohibit, program command prohibit, read command prohibit, and boot block cluster rewrite prohibit setting functions are enabled by default after shipment, and security can be set by rewriting via on-board/off-board programming. Each security function can be used in combination with the others at the same time.

Table 26-3. Security Functions

Function	Function Outline
Chip erase command prohibit	Execution of block erase and chip erase commands on all the blocks is prohibited. Once prohibition is set, setting of prohibition cannot be initialized because the chip erase command cannot be executed.
Block erase command prohibit	Execution of a block erase command on all blocks is prohibited. Setting of prohibition can be initialized by execution of a chip erase command.
Program command prohibit	Execution of program and block erase commands on all the blocks is prohibited. Setting of prohibition can be initialized by execution of the chip erase command.
Read command prohibit	Execution of a read command on all of the blocks is prohibited. Setting of the prohibition can be initialized by execution of a chip erase command.
Boot block cluster rewrite prohibit setting	Boot block cluster from block 0 to a specified block can be protected. Once a boot block cluster has been protected, it cannot be rewritten (or erased/written) afterward. Even if a chip erase command is executed, the prohibited setting cannot be initialized. The maximum block that can be specified is as follows. μPD70F3747: Block 63 μPD70F3750, 70F3752, 70F3755, 70F3757: Block 127

<R> **29.6.3 Supply current**

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = 3.7 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Normal operation mode[Note 2]	PLL operating	f_{XX} = 32 MHz (f_X = 8 MHz)	All peripheral function operating		39	51	mA
					All peripheral function stopped		32		mA
			PLL operating	f_{XX} = 20 MHz (f_X = 10 MHz)	All peripheral function operating		27	37	mA
					All peripheral function stopped		22		mA
			PLL stopped	f_{XX} = 16 MHz (f_X = 16 MHz)	All peripheral function operating		21	30	mA
					All peripheral function stopped		19		mA
	I_{DD2}	HALT mode[Note 2]	PLL operating	f_{XX} = 32 MHz (f_X = 8 MHz)	All peripheral function operating		24	34	mA
					All peripheral function stopped		18		mA
			PLL operating	f_{XX} = 20 MHz (f_X = 10 MHz)	All peripheral function operating		16	23	mA
					All peripheral function stopped		12		mA
			PLL stopped	f_{XX} = 16 MHz (f_X = 16 MHz)	All peripheral function operating		13	20	mA
					All peripheral function stopped		9		mA
	I_{DD3}	IDLE1 mode	PLL stopped[Note 3]	f_{XX} = 16 MHz (f_X = 16 MHz)	TAA, UARTD operating		2.4	3.6	mA
					All peripheral function stopped		1.6		mA
				f_{XX} = 8 MHz (f_X = 8 MHz)	TAA, UARTD operating		1.6	2.5	mA
					All peripheral function stopped		1.3		mA
			f_{XX} = High-speed internal oscillation (f_{RH})[Note 4]		TAA, UARTD operating		1.5	2.3	mA
					All peripheral function stopped		1.1		mA
	I_{DD4}	IDLE2 mode	PLL stopped[Note 3]	f_{XX} = 16 MHz (f_X = 16 MHz)			0.8	1.2	mA
				f_{XX} = 8 MHz (f_X = 8 MHz)			0.5	0.8	mA
			f_{XX} = High-speed internal oscillation (f_{RH})[Note 4]				0.2	0.5	mA
	I_{DD5}	Subclock operation mode[Notes 4, 5]	Crystal resonator (f_{XT} = 32.768 kHz)				80	400	μA
	I_{DD6}	Sub-IDLE mode[Notes 4, 5]	Crystal resonator (f_{XT} = 32.768 kHz)				20	190	μA
	I_{DD7}	STOP mode[Notes 4, 6]	Low-speed internal oscillator (f_{RL}) operating				18.5	100	μA
			Low-speed internal oscillator (f_{RL}) stopped				10.5	85	μA

Notes 1. Total current of V_{DD} and EV_{DD} (all ports stopped). The current of AV_{REF0} and the port buffer current including the current flowing through the on-chip pull-up/pull-down resistors are not included.

2. During SSCG operation, TYP. value + 2.5 mA, MAX. value + 4 mA

3. High-speed internal oscillator (f_{RH}) stopped.

4. When the main clock oscillator (f_{XX}) is stopped.

5. Low-speed internal oscillator (f_{RL}) operating, high-speed internal oscillator (f_{RH}) stopped.

6. When the subclock oscillator (f_{XT}) is not used.

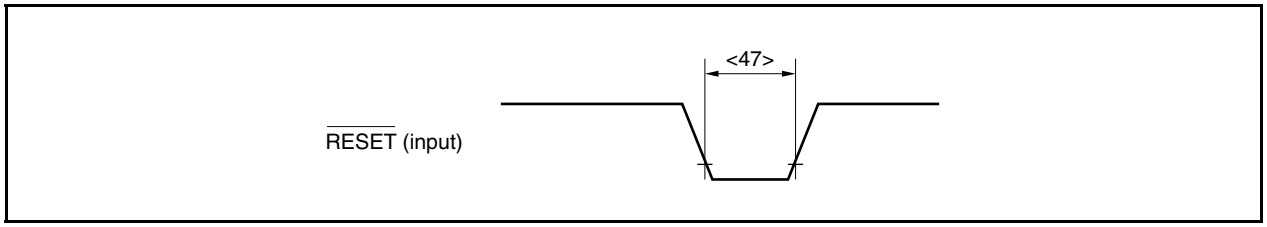
30.8 Basic Operation

(1) Reset timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = 3.3 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL}	<47>		250		ns

Reset



(2) Interrupt timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = 3.7 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

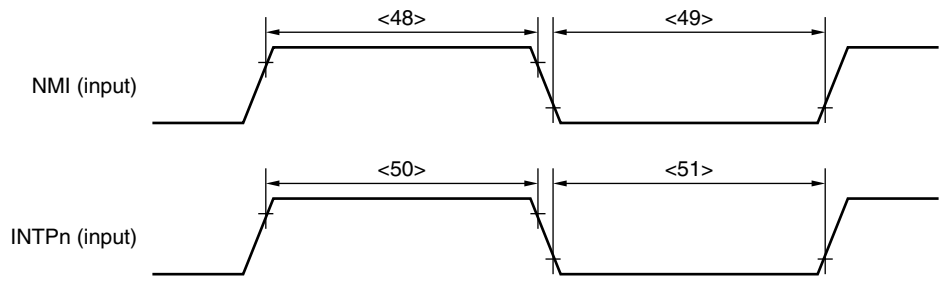
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	t_{WNIH}	<48>	Analog noise elimination	250		ns
NMI low-level width	t_{WNIL}	<49>	Analog noise elimination	250		ns
INTPn[Note 1] high-level width	t_{WITH}	<50>	Analog noise elimination (n = 0 to 7)	250		ns
			Digital noise elimination (n = 3)	**Note 2**		ns
INTPn[Note 1] low-level width	t_{WITL}	<51>	Analog noise elimination (n = 0 to 7)	250		ns
			Digital noise elimination (n = 3)	**Note 2**		ns

Notes 1. The same value as the INTP0/P03 pin applies in the case of the ADTRG pin. The same value as the INTP2/P05 pin applies in the case of the $\overline{\text{DRST}}$ pin.

2. $2T_{samp} + 20$ or $3T_{samp} + 20$

T_{samp}: Sampling clock for noise elimination

Reset/interrupt



Remark n = 0 to 7

(3/12)

Symbol	Name	Unit	Page
CB2RXL	CSIB2 receive data register L	CSI	674
CB2STR	CSIB2 status register	CSI	681
CB2TIC	Interrupt control register	INTC	841
CB2TX	CSIB2 transmit data register	CSI	674
CB2TXL	CSIB2 transmit data register L	CSI	674
CCLS	CPU operation clock status register	CG	271
CLM	Clock monitor mode register	CLM	902
DADC0	DMA addressing control register 0	DMA	799
DADC1	DMA addressing control register 1	DMA	799
DADC2	DMA addressing control register 2	DMA	799
DADC3	DMA addressing control register 3	DMA	799
DBC0	DMA transfer count register 0	DMA	798
DBC1	DMA transfer count register 1	DMA	798
DBC2	DMA transfer count register 2	DMA	798
DBC3	DMA transfer count register 3	DMA	798
DCHC0	DMA channel control register 0	DMA	800
DCHC1	DMA channel control register 1	DMA	800
DCHC2	DMA channel control register 2	DMA	800
DCHC3	DMA channel control register 3	DMA	800
DDA0H	DMA destination address register 0H	DMA	797
DDA0L	DMA destination address register 0L	DMA	797
DDA1H	DMA destination address register 1H	DMA	797
DDA1L	DMA destination address register 1L	DMA	797
DDA2H	DMA destination address register 2H	DMA	797
DDA2L	DMA destination address register 2L	DMA	797
DDA3H	DMA destination address register 3H	DMA	797
DDA3L	DMA destination address register 3L	DMA	797
DMAIC0	Interrupt control register	INTC	841
DMAIC1	Interrupt control register	INTC	841
DMAIC2	Interrupt control register	INTC	841
DMAIC3	Interrupt control register	INTC	841
DSA0H	DMA source address register 0H	DMA	796
DSA0L	DMA source address register 0L	DMA	796
DSA1H	DMA source address register 1H	DMA	796
DSA1L	DMA source address register 1L	DMA	796
DSA2H	DMA source address register 2H	DMA	796
DSA2L	DMA source address register 2L	DMA	796
DSA3H	DMA source address register 3H	DMA	796
DSA3L	DMA source address register 3L	DMA	796
DTFR0	DMA trigger factor register 0	DMA	801
DTFR1	DMA trigger factor register 1	DMA	801
DTFR2	DMA trigger factor register 2	DMA	801
DTFR3	DMA trigger factor register 3	DMA	801
DWC0	Data wait control register 0	BCU	250