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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	128
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3757gj-gae-ax

PREFACE

Readers This manual is intended for users who wish to understand the functions of the V850ES/Hx3 and design application systems using the V850ES/Hx3.

Purpose This manual is intended to give users an understanding of the hardware functions of the V850ES/Hx3 shown in the **Organization** below.

Organization This manual is divided into two parts: Hardware (this manual) and Architecture (**V850ES Architecture User's Manual**).

Hardware	Architecture
• Pin functions	• Data types
• CPU function	• Register set
• On-chip peripheral functions	• Instruction format and instruction set
• Flash memory programming	• Interrupts and exceptions
• Electrical specifications	• Pipeline operation

How to Read This Manual It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To understand the overall functions of the V850ES/Hx3
→Read this manual according to the **CONTENTS**.

To find the details of a register where the name is known
→Use **APPENDIX B REGISTER INDEX**.

To understand the details of an instruction function
→Refer to the **V850ES Architecture User's Manual** available separately.

To know the electrical specifications of the V850ES/HE3
→See **CHAPTER 29 ELECTRICAL SPECIFICATIONS (V850ES/HE3)**.

To know the electrical specifications of the V850ES/HF3
→See **CHAPTER 30 ELECTRICAL SPECIFICATIONS (V850ES/HF3)**.

To know the electrical specifications of the V850ES/HG3
→See **CHAPTER 31 ELECTRICAL SPECIFICATIONS (V850ES/HG3)**.

To know the electrical specifications of the V850ES/HJ3
→See **CHAPTER 32 ELECTRICAL SPECIFICATIONS (V850ES/HJ3)**.

4.3.4 Port 4

Port 4 I/O settings can be controlled in 1-bit units.

Each product has the same number of I/O ports, but the alternate functions of the pins differ.

Generic Name	Number of I/O Ports
V850ES/HE3	3-bit I/O port
V850ES/HF3	3-bit I/O port
V850ES/HG3	3-bit I/O port
V850ES/HJ3	3-bit I/O port

Table 4-13. Alternate-Function Pins of Port 4

Function Name	Alternate-Function Name		Pin No.				Remark	Block Type
	Name	I/O	HE3	HF3	HG3	HJ3		
P40	SIB0/KR0	Input	19	19	22	22Note 1	–	E11-U
	SIB0/KR0/RXDD3/INTP14	Input	–	–	–	22Note 2		F113x-UI
P41	SOB0/KR1	I/O	20	20	23	23Note 1		E01-U
	SOB0/KR1/TXDD3	I/O	–	–	–	23Note 2		F010x-U
P42	$\overline{\text{SCKB0}}$/KR2	I/O	21	21	24	24		E21-U

Notes 1. μPD70F3755 only

2. μPD70F3757 only

Caution The P40 to P42 pins have hysteresis characteristics in the input mode of the alternate function, but do not have hysteresis characteristics in the port mode.

(1) Port register 4 (P4)

After reset: 00H (output latch) R/W Address: FFFFF408H

	7	6	5	4	3	2	1	0
P4	0	0	0	0	0	P42	P41	P40

P4n	Output data control (in output mode) (n = 0 to 2)
0	Outputs 0
1	Outputs 1

(3) Port mode control register DL (PMCDL) (V850ES/HJ3 only)

After reset: FFFFH R/W Address: PMCDL FFFFF044H,
PMCDLL FFFFF044H, PMCDLH FFFFF045H

	15	14	13	12	11	10	9	8
PMCDL (PMCDLH)	PMCDL15	PMCDL14	PMCDL13	PMCDL12	PMCDL11	PMCDL10	PMCDL9	PMCDL8

	7	6	5	4	3	2	1	0
(PMCDLL)	PMCDL7	PMCDL6	PMCDL5	PMCDL4	PMCDL3	PMCDL2	PMCDL1	PMCDL0

PMCDLn	Specification of PDLn pin operation mode (n = 0 to 15)
0	I/O port
1	ADn I/O (address/data bus I/O)

Remarks 1. The PMCDL register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PMCDL register as the PMCDLH register and the lower 8 bits as the PMCDLL register, PMCDL can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PMCDL register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PMCDLH register.

(2) Internal oscillation mode register (RCM)

The RCM register is an 8-bit register that sets the operation mode of the internal oscillator.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 80H.

After reset: 80H R/W Address: FFFFF80CH

	7	6	5	4	3	2	<1>	<0>
RCM	RSTS[Note]	0	0	0	0	0	HRSTOP	RSTOP

RSTS[Note]	Status of high-speed internal oscillator
0	High-speed internal oscillator (f_{RH}: 8 MHz) stops or waits for oscillation stabilization
1	High-speed internal oscillator (f_{RH}: 8 MHz) oscillates

HRSTOP	Oscillation/stop of high-speed internal oscillator
0	High-speed internal oscillator (f_{RH}: 8 MHz) oscillates
1	High-speed internal oscillator (f_{RH}: 8 MHz) stopped

RSTOP	Oscillation/stop of low-speed internal oscillator
0	Low-speed internal oscillator (f_{RL}: 240 kHz) oscillates
1	Low-speed internal oscillator (f_{RL}: 240 kHz) stops

Note The RSTS bit is a read-only bit.

Cautions

1. The high-speed internal oscillator (f_{RH}) cannot be stopped while the CPU is operating with the high-speed internal oscillation clock (f_{RH}) (MCM.MCM0 bit = 1). Do not set the HRSTOP bit to 1.

2. The low-speed internal oscillator (f_{RL}) cannot be stopped while the CPU is operating with the low-speed internal oscillation clock (f_{RL}) (CCLS.CCLSF bit = 1). Do not set the RSTOP bit to 1.

3. The low-speed internal oscillator (f_{RL}) oscillates if the CCLS.CCLSF bit is set to 1 (when WDT overflow occurs during oscillation stabilization time) even when the RSTOP bit is set to 1. At this time, the RSTOP bit remains being set to 1.

7.5.8 Timer output operations

The following table shows the operations and output levels of the TOAAn0 and TOAAn1 pins.

Table 7-4. Timer Output Control in Each Mode

Operation Mode	TOAAn1 Pin	TOAAn0 Pin
Interval timer mode	Square wave output	
External event count mode	–	
External trigger pulse output mode	External trigger pulse output	Square wave output
One-shot pulse output mode	One-shot pulse output	
PWM output mode	PWM output	
Free-running timer mode	Square wave output (only when compare function is used)	
Pulse width measurement mode	–	

Remark n = 0 to 4

Table 7-5. Truth Table of TOAAn0 and TOAAn1 Pins Under Control of Timer Output Control Bits

TAAnIOC0.TAAnOLm Bit	TAAnIOC0.TAAnOEm Bit	TAAnCTL0.TAAnCE Bit	Level of TOAAnm Pin
0	0	×	Low-level output
	1	0	Low-level output
		1	Low level immediately before counting, high level after counting is started
1	0	×	High-level output
	1	0	High-level output
		1	High level immediately before counting, low level after counting is started

Remark n = 0 to 4
m = 0, 1

If the set value of the TABnCCRk register is greater than the set value of the TABnCCR0 register, the count value of the 16-bit counter does not match the value of the TABnCCRk register. Consequently, the INTTABnCCk signal is not generated, nor is the output of the TOABnk pin changed.

Remark k = 1 to 3

Figure 8-8. Timing Chart When D_{01} < D_{k1}

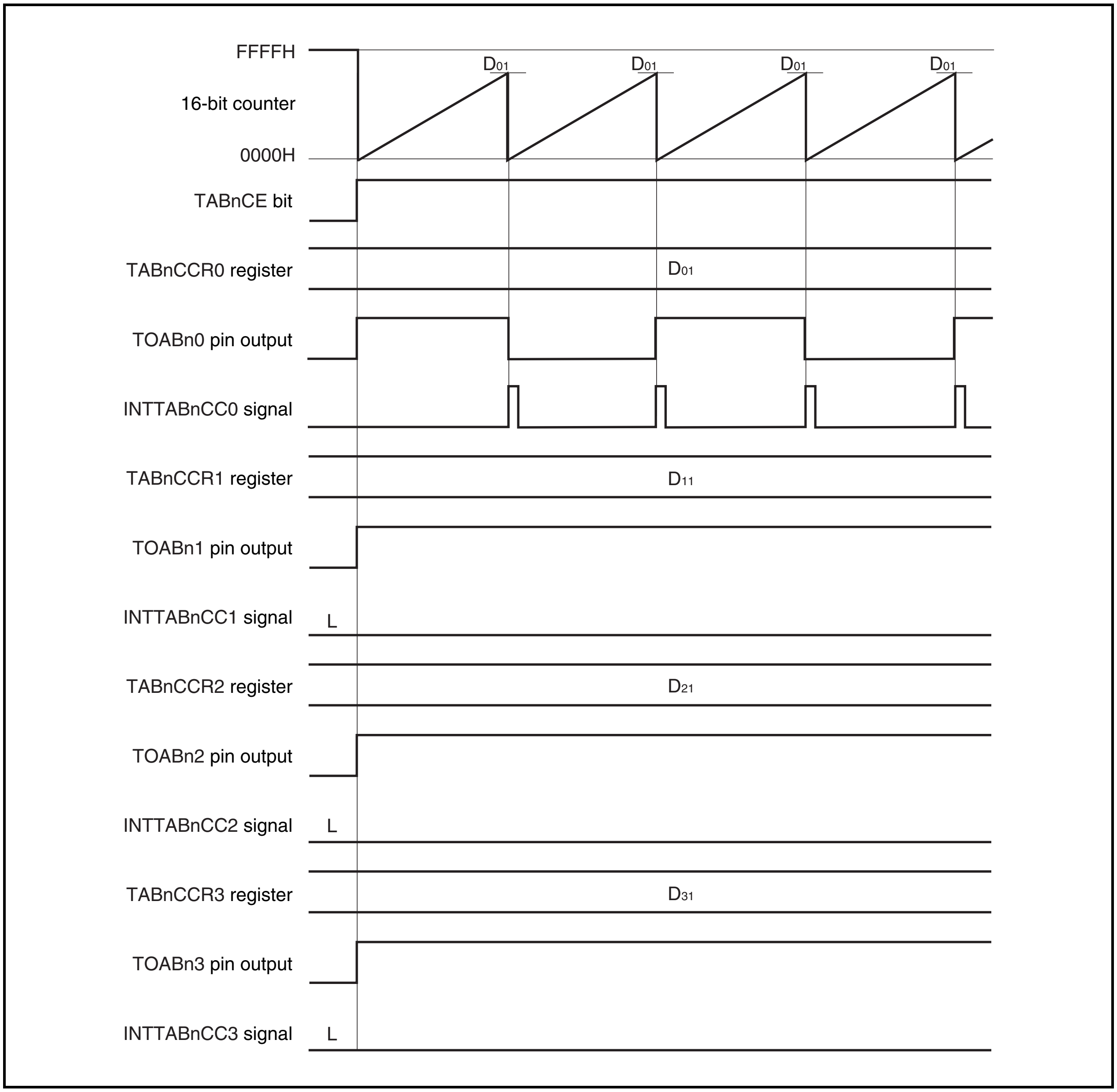


Figure 8-11. Register Setting for Operation in External Event Count Mode (2/2)

(f) TABn capture/compare register 0 (TABnCCR0)

If D_0 is set to the TABnCCR0 register, the counter is cleared and a compare match interrupt request signal (INTTABnCC0) is generated when the number of external event counts reaches (D_0 + 1).

(g) TABn capture/compare registers 1 to 3 (TABnCCR1 to TABnCCR3)

Usually, the TABnCCR1 to TABnCCR3 registers are not used in the external event count mode. However, the set value of the TABnCCR1 to TABnCCR3 registers are transferred to the CCR1 to CCR3 buffer registers. When the count value of the 16-bit counter matches the value of the CCR1 to CCR3 buffer registers, compare match interrupt request signals (INTTABnCC1 to INTTABnCC3) are generated.

Therefore, mask the interrupt signal by using the interrupt mask flags (TABnCCMK1 to TABnCCMK3).

Caution When an external clock is used as the count clock, the external clock can be input only from the TIABn0 pin. At this time, set the TABnIOC1.TABnIS1 and TABnIOC1.TABnIS0 bits to 00 (capture trigger input (TIABn0 pin): no edge detection).

Remark The TABn I/O control register 1 (TABnIOC1) and TABn option register 0 (TABnOPT0) are not used in the external event count mode.

To transfer data from the TABnCCRm register to the CCRm buffer register, the TABnCCR1 register must be written.

To change both the cycle and active level of the PWM waveform at this time, first set the cycle to the TABnCCR0 register, set the active level width to the TABnCCR2 and TABnCCR3 registers, and then set an active level width to the TABnCCR1 register.

To change only the active level width (duty factor) of PWM wave, first set the active level to the TABnCCR2 and TABnCCR3 registers, and then set an active level to the TABnCCR1 register.

To change only the active level width (duty factor) of the PWM waveform output by the TOABn1 pin, only the TABnCCR1 register has to be set.

To change only the active level width (duty factor) of the PWM waveform output by the TOABn2 and TOABn3 pins, first set an active level width to the TABnCCR2 and TABnCCR3 registers, and then write the same value to the TABnCCR1 register.

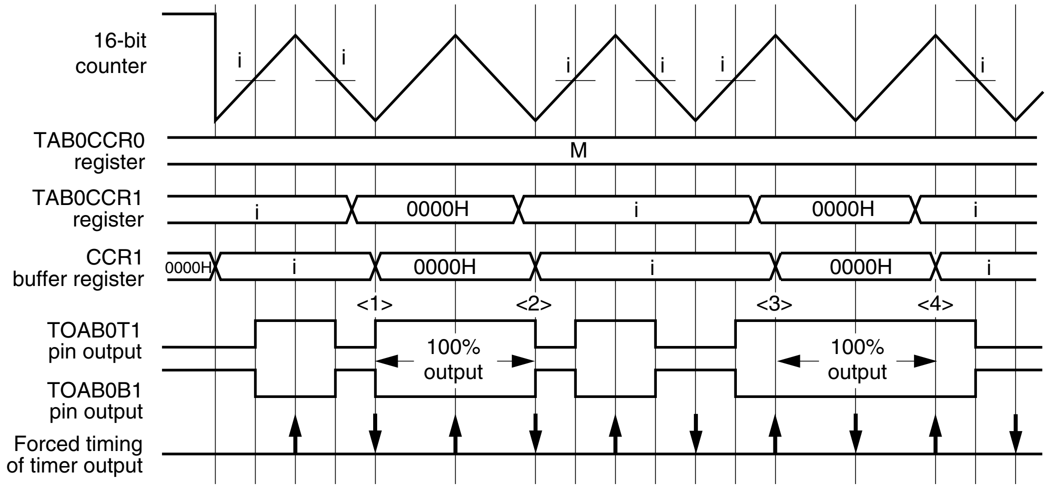
After the TABnCCR1 register is written, the value written to the TABnCCRm register is transferred to the CCRm buffer register in synchronization with the timing of clearing the 16-bit counter, and is used as a value to be compared with the value of the 16-bit counter.

To change only the cycle of the PWM waveform, first set a cycle to the TABnCCR0 register, and then write the same value to the TABnCCR1 register.

To write the TABnCCR0 to TABnCCR3 registers again after writing the TABnCCR1 register once, do so after the INTTABnCC0 signal is generated. Otherwise, the value of the CCRm buffer register may become undefined because the timing of transferring data from the TABnCCRm register to the CCRm buffer register conflicts with writing the TABnCCRm register.

Remark m = 0 to 3

Figure 10-10. 100% PWM Output Waveform (Without Dead Time)



<1> 100% output is selected by the valley interrupt (with a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output, but raising the timer output takes precedence when the value of the TAB0CCRm register matches the value of the 16-bit counter. As a result, the 100% output is produced.

<2> 100% output is canceled by the valley interrupt (without a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output. This cancels the 100% output.

<3> 100% output is selected by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This produces the 100% output.

<4> 100% output is canceled by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This cancels the 100% output.

Remark ↑ means forced raising and ↓ means forced lowering.

(3) Watch timer operation mode register (WTM)

The WTM register enables or disables the count clock and operation of the watch timer, sets the interval time of the prescaler, controls the operation of the 5-bit counter, and sets the set time of the watch flag.

Set the PRSM0 register before setting the WTM register.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

(1/2)

After reset: 00H R/W Address: FFFFF680H

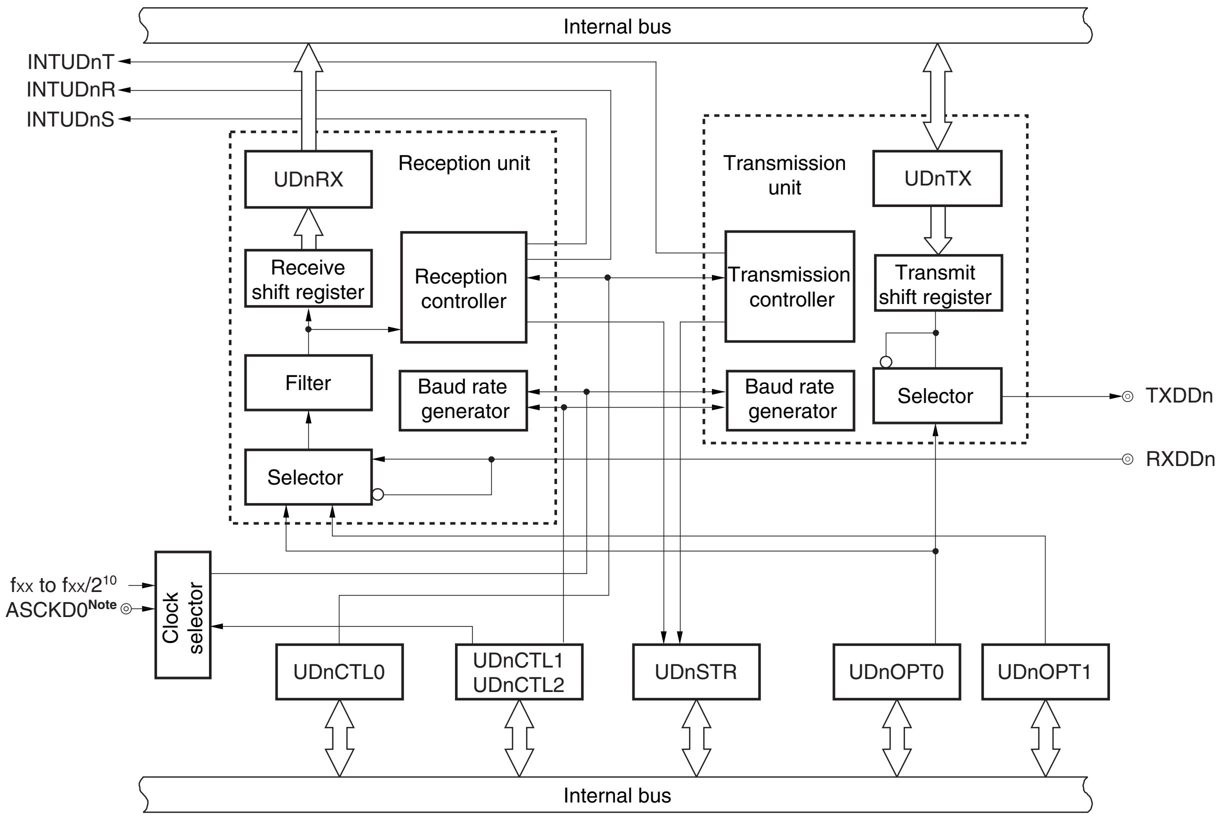
	7	6	5	4	3	2	1	0
WTM	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM7	WTM6	WTM5	WTM4	Selection of interval time of prescaler
0	0	0	0	$2^4/f_W$ (488 μs: $f_W = f_{XT}$)
0	0	0	1	$2^5/f_W$ (977 μs: $f_W = f_{XT}$)
0	0	1	0	$2^6/f_W$ (1.95 ms: $f_W = f_{XT}$)
0	0	1	1	$2^7/f_W$ (3.91 ms: $f_W = f_{XT}$)
0	1	0	0	$2^8/f_W$ (7.81 ms: $f_W = f_{XT}$)
0	1	0	1	$2^9/f_W$ (15.6 ms: $f_W = f_{XT}$)
0	1	1	0	$2^{10}/f_W$ (31.3 ms: $f_W = f_{XT}$)
0	1	1	1	$2^{11}/f_W$ (62.5 ms: $f_W = f_{XT}$)
1	0	0	0	$2^4/f_W$ (488 μs: $f_W = f_{BRG}$)
1	0	0	1	$2^5/f_W$ (977 μs: $f_W = f_{BRG}$)
1	0	1	0	$2^6/f_W$ (1.95 ms: $f_W = f_{BRG}$)
1	0	1	1	$2^7/f_W$ (3.90 ms: $f_W = f_{BRG}$)
1	1	0	0	$2^8/f_W$ (7.81 ms: $f_W = f_{BRG}$)
1	1	0	1	$2^9/f_W$ (15.6 ms: $f_W = f_{BRG}$)
1	1	1	0	$2^{10}/f_W$ (31.2 ms: $f_W = f_{BRG}$)
1	1	1	1	$2^{11}/f_W$ (62.5 ms: $f_W = f_{BRG}$)

14.2 Configuration

The block diagram of the UARTDn is shown below.

Figure 14-1. Block Diagram of Asynchronous Serial Interface Dn



Note UARTD0 only

Remark For the configuration of the baud rate generator, see **Figure 14-32**.

UARTDn includes the following hardware units.

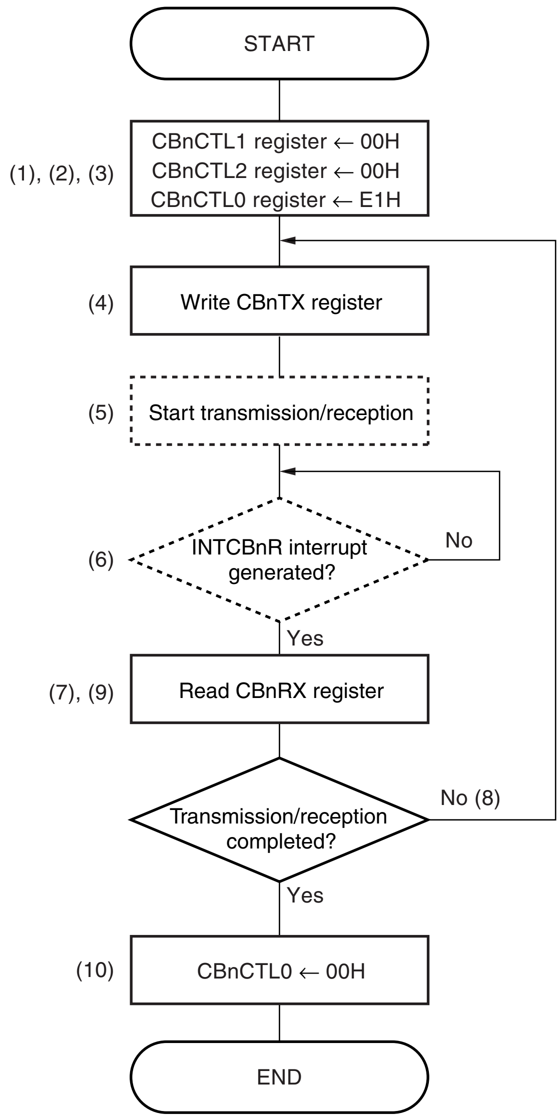
Table 14-2. Configuration of UARTDn

Item	Configuration
Registers	UARTDn control register 0 (UDnCTL0) UARTDn control register 1 (UDnCTL1) UARTDn control register 2 (UDnCTL2) UARTDn option control register 0 (UDnOPT0) UARTDn option control register 1 (UDnOPT1) UARTDn status register (UDnSTR) UARTDn receive shift register UARTDn receive data register (UDnRX) UARTDn transmit shift register UARTDn transmit data register (UDnTX)

15.6.3 Single transfer mode (master mode, transmission/reception mode)

MSB first (CBnCTL0.CBnDIR bit = 0), communication type 1 (CBnCTL1.CBnCKP and CBnCTL1.CBnDAP bits = 00), communication clock (f_{CCLK}) = f_{XX}/2 (CBnCTL1.CBnCKS2 to CBnCTL1.CBnCKS0 bits = 000), transfer data length = 8 bits (CBnCTL2.CBnCL3 to CBnCTL2.CBnCL0 bits = 0000)

(1) Operation flow



Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **(2) Operation timing**.

15.8.1 Baud rate generation

The transmission/reception clock is generated by dividing the main clock. The baud rate generated from the main clock is obtained by the following equation.

$$f_{BRG} = \frac{f_{XX}}{2^{k+1} \times N}$$

Caution Set so that the f_{BRG} is 8 MHz or less.

Remark f_{BRG}: BRG count clock
f_{XX}: Main clock oscillation frequency
k: PRSM0 register setting value = 0 to 3
N: PRSCM0 register setting value = 1 to 256
However, N = 256 only when PRSCM0 register is set to 00H.

15.9 Cautions

(1) When transferring transmit data and receive data using DMA transfer, error processing cannot be performed even if an overrun error occurs during serial transfer. Check that the no overrun error has occurred by reading the CBnSTR.CBnOVE bit after DMA transfer has been completed.

(2) In regards to registers that are forbidden from being rewritten during operations (CBnCTL0.CBnPWR bit is 1), if rewriting has been carried out by mistake during operations, set the CBnCTL0.CBnPWR bit to 0 once, then initialize CSIBn.
Registers to which rewriting during operation are prohibited are shown below.
- CBnCTL0 register: CBnTXE, CBnRXE, CBnDIR, CBnTMS bits
- CBnCTL1 register: CBnCKP, CBnDAP, CBnCKS2 to CBnCKS0 bits
- CBnCTL2 register: CBnCL3 to CBnCL0 bits

(3) In communication type 2 and 4 (CBnCTL1.CBnDAP bit = 1), the CBnSTR.CBnTSF bit is cleared half a $\overline{\text{SCKBn}}$ clock after occurrence of a reception complete interrupt (INTCBnR).
In the single transfer mode, writing the next transmit data is ignored during communication (CBnTSF bit = 1), and the next communication is not started. Also if reception-only communication (CBnCTL0.CBnTXE bit = 0, CBnCTL0.CBnRXE bit = 1) is set, the next communication is not started even if the receive data is read during communication (CBnTSF bit = 1).
Therefore, when using the single transfer mode with communication type 2 or 4 (CBnDAP bit = 1), pay particular attention to the following.

- To start the next transmission, confirm that CBnTSF bit = 0 and then write the transmit data to the CBnTX register.
- To perform the next reception continuously when reception-only communication (CBnTXE bit = 0, CBnRXE bit = 1) is set, confirm that CBnTSF bit = 0 and then read the CBnRX register.

Or, use the continuous transfer mode instead of the single transfer mode. Use of the continuous transfer mode is recommended especially for using DMA.

(2) When arbitration loss occurs during transmission of extension code

<1> When WTIM0 bit = 0

ST	AD6 to AD0	R/W̄	ACK̄	D7 to D0	ACK̄	D7 to D0	ACK̄	SP

▲1 ▲2 ▲3 Δ4

▲1: IICS0 register = 0110X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 0010X000B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1

ST	AD6 to AD0	R/W̄	ACK̄	D7 to D0	ACK̄	D7 to D0	ACK̄	SP

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0110X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010X100B

▲4: IICS0 register = 0010XX00B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(7) External interrupt falling, rising edge specification register 9H (INTF9H, INTR9H)

The INTF9H and INTR9H registers are 8-bit registers that specify detection of the falling and rising edges of the external interrupt pins (INTP4 to INTP6).

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When the function is changed from the external interrupt function (alternate function) to the port function, an edge may be detected. Therefore, clear the INTF9n and INTR9n bits to 0, and then set the port mode.

After reset: 00H R/W Address: INTF9H FFFFFC13H, INTR9H FFFFFC33H

	15	14	13	12	11	10	9	8
INTF9H	INTF915	INTF914	INTF913	0	0	0	0	0
	INTP6	INTP5	INTP4					

	15	14	13	12	11	10	9	8
INTR9H	INTR915	INTR914	INTR913	0	0	0	0	0
	INTP6	INTP5	INTP4					

Remark For the valid edge specification combinations, see **Table 18-12**.

Table 18-12. Valid Edge Specification

INTF9n	INTR9n	Valid Edge Specification (n = 13 to 15)
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both rising and falling edges

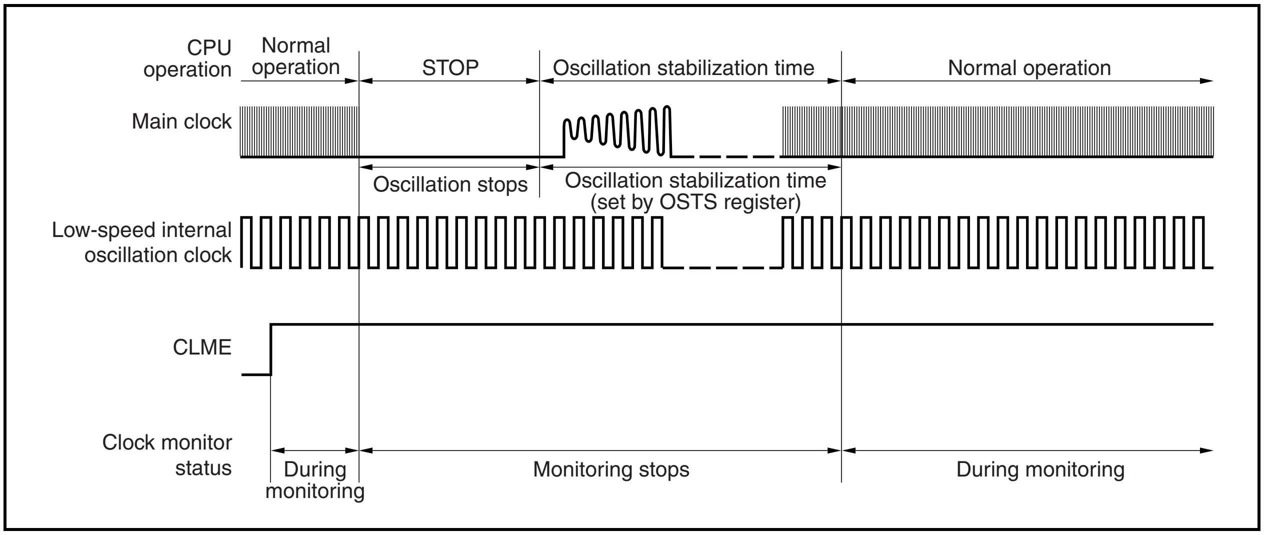
Caution Be sure to set the INTF9n and INTR9n bits to 00 if the corresponding pin is not used as the INTP4 to INTP6 pins.

Remark n = 13 to 15: Control of INTP4 to INTP6 pins

(3) Operation in STOP mode or after STOP mode is released

If the STOP mode is set with the CLM.CLME bit = 1, the monitor operation is stopped in the STOP mode and while the oscillation stabilization time is being counted. After the oscillation stabilization time, the monitor operation is automatically started.

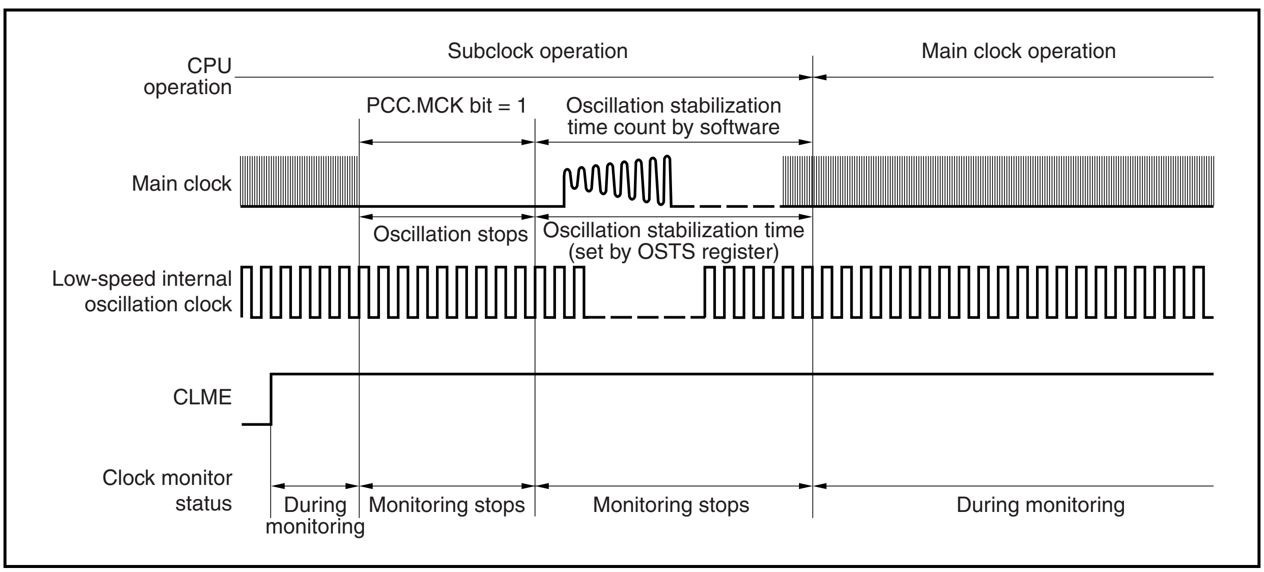
Figure 22-4. Operation in STOP Mode or After STOP Mode Is Released



(4) Operation when main clock is stopped (arbitrary)

During subclock operation (PCC.CLS bit = 1) or when the main clock is stopped by setting the PCC.MCK bit to 1, the monitor operation is stopped until the main clock operation is started (PCC.CLS bit = 0). The monitor operation is automatically started when the main clock operation is started.

Figure 22-5. Operation When Main Clock Is Stopped (Arbitrary)



(5) Operation while CPU is operating on low-speed internal oscillation clock (CCLS.CCLSF bit = 1)

The monitor operation is not started when the CCLSF bit is 1, even if the CLME bit is set to 1.

(6) Operation while CPU is operating on high-speed internal oscillation clock (MCM.MCS bit = 0)

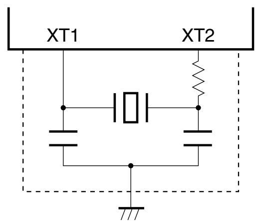
The monitor operation is not started when the MCM.MCS bit is 0, even if the CLM.CLME bit is set to 1.

Table 28-3. Wiring Between V850ES/Hx3 and MINICUBE2

Pin Configuration of MINICUBE2 (QB-MINI2)			With CSIB0-HS	With UARTD0
Signal Name	I/O	Pin Function	Pin Name	Pin Name
SI/RxD	Input	Pin to receive commands and data from V850ES/Hx3	P41/SOB0	P30/TXDD0
SO/TxD	Output	Pin to transmit commands and data to V850ES/Hx3	P40/SIB0	P31/RXDD0
SCK	Output	Clock output pin for 3-wire serial communication	P42/$\overline{\text{SCKB0}}$	Not needed
CLK	Output	Not used	Not needed	Not needed
RESET_OUT	Output	Reset output pin to V850ES/Hx3	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
FLMD0	Output	Output pin to set V850ES/Hx3 to debug mode or programming mode	FLMD0	FLMD0
FLMD1	Output	Output pin to set programming mode	PDL5/FLMD1	PDL5/FLMD1
HS	Input	Handshake signal for CSI0 + HS communication	PCM0/$\overline{\text{WAIT}}$	Not needed
GND	–	Ground	V_{SS}	V_{SS}
			AV_{SS}	AV_{SS}
			EV_{SS}	EV_{SS}
			BV_{SS}	BV_{SS}
RESET_IN	Input	Reset input pin on the target system		

29.4.2 Subclock oscillator characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = 3.3 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2				10	s

Notes 1. Indicates only oscillator characteristics. For the CPU operation clock, see **29.7 AC Characteristics**.

2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.3 V) to when the oscillation stabilizes.

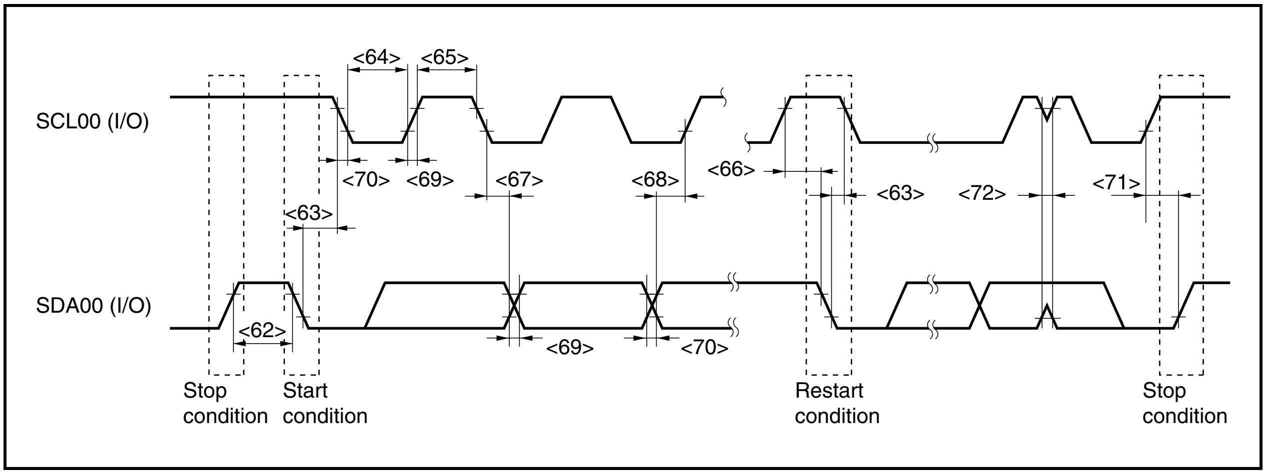
Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

3. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

I²C bus mode



(8) A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = BV_{DD} = 3.7 V to 5.5 V, 4.0 V ≤ AV_{REF0} ≤ 5.5 V, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error Note 1		4.0 ≤ AV_{REF0} ≤ 5.5 V		±0.15	±0.3	%FSR
Conversion time	t_{CONV}		3.1		16	μs
Stabilization time	t_{STA}	After ADA0M0.ADA0PS bit changes from 0 to 1	2			μs
Power down recovery time	t_{DPU}	Starting operation after STOP mode is released	1			μs
Zero scale error Note 1	ZSE				±0.3	%FSR
Full scale error Note 1	FSE				±0.3	%FSR
Non-linearity error Note 2	INL				±2.5	LSB
Differential linearity error Note 2	DNL				±1.5	LSB
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
AV_{REF0} current	I_{AREF0}	When using A/D converter		4	7	mA
		When not using A/D converter		1	10	μA

Notes 1. Excluding quantization error (±0.05 %FSR). Indicates the ratio to the full-scale value (%FSR).

2. Quantization error (±0.5LSB)

Remark FSR: Full Scale Range

(3/12)

Symbol	Name	Unit	Page
CB2RXL	CSIB2 receive data register L	CSI	674
CB2STR	CSIB2 status register	CSI	681
CB2TIC	Interrupt control register	INTC	841
CB2TX	CSIB2 transmit data register	CSI	674
CB2TXL	CSIB2 transmit data register L	CSI	674
CCLS	CPU operation clock status register	CG	271
CLM	Clock monitor mode register	CLM	902
DADC0	DMA addressing control register 0	DMA	799
DADC1	DMA addressing control register 1	DMA	799
DADC2	DMA addressing control register 2	DMA	799
DADC3	DMA addressing control register 3	DMA	799
DBC0	DMA transfer count register 0	DMA	798
DBC1	DMA transfer count register 1	DMA	798
DBC2	DMA transfer count register 2	DMA	798
DBC3	DMA transfer count register 3	DMA	798
DCHC0	DMA channel control register 0	DMA	800
DCHC1	DMA channel control register 1	DMA	800
DCHC2	DMA channel control register 2	DMA	800
DCHC3	DMA channel control register 3	DMA	800
DDA0H	DMA destination address register 0H	DMA	797
DDA0L	DMA destination address register 0L	DMA	797
DDA1H	DMA destination address register 1H	DMA	797
DDA1L	DMA destination address register 1L	DMA	797
DDA2H	DMA destination address register 2H	DMA	797
DDA2L	DMA destination address register 2L	DMA	797
DDA3H	DMA destination address register 3H	DMA	797
DDA3L	DMA destination address register 3L	DMA	797
DMAIC0	Interrupt control register	INTC	841
DMAIC1	Interrupt control register	INTC	841
DMAIC2	Interrupt control register	INTC	841
DMAIC3	Interrupt control register	INTC	841
DSA0H	DMA source address register 0H	DMA	796
DSA0L	DMA source address register 0L	DMA	796
DSA1H	DMA source address register 1H	DMA	796
DSA1L	DMA source address register 1L	DMA	796
DSA2H	DMA source address register 2H	DMA	796
DSA2L	DMA source address register 2L	DMA	796
DSA3H	DMA source address register 3H	DMA	796
DSA3L	DMA source address register 3L	DMA	796
DTFR0	DMA trigger factor register 0	DMA	801
DTFR1	DMA trigger factor register 1	DMA	801
DTFR2	DMA trigger factor register 2	DMA	801
DTFR3	DMA trigger factor register 3	DMA	801
DWC0	Data wait control register 0	BCU	250