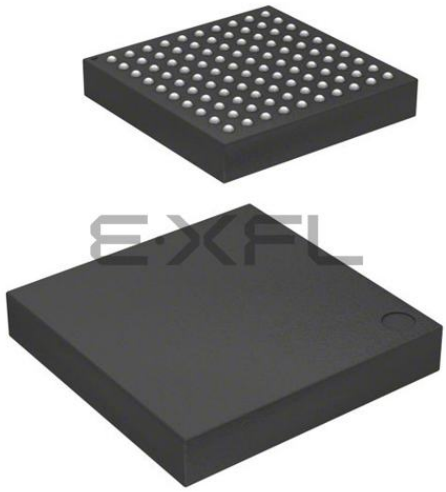

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 78 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 22x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFLGA |
| Supplier Device Package | 100-TFLGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56514bdlj-20 |

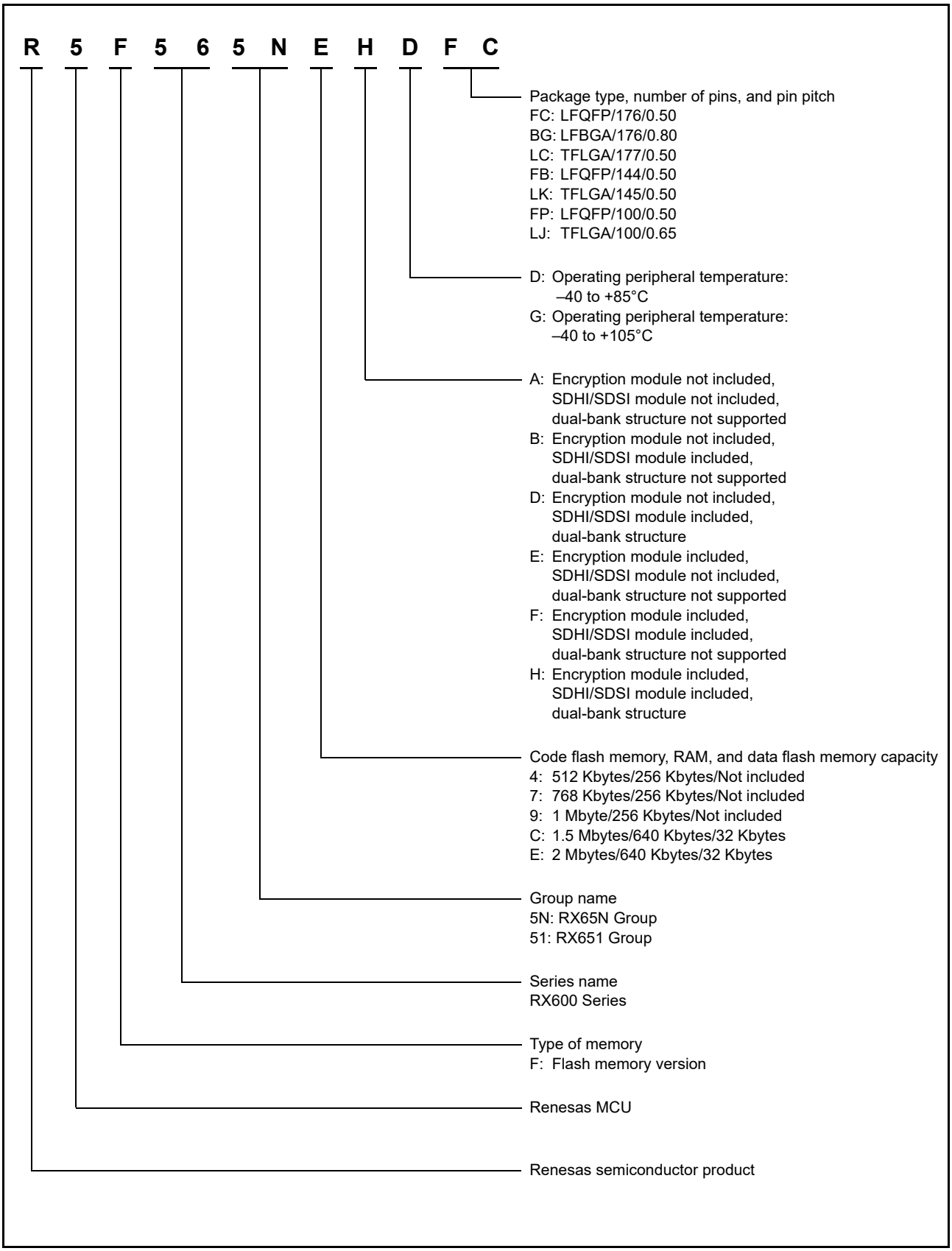



**Figure 1.1 How to Read the Product Part Number**

**Table 1.4 Pin Functions (4/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial communications interface (SCIh) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | RXD12 | Input | Input pin for received data |
| | TXD12 | Output | Output pin for transmitted data |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL12 | I/O | Input/output pin for the $I^2C$ clock |
| | SSDA12 | I/O | Input/output pin for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | SMISO12 | I/O | Input/output pin for slave transmission of data |
| | SMOSI12 | I/O | Input/output pin for master transmission of data |
| | SS12# | Input | Chip-select input pin |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for received data |
| | TXDX12 | Output | Output pin for transmitted data |
| | SIOX12 | I/O | Input/output pin for received or transmitted data |
| Serial communications interface (SCIi) | • Asynchronous mode/clock synchronous mode | | |
| | SCK10 and SCK11 | I/O | Input/output pin for the clock |
| | RXD10 and RXD11 | Input | Input pin for received data |
| | TXD10 and TXD11 | Output | Output pin for transmitted data |
| | CTS10# and CTS11# | Input | Input pin for controlling the start of transmission and reception |
| | RTS10# and RTS11# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL10 and SSCL11 | I/O | Input/output pin for the $I^2C$ clock |
| | SSDA10 and SSDA11 | I/O | Input/output pin for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK10 and SCK11 | I/O | Input/output pin for the clock |
| | SMISO10 and SMISO11 | I/O | Input/output pin for slave transmission of data |
| | SMOSI10 and SMOSI11 | I/O | Input/output pin for master transmission of data |
| | SS10# and SS11# | Input | Chip-select input pin |
| $I^2C$ bus interface | SCL0[FM+], SCL1, SCL2, SCL2-DS | I/O | Input/output pins for clocks. Bus can be directly driven by the N-channel open drain |
| | SDA0[FM+], SDA1, SDA2, SDA2-DS | I/O | Input/output pins for data. Bus can be directly driven by the N-channel open drain |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| H13 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | ET0_MDIO/ RXD5/SMISO5/ SSCL5 | | LCD_DATA5-B | IRQ6-DS | |
| H14 | | PA2 | A2 | MTIOC7A/ PO18 | RXD5/SMISO5/ SSCL5/SSLA3-B | | LCD_DATA6-B | | |
| H15 | TRDATA3 | PG7 | D31 | | | | | | |
| J1 | EXTAL | P36 | | | | | | | |
| J2 | VCC | | | | | | | | |
| J3 | | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| J4 | TMS | PF3 | | | | | | | |
| J12 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | ET0_LINKSTA/ RSPCKA-B | | LCD_DATA3-B | | |
| J13 | VSS | | | | | | | | |
| J14 | | PA7 | A7 | TIOCB2/PO23 | ET0_WOL/ MISOA-B | | LCD_DATA1-B | | |
| J15 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B | | LCD_DATA2-B | | |
| K1 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | PCKO | | IRQ3-DS | |
| K2 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | VSYNC | | IRQ2-DS | |
| K3 | TDI | PF2 | | | RXD1/SMISO1/ SSCL1 | | | | |
| K4 | TCK | PF1 | | | SCK1 | | | | |
| K12 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6# | SDSI_D2-B | LCD_TCON2-B | | |
| K13 | | P71 | A18/CS1# | | ET0_MDIO | | | | |
| K14 | VCC | | | | | | | | |
| K15 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6 | | LCD_DATA0-B | IRQ12 | |
| L1 | | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| L2 | | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |
| L3 | TDO | PF0 | | | TXD1/SMOSI1/ SSDA1 | | | | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (8/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| R9 | | P53*2 | BCLK | | | | | | |
| R10 | VSS | | | | | | | | |
| R11 | VCC | | | | | | | | |
| R12 | | P80 | EDREQ0 | MTIOC3B/ PO26 | ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10# | QIO2-A/SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| R13 | | P76 | CS6# | PO22 | ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11 | QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| R14 | | P74 | A20/CS4# | PO19 | ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11# | | LCD_DATA21-A | | |
| R15 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | LCD_DATA22-A | IRQ12 | |

Note 1. The 176-pin LFBGA does not include the E5 pin.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| L11 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A | | | |
| L12 | TRDATA4 | P73 | CS3# | PO16 | ET0_WOL | | | | |
| L13 | VSS | | | | | | | | |
| M1 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCURB | SDHI_D0-C*1/ PIXD6 | | | |
| M2 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | SDHI_D3-C*1/ PIXD3 | | IRQ7 | ADTRG1# |
| M3 | | P86 | | MTIOC4D/ TIOCA0 | SMISO10/ SSCL10/RXD10 | PIXD1 | | | |
| M4 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | | IRQ2 | |
| M5 | VCC_USB | | | | | | | | |
| M6 | VSS_USB | | | | | | | | |
| M7 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |
| M8 | | PC6 | D2[A2/D2]*1/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | MMC_D6-A | | IRQ13 | |
| M9 | TRDATA1 | P81 | EDACK0 | MTIOC3D/ PO27 | ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10 | QIO3-A/SDHI_CD/ MMC_D3-A | | | |
| M10 | TRDATA7 | P77 | CS7# | PO23 | ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11 | QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A | | | |
| M11 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |
| M12 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | | IRQ12 | |
| M13 | VCC | | | | | | | | |
| N1 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN | SDHI_CLK-C*1/ PIXD5 | | IRQ9 | |
| N2 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID | SDHI_CMD-C*1/ PIXD4 | | IRQ8 | |
| N3 | | P87 | | MTIOC4C/ TIOCA2 | SMOSI10/ SSDA10/TXD10 | SDHI_D2-C*1/ PIXD2 | | | |
| N4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | IRQ4 | |
| N5 | | | | | USB0_DM | | | | |
| N6 | | | | | USB0_DP | | | | |

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (6/7)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 110 | | PE1 | D9[A9/D9]/ D1[A1/D1]*1 | MTIOC4C/ MTIOC3B/ PO18 | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B | MMC_D5-B | LCD_DATA15-B*1 | | ANEX1 |
| 111 | | PE0 | D8[A8/D8]/ D0[A0/D0]*1 | MTIOC3D | SCK12/SSLB1-B | MMC_D4-B | LCD_DATA16-B*1 | | ANEX0 |
| 112 | | P64 | WE#/D3[A3/ D3]*1/CS4# | | | | | | |
| 113 | | P63 | CAS#/ D2[A2/D2]*1/ CS3# | | | | | | |
| 114 | | P62 | RAS#/ D1[A1/D1]*1/ CS2# | | | | | | |
| 115 | | P61 | SDCS#/ D0[A0/D0]*1/ CS1# | | | | | | |
| 116 | VSS | | | | | | | | |
| 117 | | P60 | CS0# | | | | | | |
| 118 | VCC | | | | | | | | |
| 119 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | SSLC3-A | QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B | LCD_DATA17-B*1 | IRQ7 | AN107 |
| 120 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | SSLC2-A | QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B*1 | IRQ6 | AN106 |
| 121 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ POE10# | SSLC1-A | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DATA19-B*1 | IRQ5 | AN113 |
| 122 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | SSLC0-A | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B*1 | IRQ4 | AN112 |
| 123 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | RSPCKC-A | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B*1 | IRQ3 | AN111 |
| 124 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | MISOC-A/CRX0 | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B*1 | IRQ2 | AN110 |
| 125 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | MOSIC-A/CTX0 | | LCD_DATA23-B*1 | IRQ1 | AN109 |
| 126 | | PD0 | D0[A0/D0] | POE4# | | | LCD_EXTCLK-B*1 | IRQ0 | AN108 |
| 127 | | P93 | A19 | POE0# | CTS7#/RTS7#/ SS7# | | | | AN117 |
| 128 | | P92 | A18 | POE4# | RXD7/SMISO7/ SSCL7 | | | | AN116 |
| 129 | | P91 | A17 | | SCK7 | | | | AN115 |
| 130 | VSS | | | | | | | | |
| 131 | | P90 | A16 | | TXD7/SMOSI7/ SSDA7 | | | | AN114 |
| 132 | VCC | | | | | | | | |
| 133 | | P47 | | | | | | IRQ15-DS | AN007 |
| 134 | | P46 | | | | | | IRQ14-DS | AN006 |
| 135 | | P45 | | | | | | IRQ13-DS | AN005 |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (2/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 26 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | SCK0/ USB0_OVRCUR B | | | | |
| 27 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN | | | IRQ9 | |
| 28 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID | | | IRQ8 | |
| 29 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | | | IRQ7 | ADTRG1 # |
| 30 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B | | | IRQ6 | ADTRG0 # |
| 31 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | | | IRQ5 | |
| 32 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A | | | IRQ4 | |
| 33 | | P13 | | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | | IRQ3 | ADTRG1 # |
| 34 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/ SCL0[FM+] | | | IRQ2 | |
| 35 | VCC_USB | | | | | | | | |
| 36 | | | | | USB0_DM | | | | |
| 37 | | | | | USB0_DP | | | | |
| 38 | VSS_USB | | | | | | | | |
| 39 | | P55 | D0[A0/D0]*1/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | ET0_EXOUT/ CRX1 | | | IRQ10 | |
| 40 | | P54 | ALE/D1[A1/ D1]*1/ EDACK0 | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1 | | | | |
| 41 | | P53*2 | BCLK | | | | | | |
| 42 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3-A | | | | |
| 43 | | P51 | WR1#/ BC1#/ WAIT# | | SCK2/SSLB2-A | | | | |
| 44 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1-A | | | | |

**Table 4.1 List of I/O Registers (Address Order) (6 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 2862h | EXDMAC1 | EXDMA Peripheral Request Flag Register | EDMPRF | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2A00h | EXDMAC | EXDMAC Module Start Register | EDMAST | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE0h | EXDMAC | Cluster Buffer Register 0 | CLSBR0 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE4h | EXDMAC | Cluster Buffer Register 1 | CLSBR1 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE8h | EXDMAC | Cluster Buffer Register 2 | CLSBR2 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BECh | EXDMAC | Cluster Buffer Register 3 | CLSBR3 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF0h | EXDMAC | Cluster Buffer Register 4 | CLSBR4 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF4h | EXDMAC | Cluster Buffer Register 5 | CLSBR5 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF8h | EXDMAC | Cluster Buffer Register 6 | CLSBR6 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BFCh | EXDMAC | Cluster Buffer Register 7 | CLSBR7 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 3002h | BSC | CS0 Mode Register | CS0MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3004h | BSC | CS0 Wait Control Register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3008h | BSC | CS0 Wait Control Register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3012h | BSC | CS1 Mode Register | CS1MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3014h | BSC | CS1 Wait Control Register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3018h | BSC | CS1 Wait Control Register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3022h | BSC | CS2 Mode Register | CS2MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3024h | BSC | CS2 Wait Control Register 1 | CS2WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3028h | BSC | CS2 Wait Control Register 2 | CS2WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3032h | BSC | CS3 Mode Register | CS3MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3034h | BSC | CS3 Wait Control Register 1 | CS3WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3038h | BSC | CS3 Wait Control Register 2 | CS3WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3042h | BSC | CS4 Mode Register | CS4MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3044h | BSC | CS4 Wait Control Register 1 | CS4WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3048h | BSC | CS4 Wait Control Register 2 | CS4WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3052h | BSC | CS5 Mode Register | CS5MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3054h | BSC | CS5 Wait Control Register 1 | CS5WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3058h | BSC | CS5 Wait Control Register 2 | CS5WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3062h | BSC | CS6 Mode Register | CS6MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3064h | BSC | CS6 Wait Control Register 1 | CS6WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3068h | BSC | CS6 Wait Control Register 2 | CS6WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3072h | BSC | CS7 Mode Register | CS7MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3074h | BSC | CS7 Wait Control Register 1 | CS7WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3078h | BSC | CS7 Wait Control Register 2 | CS7WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3802h | BSC | CS0 Control Register | CS0CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 380Ah | BSC | CS0 Recovery Cycle Register | CS0REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3812h | BSC | CS1 Control Register | CS1CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 381Ah | BSC | CS1 Recovery Cycle Register | CS1REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3822h | BSC | CS2 Control Register | CS2CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 382Ah | BSC | CS2 Recovery Cycle Register | CS2REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3832h | BSC | CS3 Control Register | CS3CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 383Ah | BSC | CS3 Recovery Cycle Register | CS3REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3842h | BSC | CS4 Control Register | CS4CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 384Ah | BSC | CS4 Recovery Cycle Register | CS4REC | 16 | 16 | 1, 2 BCLK | | Buses |

**Table 4.1 List of I/O Registers (Address Order) (14 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8040h | DA | D/A Data Register 0 | DADR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8042h | DA | D/A Data Register 1 | DADR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8044h | DA | D/A Control Register | DACR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8045h | DA | DADRm Format Select Register | DADPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8046h | DA | D/A A/D Synchronous Start Control Register | DAADSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8048h | DA | D/A Output Amplifier Control Register | DAAMPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 805Ch | DA | D/A Output Amplifier Stabilization Wait Control Register | DAASWCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DA |
| 0008 8100h | TPUA | Timer Start Register | TSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8101h | TPUA | Timer Synchronous Register | TSYR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8108h | TPU0 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8109h | TPU1 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Ah | TPU2 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Bh | TPU3 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Ch | TPU4 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 810Dh | TPU5 | Noise Filter Control Register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8110h | TPU0 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8111h | TPU0 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8112h | TPU0 | Timer I/O Control Register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8113h | TPU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8114h | TPU0 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8115h | TPU0 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8116h | TPU0 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8118h | TPU0 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 811Ah | TPU0 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 811Ch | TPU0 | Timer General Register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 811Eh | TPU0 | Timer General Register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8120h | TPU1 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8121h | TPU1 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8122h | TPU1 | Timer I/O Control Register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8124h | TPU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8125h | TPU1 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8126h | TPU1 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8128h | TPU1 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 812Ah | TPU1 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8130h | TPU2 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8131h | TPU2 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8132h | TPU2 | Timer I/O Control Register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8134h | TPU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8135h | TPU2 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8136h | TPU2 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8138h | TPU2 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 813Ah | TPU2 | Timer General Register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8140h | TPU3 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8141h | TPU3 | Timer Mode Register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8142h | TPU3 | Timer I/O Control Register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8143h | TPU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8144h | TPU3 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8145h | TPU3 | Timer Status Register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8146h | TPU3 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 8148h | TPU3 | Timer General Register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |

**Table 4.1 List of I/O Registers (Address Order) (37 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C086h | PORT3 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C087h | PORT3 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C088h | PORT4 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C089h | PORT4 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ah | PORT5 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Bh | PORT5 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ch | PORT6 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Dh | PORT6 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Eh | PORT7 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Fh | PORT7 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C090h | PORT8 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C091h | PORT8 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C092h | PORT9 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C093h | PORT9 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C094h | PORTA | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C095h | PORTA | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C096h | PORTB | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C097h | PORTB | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C098h | PORTC | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C099h | PORTC | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Ah | PORTD | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Bh | PORTD | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Ch | PORTE | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Dh | PORTE | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Eh | PORTF | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Fh | PORTF | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A0h | PORTG | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A1h | PORTG | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A4h | PORTJ | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A5h | PORTJ | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C0h | PORT0 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

**Table 4.1 List of I/O Registers (Address Order) (45 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 0820h to 0009 083Fh | CAN0 | Message Control Registers 0 to 31 | MCTL0 to 31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0840h | CAN0 | Control Register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0842h | CAN0 | Status Register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0844h | CAN0 | Bit Configuration Register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0848h | CAN0 | Receive FIFO Control Register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0849h | CAN0 | Receive FIFO Pointer Control Register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Ah | CAN0 | Transmit FIFO Control Register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Bh | CAN0 | Transmit FIFO Pointer Control Register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Ch | CAN0 | Error Interrupt Enable Register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Dh | CAN0 | Error Interrupt Factor Judge Register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Eh | CAN0 | Receive Error Count Register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Fh | CAN0 | Transmit Error Count Register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0850h | CAN0 | Error Code Store Register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0851h | CAN0 | Channel Search Support Register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0852h | CAN0 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0853h | CAN0 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0854h | CAN0 | Time Stamp Register | TSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0856h | CAN0 | Acceptance Filter Support Register | AFSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0858h | CAN0 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1200h to 0009 13FFh | CAN1 | Mailbox Registers 0 to 31 | MB0 to 31 | 128 | 8, 16, 32*6 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1400h to 0009 141Fh | CAN1 | Mask Registers 0 to 7 | MKR0 to 7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1420h | CAN1 | FIFO Received ID Compare Register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1424h | CAN1 | FIFO Received ID Compare Register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1428h | CAN1 | Mask Invalid Register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 142Ch | CAN1 | Mailbox Interrupt Enable Register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1820h to 0009 183Fh | CAN1 | Message Control Registers 0 to 31 | MCTL0 to 31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1840h | CAN1 | Control Register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1842h | CAN1 | Status Register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1844h | CAN1 | Bit Configuration Register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1848h | CAN1 | Receive FIFO Control Register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1849h | CAN1 | Receive FIFO Pointer Control Register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Ah | CAN1 | Transmit FIFO Control Register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Bh | CAN1 | Transmit FIFO Pointer Control Register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Ch | CAN1 | Error Interrupt Enable Register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Dh | CAN1 | Error Interrupt Factor Judge Register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Eh | CAN1 | Receive Error Count Register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 184Fh | CAN1 | Transmit Error Count Register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1850h | CAN1 | Error Code Store Register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1851h | CAN1 | Channel Search Support Register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1852h | CAN1 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1853h | CAN1 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1854h | CAN1 | Time Stamp Register | TSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1856h | CAN1 | Acceptance Filter Support Register | AFSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 1858h | CAN1 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 4200h | CMTW0 | Timer Start Register | CMWSTR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMTW |

**Table 4.1 List of I/O Registers (Address Order) (52 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 124Dh | MTU4 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1260h | MTU | Timer Waveform Control Register A | TWCRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1270h | MTU | Timer Mode Register 2A | TMDR2A | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1272h | MTU3 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1274h | MTU4 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1276h | MTU4 | Timer General Register F | TGRF | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1280h | MTU | Timer Start Register A | TSTRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1281h | MTU | Timer Synchronous Register A | TSYRA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1282h | MTU | Timer Counter Synchronous Start Register | TCSYSTR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1284h | MTU | Timer Read/Write Enable Register A | TRWERA | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1290h | MTU0 | Noise Filter Control Register 0 | NFCR0 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1291h | MTU1 | Noise Filter Control Register 1 | NFCR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1292h | MTU2 | Noise Filter Control Register 2 | NFCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1293h | MTU3 | Noise Filter Control Register 3 | NFCR3 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1294h | MTU4 | Noise Filter Control Register 4 | NFCR4 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1298h | MTU8 | Noise Filter Control Register 8 | NFCR8 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1299h | MTU0 | Noise Filter Control Register C | NFCRC | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1300h | MTU0 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1301h | MTU0 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1302h | MTU0 | Timer I/O Control Register H | TIORH | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1303h | MTU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1304h | MTU0 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1306h | MTU0 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1308h | MTU0 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 130Ah | MTU0 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 130Ch | MTU0 | Timer General Register C | TGRC | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 130Eh | MTU0 | Timer General Register D | TGRD | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1320h | MTU0 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (59 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000E 1300h | GLCDC | Gamma Correction G Block Register Update Control Register | GAMGVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1304h | GLCDC | Gamma Correction Block Function Switch Register | GAMSW | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1308h | GLCDC | Gamma Correction G Table Setting Register 1 | GAMGLUT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 130Ch | GLCDC | Gamma Correction G Table Setting Register 2 | GAMGLUT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1310h | GLCDC | Gamma Correction G Table Setting Register 3 | GAMGLUT3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1314h | GLCDC | Gamma Correction G Table Setting Register 4 | GAMGLUT4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1318h | GLCDC | Gamma Correction G Table Setting Register 5 | GAMGLUT5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 131Ch | GLCDC | Gamma Correction G Table Setting Register 6 | GAMGLUT6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1320h | GLCDC | Gamma Correction G Table Setting Register 7 | GAMGLUT7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1324h | GLCDC | Gamma Correction G Table Setting Register 8 | GAMGLUT8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1328h | GLCDC | Gamma Correction G Area Setting Register 1 | GAMGAREA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 132Ch | GLCDC | Gamma Correction G Area Setting Register 2 | GAMGAREA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1330h | GLCDC | Gamma Correction G Area Setting Register 3 | GAMGAREA3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1334h | GLCDC | Gamma Correction G Area Setting Register 4 | GAMGAREA4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1338h | GLCDC | Gamma Correction G Area Setting Register 5 | GAMGAREA5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1340h | GLCDC | Gamma Correction B Block Register Update Control Register | GAMBVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1348h | GLCDC | Gamma Correction B Table Setting Register 1 | GAMBLUT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 134Ch | GLCDC | Gamma Correction B Table Setting Register 2 | GAMBLUT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1350h | GLCDC | Gamma Correction B Table Setting Register 3 | GAMBLUT3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1354h | GLCDC | Gamma Correction B Table Setting Register 4 | GAMBLUT4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1358h | GLCDC | Gamma Correction B Table Setting Register 5 | GAMBLUT5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 135Ch | GLCDC | Gamma Correction B Table Setting Register 6 | GAMBLUT6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1360h | GLCDC | Gamma Correction B Table Setting Register 7 | GAMBLUT7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1364h | GLCDC | Gamma Correction B Table Setting Register 8 | GAMBLUT8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1368h | GLCDC | Gamma Correction B Area Setting Register 1 | GAMBAREA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 136Ch | GLCDC | Gamma Correction B Area Setting Register 2 | GAMBAREA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1370h | GLCDC | Gamma Correction B Area Setting Register 3 | GAMBAREA3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1374h | GLCDC | Gamma Correction B Area Setting Register 4 | GAMBAREA4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1378h | GLCDC | Gamma Correction B Area Setting Register 5 | GAMBAREA5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1380h | GLCDC | Gamma Correction R Block Register Update Control Register | GAMRVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1388h | GLCDC | Gamma Correction R Table Setting Register 1 | GAMRLUT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 138Ch | GLCDC | Gamma Correction R Table Setting Register 2 | GAMRLUT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1390h | GLCDC | Gamma Correction R Table Setting Register 3 | GAMRLUT3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1394h | GLCDC | Gamma Correction R Table Setting Register 4 | GAMRLUT4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 1398h | GLCDC | Gamma Correction R Table Setting Register 5 | GAMRLUT5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 139Ch | GLCDC | Gamma Correction R Table Setting Register 6 | GAMRLUT6 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13A0h | GLCDC | Gamma Correction R Table Setting Register 7 | GAMRLUT7 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13A4h | GLCDC | Gamma Correction R Table Setting Register 8 | GAMRLUT8 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13A8h | GLCDC | Gamma Correction R Area Setting Register 1 | GAMRAREA1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13ACh | GLCDC | Gamma Correction R Area Setting Register 2 | GAMRAREA2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13B0h | GLCDC | Gamma Correction R Area Setting Register 3 | GAMRAREA3 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13B4h | GLCDC | Gamma Correction R Area Setting Register 4 | GAMRAREA4 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13B8h | GLCDC | Gamma Correction R Area Setting Register 5 | GAMRAREA5 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13C0h | GLCDC | Output Control Block Register Update Control Register | OUTVEN | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13C4h | GLCDC | Output Interface Register | OUTSET | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13C8h | GLCDC | Brightness Adjustment Register 1 | BRIGHT1 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |
| 000E 13CCh | GLCDC | Brightness Adjustment Register 2 | BRIGHT2 | 32 | 32 | 2, 3 PCLKA | 1, 2 ICLK | GLCDC |

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Rating**

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | | VCC, VCC_USB | –0.3 to +4.0 | V |
| $V_{BATT}$ power supply voltage | | $V_{BATT}$ | –0.3 to +4.0 | V |
| Input voltage (except for ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 0.3 (up to 4.0) | V |
| Input voltage (ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 4.0 (up to 5.8) | V |
| Reference power supply voltage | | VREFH0 | –0.3 to AVCC0 + 0.3 (up to 4.0) | V |
| Analog power supply voltage | | AVCC0, AVCC1*2 | –0.3 to +4.0 | V |
| Analog input voltage | | $V_{AN}$ | –0.3 to AVCC + 0.3 (up to 4.0) | V |
| Junction temperature | D version | $T_j$ | –40 to +105 | °C |
| | G version | $T_j$ | –40 to +125 | °C |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

**Table 5.2 Recommended operating conditions**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage*1 | VCC | 2.7 | — | 3.6 | V |
| | VSS | — | 0 | — | V |
| $V_{BATT}$ power supply voltage | $V_{BATT}$ | 2.0 | — | 3.6 | V |
| USB power supply voltage | VCC_USB | — | VCC | — | V |
| | VSS_USB | — | 0 | — | V |
| Analog power supply voltage*1, *2 | AVCC0 | — | VCC | — | V |
| | AVSS0 | — | 0 | — | V |
| | AVCC1 | — | VCC | — | V |
| | AVSS1 | — | 0 | — | V |
| | VREFH0 | 2.7 | — | AVCC0 | V |
| | VREFL0 | — | 0 | — | V |
| Input voltage (except for 5 V tolerant ports, except for ports 03, 05 and 40 to 47)*3 | $V_{in}$ | –0.3 | — | VCC + 0.3 | V |
| Input voltage (ports 03, 05 and 40 to 47) | $V_{in}$ | –0.3 | — | AVCC + 0.3 | V |
| Input voltage (5V tolerant ports 11 to 17, ports 20 and 21, ports 30 to 33, port 67, and ports C0 to C3)*4 | $V_{in}$ | –0.3 | — | VCC + 3.6 (up to 5.5) | V |
| Input voltage (5V tolerant port 07) | $V_{in}$ | –0.3 | — | AVCC + 3.6 (up to 5.5) | V |
| Operating temperature (D version) | $T_{opr}$ | –40 | — | 85 | °C |
| Operating temperature (G version) | $T_{opr}$ | –40 | — | 105 | °C |

Note 1. Comply with the following potential condition: VCC = AVCC0 = AVCC1 = VCC_USB

Note 2. For details, see section 53.6.11, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

Note 3. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

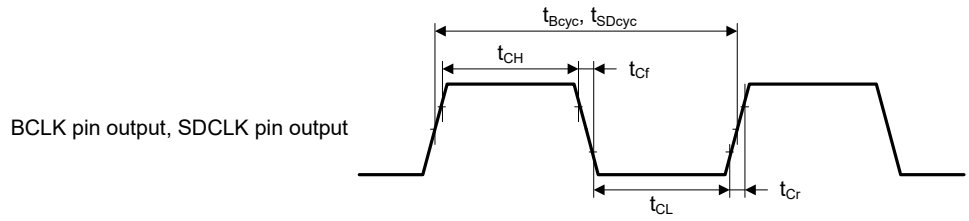
Note 4. For P32, P31, and P30, input as follows when the $V_{BATT}$ power supply is selected.
$V_{in}$ Min. = –0.3, Max. = $V_{BATT}$ + 0.3 ($V_{BATT}$ = 2.0 to 3.6 V)

## 5.3.2 Clock Timing

**Table 5.14 BCLK Pin Output, SDCLK Pin Output Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| BCLK pin output cycle time | Other than 100-pin package | $t_{Bcyc}$ | 16.6 | — | — | ns | Figure 5.3 |
| | 100-pin package | | 33.2 | — | — | ns | |
| BCLK pin output high pulse width | | $t_{CH}$ | 3.3 | — | — | ns | |
| BCLK pin output low pulse width | | $t_{CL}$ | 3.3 | — | — | ns | |
| BCLK pin output rising time | | $t_{Cr}$ | — | — | 5 | ns | |
| BCLK pin output falling time | | $t_{Cf}$ | — | — | 5 | ns | |
| SDCLK pin output cycle time | Other than 100-pin package | $t_{Bcyc}$ | 16.6 | — | — | ns | |
| SDCLK pin output high pulse width | | $t_{CH}$ | 3.3 | — | — | ns | |
| SDCLK pin output low pulse width | | $t_{CL}$ | 3.3 | — | — | ns | |
| SDCLK pin output rising time | | $t_{Cr}$ | — | — | 5 | ns | |
| SDCLK pin output falling time | | $t_{Cf}$ | — | — | 5 | ns | |




Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, C = 30 pF

**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

### Table 5.28 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| TMR | Timer clock pulse width | Single-edge setting | $t_{TMCWH}$, $t_{TMCWL}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.36 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

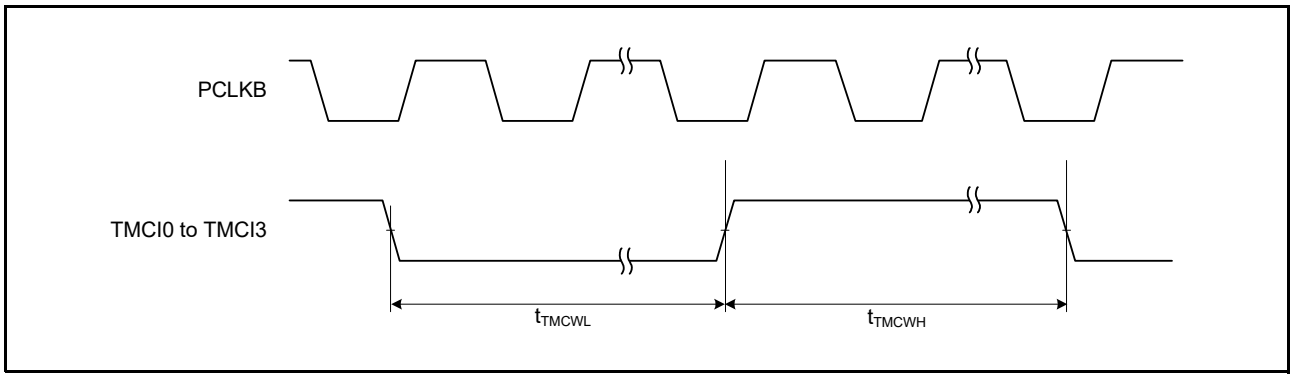



**Figure 5.36 TMR Clock Input Timing**

### Table 5.29 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| CMTW | Input capture input pulse width | Single-edge setting | $t_{CMTWTICW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.37 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

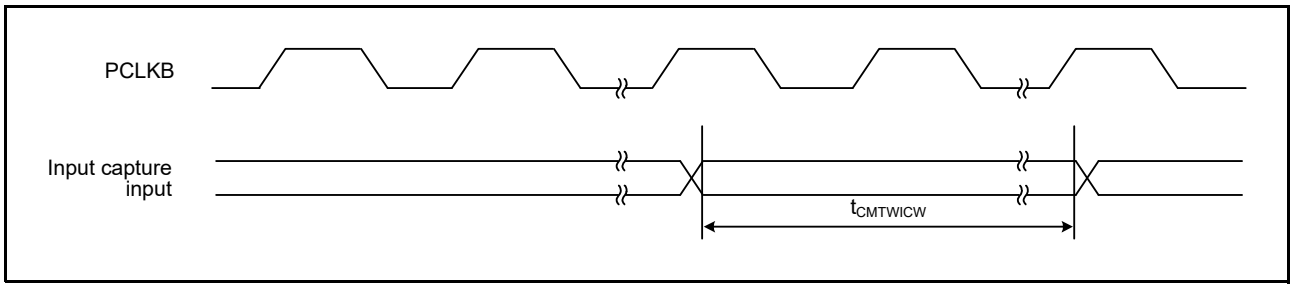



**Figure 5.37 CMTW Input Capture Input Timing**

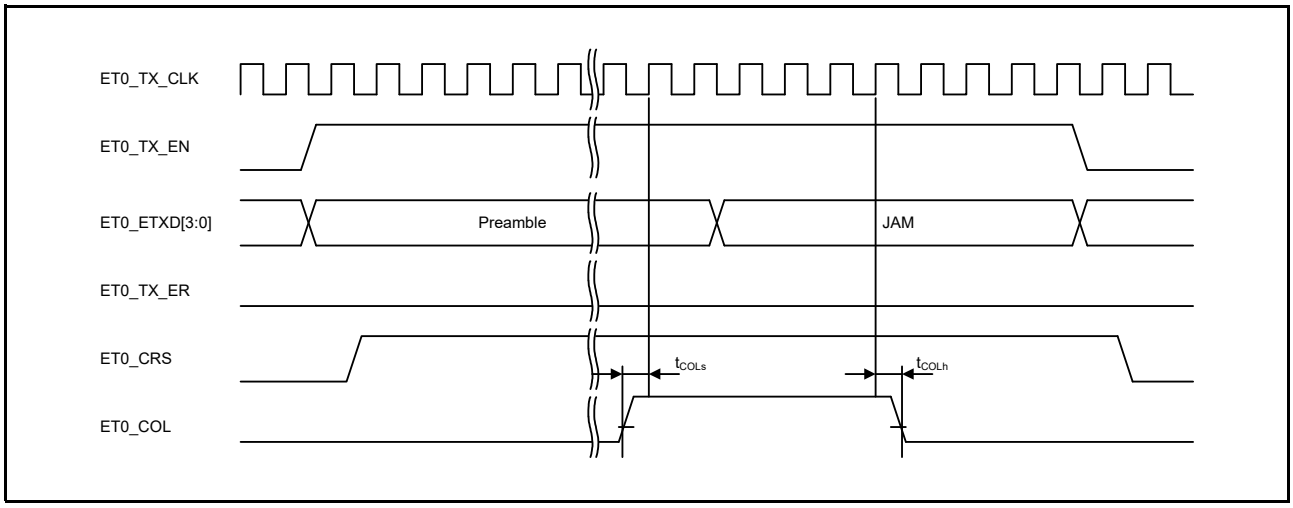



**Figure 5.62 MII Transmission Timing (Conflict Occurrence)**

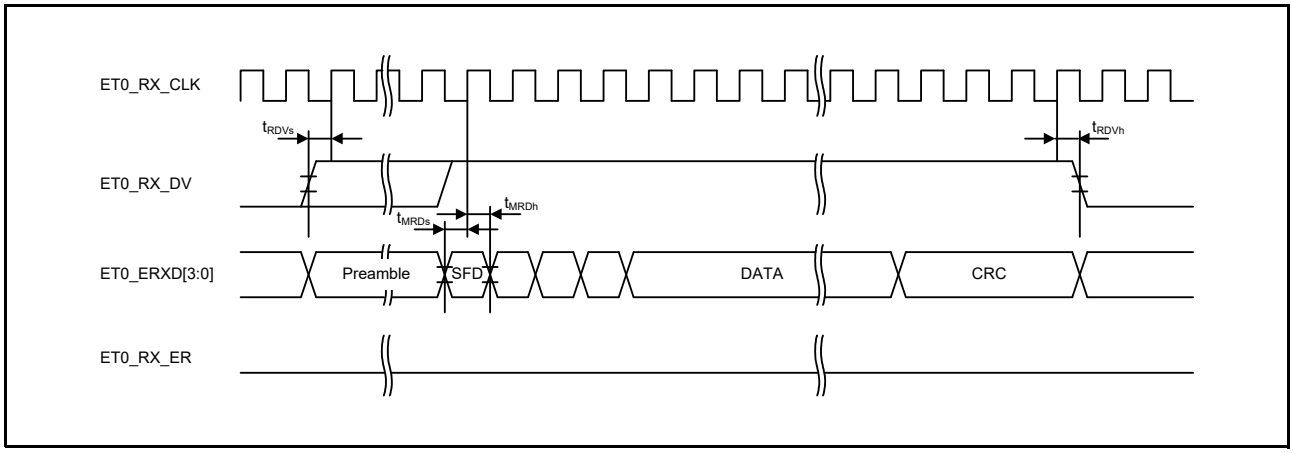



**Figure 5.63 MII Reception Timing (Normal Operation)**

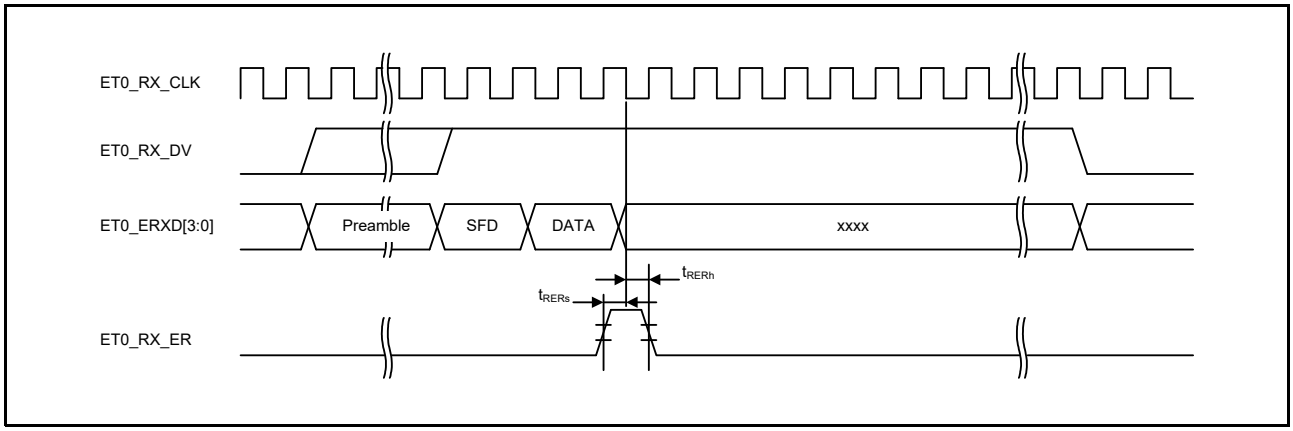



**Figure 5.64 MII Reception Timing (Error Occurrence)**

### Table 5.55 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

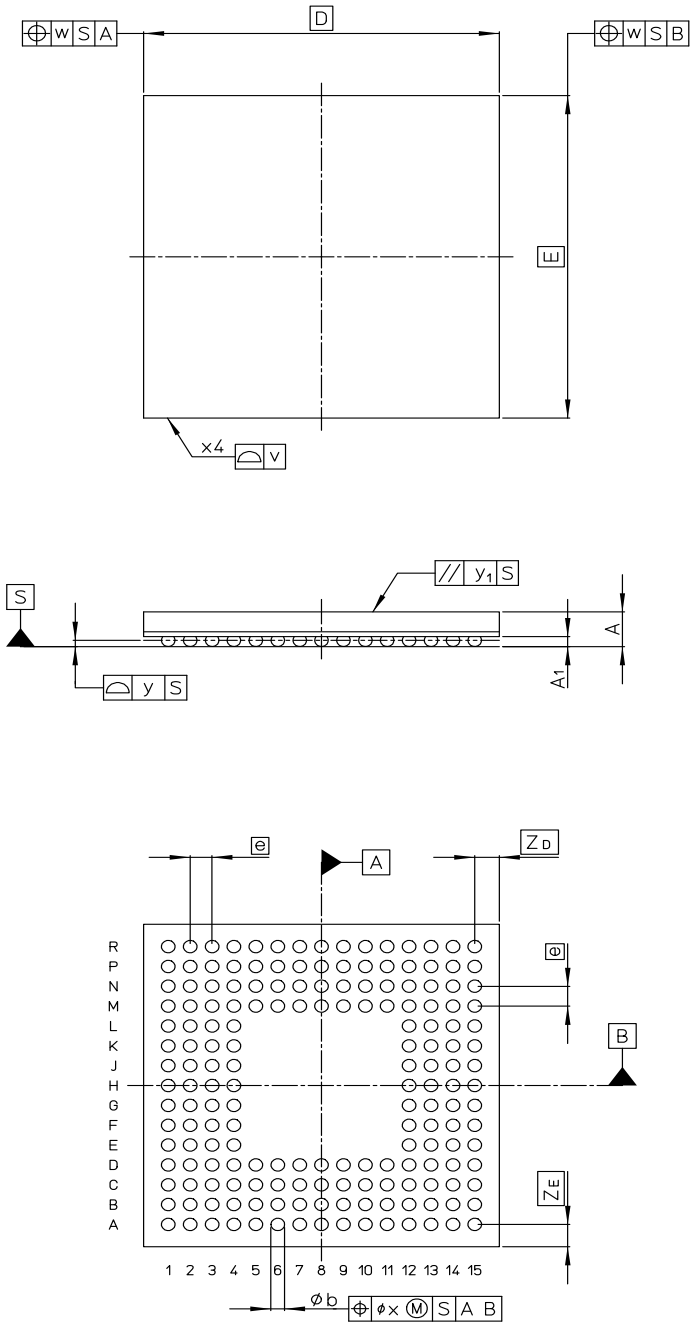
| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 15 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 4 bytes | $t_{DP4}$ | — | 0.36 | 3.8 | — | 0.18 | 1.9 | — | 0.16 | 1.7 | ms |
| Erasure time | 64 bytes | $t_{DP64}$ | — | 3.1 | 18 | — | 1.9 | 11 | — | 1.7 | 10 | ms |
| | 128 bytes | $t_{DP128}$ | — | 4.7 | 27 | — | 2.9 | 16 | — | 2.6 | 15 | ms |
| | 256 bytes | $t_{DP256}$ | — | 8.9 | 50 | — | 5.4 | 31 | — | 4.9 | 28 | ms |
| Blank check time | 4 bytes | $t_{DBC4}$ | — | — | 84 | — | — | 33 | — | — | 30 | µs |
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 100000 *2 | — | — | 100000 *2 | — | — | 100000 *2 | — | — | Times |
| Suspend delay time during programming | | $t_{DSPD}$ | — | — | 264 | — | — | 132 | — | — | 120 | µs |
| First suspend delay time during erasure (in suspend priority mode) | 64 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| | 128 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| | 256 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| Second suspend delay time during erasure (in suspend priority mode) | 64 bytes | — | — | — | 300 | — | — | 300 | — | — | 300 | µs |
| | 128 bytes | — | — | — | 390 | — | — | 390 | — | — | 390 | µs |
| | 256 bytes | — | — | — | 570 | — | — | 570 | — | — | 570 | µs |
| Suspend delay time during erasing (in suspend priority mode) | 64 bytes | — | — | — | 300 | — | — | 300 | — | — | 300 | µs |
| | 128 bytes | — | — | — | 390 | — | — | 390 | — | — | 390 | µs |
| | 256 bytes | — | — | — | 570 | — | — | 570 | — | — | 570 | µs |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 22 | — | — | 20 | µs |
| Data hold time*3 | | $t_{DDRP}$ | 10 | — | — | 10 | — | — | 10 | — | — | Year |

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

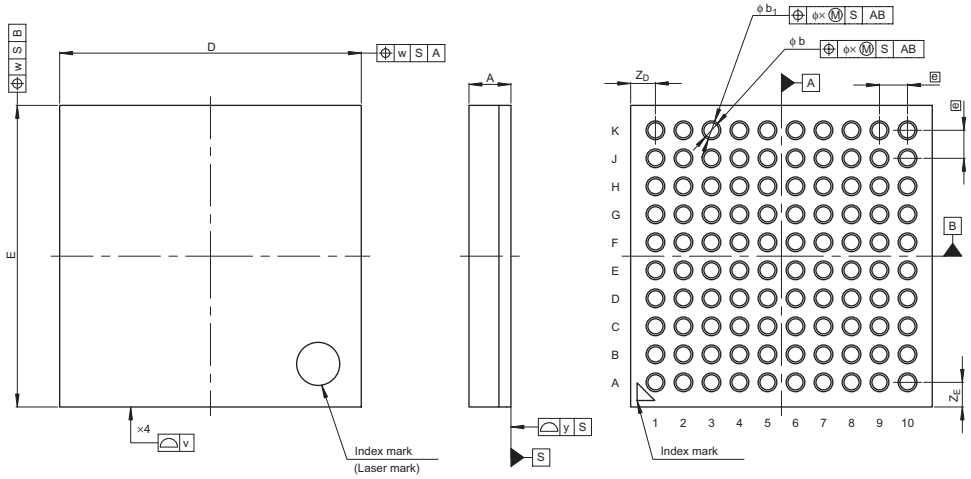
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFBGA176-13x13-0.80 | PLBG0176GA-A | BP-176/BP-176V | 0.45g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 13.0 | — |
| E | — | 13.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.40 |
| A1 | 0.35 | 0.40 | 0.45 |
| e | — | 0.80 | — |
| b | 0.45 | 0.50 | 0.55 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| y1 | — | — | 0.2 |
| SD | — | — | — |
| SE | — | — | — |
| ZD | — | 0.90 | — |
| ZE | — | 0.90 | — |

Figure B 176-Pin LFBGA (PLBG0176GA-A)

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA100-7x7-0.65 | PTLG0100JA-A | 100F0G | 0.1g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.385 | 0.435 | 0.485 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |

Figure F 100-Pin TFLGA (PTLG0100JA-A)