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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56514edfb-30

Table 1.3 List of Products (3/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N4EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
RX65N (G version)	R5F565NEDGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NEDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565N9AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N9BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N9EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N9FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105

Table 1.3 List of Products (7/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F5651EDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651EHDJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F5651CDDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651CHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F56519ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56519BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56519EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56519FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56517ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56517BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56517EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56517FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56514ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56514BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56514EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56514FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
RX651 (G version)	R5F5651EDGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651EHGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651CDGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651CHGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651EDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651EHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651CDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651CHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F56519AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F56519BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F56519EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F56519FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105
	R5F56517AGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F56517BGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
B15		PE3	D11[A11/ D11]/D3[A3/ D3]	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#/SS12#	MMC_D7-B	LCD_DA TA13-B		AN101
C1	AVSS1								
C2	AVCC1								
C3	VREFH0								
C4		P43						IRQ11- DS	AN003
C5		P45						IRQ13- DS	AN005
C6		P90	D16/A16		TXD7/SMOSI7/ SSDA7				AN114
C7		PD0	D0[A0/D0]	POE4#			LCD_EX TCLK-B	IRQ0	AN108
C8		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2- B/MMC_D2-B	LCD_DA TA22-B	IRQ2	AN110
C9		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3- B/MMC_D3-B	LCD_DA TA21-B	IRQ3	AN111
C10	TRDATA6	PG0	D24						
C11	VCC								
C12		P62	RAS#/ D1[A1/D1]/ CS2#						
C13		PE4	D12[A12/ D12]/D4[A4/ D4]	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DA TA12-B		AN102
C14	VSS								
C15		P70	SDCLK						
D1		P01		TMC10	RXD6/SMISO6/ SSCL6			IRQ9	AN119
D2		P02		TMC11	SCK6			IRQ10	AN120
D3		P03						IRQ11	DA0
D4		P00		TMR10	TXD6/SMOSI6/ SSDA6			IRQ8	AN118
D5		P44						IRQ12- DS	AN004
D6		P93	D19/A19	POE0#	CTS7#/RTS7#/ SS7#				AN117
D7	TRDATA4	P95	D21/A21						
D8	VSS								
D9		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DA TA19-B	IRQ5	AN113
D10		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DA TA17-B	IRQ7	AN107
D11		P61	SDCS#/ D0[A0/D0]/ CS1#						
D12		PE5	D13[A13/ D13]/D5[A5/ D5]	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DA TA11-B	IRQ5	AN103
D13	VCC								

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
D14		PE7	D15[A15/ D15]/D7[A7/ D7]	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DA TA9-B	IRQ7	AN105
D15		P65	CKE/CS5#						
E1		PJ5		POE8#	CTS2#/RTS2#/ SS2#				
E2	EMLE								
E3		PF5						IRQ4	
E4	VSS								
E5 *1	NC								
E12		PE6	D14[A14/ D14]/D6[A6/ D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DA TA10-B	IRQ6	AN104
E13	TRDATA0	PG2	D26						
E14	TRDATA1	PG3	D27						
E15		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	VBATT								
F2	VCL								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
F4	BSCANP								
F12		P66	DQM0/CS6#	MTIOC7D					
F13	TRSYNC	PG4	D28						
F14		PA0	DQM2/ BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DA TA8-B		
F15	VSS								
G1	XCIN								
G2	XCOUT								
G3	MD/FINED								
G4	TRST#	PF4							
G12	TRCLK	PG5	D29						
G13	TRDATA2	PG6	D30						
G14		PA1	DQM3/A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DA TA7-B	IRQ11	
G15	VCC								
H1	XTAL	P37							
H2	VSS								
H3	RES#								
H4	UPSEL	P35						NMI	
H12		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DA TA4-B	IRQ5-DS	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface			
145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCI, RSPI, RIIC, CAN, USB)	(QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
L11		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A			
L12	TRDATA4	P73	CS3#	PO16	ET0_WOL				
L13	VSS								
M1		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C*1/ PIXD6			
M2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C*1/ PIXD3		IRQ7	ADTRG1 #
M3		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
M4		P12		TMC11	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
M5	VCC_USB								
M6	VSS_USB								
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
M8		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMC12/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A		IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A			
M10	TRDATA7	P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A			
M11		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
M12		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
M13	VCC								
N1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN	SDHI_CLK-C*1/ PIXD5		IRQ9	
N2		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID	SDHI_CMD-C*1/ PIXD4		IRQ8	
N3		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C*1/ PIXD2			
N4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
N5					USB0_DM				
N6					USB0_DP				

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (1/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
1	AVCC1								
2	EMLE								
3	AVSS1								
4		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
5	VCL								
6	VBATT								
7	MD/FINED								
8	XCIN								
9	XCOUT								
10	RES#								
11	XTAL	P37							
12	VSS								
13	EXTAL	P36							
14	VCC								
15	UPSEL	P35						NMI	
16	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
17		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0			IRQ3-DS	
18		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN			IRQ2-DS	
19	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
20	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
21	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A				
22	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
23		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3				ADTRG0 #
24		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN				
25		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#				

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP) / User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP).

Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

(2) Exception Table Register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.

(3) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.

(4) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(9) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (E_j) enables the exception handling ($E_j = 1$), the exception cause can be identified by checking the corresponding C_j flag in the exception handling routine. If the exception handling is masked ($E_j = 0$), the occurrence of exception can be checked by reading the F_j flag at the end of a series of processing. Once the F_j flag has been set to 1, this value is retained until it is cleared to 0 by software ($j = X, U, Z, O, \text{ or } V$).

Table 4.1 List of I/O Registers (Address Order) (17 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8320h	RIIC1	I ² C-bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8321h	RIIC1	I ² C-bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8322h	RIIC1	I ² C-bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8323h	RIIC1	I ² C-bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8324h	RIIC1	I ² C-bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8325h	RIIC1	I ² C-bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8326h	RIIC1	I ² C-bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8327h	RIIC1	I ² C-bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8328h	RIIC1	I ² C-bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8329h	RIIC1	I ² C-bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8330h	RIIC1	I ² C-bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8331h	RIIC1	I ² C-bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8332h	RIIC1	I ² C-bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8333h	RIIC1	I ² C-bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8340h	RIIC2	I ² C-bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8341h	RIIC2	I ² C-bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8342h	RIIC2	I ² C-bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8343h	RIIC2	I ² C-bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8344h	RIIC2	I ² C-bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8345h	RIIC2	I ² C-bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8346h	RIIC2	I ² C-bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8347h	RIIC2	I ² C-bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8348h	RIIC2	I ² C-bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8349h	RIIC2	I ² C-bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ah	RIIC2	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Bh	RIIC2	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ch	RIIC2	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Dh	RIIC2	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Eh	RIIC2	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Fh	RIIC2	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8350h	RIIC2	I ² C-bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8351h	RIIC2	I ² C-bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8352h	RIIC2	I ² C-bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8353h	RIIC2	I ² C-bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8500h	MMCIF	Command Setting Register	CECMDSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8508h	MMCIF	Argument Register	CEARG	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 850Ch	MMCIF	Automatically Issued CMD12 Argument Register	CEARGCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8510h	MMCIF	Command Control Register	CECMDCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8514h	MMCIF	Transfer Block Setting Register	CEBLOCKSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8518h	MMCIF	Clock Control Register	CECLKCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 851Ch	MMCIF	Buffer Access Setting Register	CEBUFACC	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8520h	MMCIF	Response Register 3	CERESP3	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8524h	MMCIF	Response Register 2	CERESP2	32	32	2, 3 PCLKB	2 ICLK	MMCIF

Table 4.1 List of I/O Registers (Address Order) (20 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9110h	S12AD1	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9112h	S12AD1	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9114h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9116h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9118h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 911Ah	S12AD1	A/D Temperature Sensor Data Register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 911Ch	S12AD1	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 911Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9120h	S12AD1	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9122h	S12AD1	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9124h	S12AD1	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9126h	S12AD1	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9128h	S12AD1	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 912Ah	S12AD1	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 912Ch	S12AD1	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 912Eh	S12AD1	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9130h	S12AD1	A/D Data Register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9132h	S12AD1	A/D Data Register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9134h	S12AD1	A/D Data Register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9136h	S12AD1	A/D Data Register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9138h	S12AD1	A/D Data Register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 913Ah	S12AD1	A/D Data Register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 913Ch	S12AD1	A/D Data Register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 913Eh	S12AD1	A/D Data Register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9140h	S12AD1	A/D Data Register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9142h	S12AD1	A/D Data Register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9144h	S12AD1	A/D Data Register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9146h	S12AD1	A/D Data Register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9148h	S12AD1	A/D Data Register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9163h	S12AD1	A/D Conversion Time Setting Protection Release Register	ADSAMPR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 916Eh	S12AD1	A/D Conversion Time Setting Register	ADSAM	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa

Table 4.1 List of I/O Registers (Address Order) (51 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 01F8h	ETHER C0	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 1200h	MTU3	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ch	MTU3	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1231h	MTU	Timer Interrupt Skipping Counter 1A	TITCNT1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ch	MTU	Timer Interrupt Skipping Counter 2A	TITCNT2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (53 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1408h	MTU2	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 140Ch	MTU2	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1600h	MTU8	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1601h	MTU8	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1602h	MTU8	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1603h	MTU8	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1604h	MTU8	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1606h	MTU8	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1608h	MTU8	Timer Counter	TCNT	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 160Ch	MTU8	Timer General Register A	TGRA	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1610h	MTU8	Timer General Register B	TGRB	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1614h	MTU8	Timer General Register C	TGRC	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1618h	MTU8	Timer General Register D	TGRD	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A00h	MTU6	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A10h	MTU6	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRb	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A31h	MTU	Timer Interrupt Skipping Counter 1B	TITCNT1B	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTBRB	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (56 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 006Ch	SCI11	I ² C Status Register	SISR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Dh	SCI11	SPI Mode Register	SPMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Eh	SCI11	Transmit Data Register H	TDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Fh	SCI11	Transmit Data Register L	TDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Eh	SCI11	Transmit Data Register HL	TDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 006Eh	SCI11	Transmit FIFO Data Register	FTDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Fh	SCI11	Transmit FIFO Data Register	FTDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Eh	SCI11	Transmit FIFO Data Register	FTDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0070h	SCI11	Receive Data Register H	RDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0071h	SCI11	Receive Data Register L	RDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0070h	SCI11	Receive Data Register HL	RDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0070h	SCI11	Receive FIFO Data Register	FRDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0071h	SCI11	Receive FIFO Data Register	FRDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0070h	SCI11	Receive FIFO Data Register	FRDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0072h	SCI11	Modulation Duty Register	MDDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0073h	SCI11	Data Comparison Control Register	DCCR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0074h	SCI11	FIFO Control Register	FCR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0075h	SCI11	FIFO Control Register	FCR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0074h	SCI11	FIFO Control Register	FCR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0076h	SCI11	FIFO Data Count Register	FDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0077h	SCI11	FIFO Data Count Register	FDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0076h	SCI11	FIFO Data Count Register	FDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0078h	SCI11	Line Status Register	LSR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0079h	SCI11	Line Status Register	LSR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0078h	SCI11	Line Status Register	LSR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 007Ah	SCI11	Comparison Data Register	CDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 007Bh	SCI11	Comparison Data Register	CDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 007Ah	SCI11	Comparison Data Register	CDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 007Ch	SCI11	Serial Port Register	SPTR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0100h	RSPI0	RSPI Control Register	SPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0101h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0102h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0103h	RSPI0	RSPI Status Register	SPSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0104h	RSPI0	RSPI Data Register	SPDR	32	8, 16, 32	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0108h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0109h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0110h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0112h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0114h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0116h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0118h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 011Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 011Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc

Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Note 7. Reference value

Table 5.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,

T_a = T_{opr}

Item			Symbol	D version		G version		Unit	Test Conditions				
				Typ.	Max.	Typ.	Max.						
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	60	—	73	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz			
		Normal	Peripheral function clock signal supplied*4		26	—	26	—					
			Peripheral function clock signal stopped*4		13	—	13	—					
		Core Mark	Peripheral function clock signal stopped*4		17	—	17	—					
			Sleep mode: The clock signal to peripheral modules is supplied*4			20	38	20			52		
		All-module-clock-stop mode (reference value)			9	26	9	39					
		Increased by BGO operation*7	Reading from the code flash memory while the data flash memory is being programmed		6	—	6	—					
			Reading from the code flash memory while the code flash memory is being programmed		7	—	7	—					
		Increased by Trusted Secure IP operation			—	12	—	12					
		Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4			1.6	—	1.6	—					
		Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4			1.6	—	1.6	—					
		Software standby mode			1.6	13	1.6	22.4					
		Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)		15.5	70	15.5	98			μA	V _{BATT} = 2.0 V, VCC = 0 V V _{BATT} = 3.3 V, VCC = 0 V V _{BATT} = 2.0 V, VCC = 0 V V _{BATT} = 3.3 V, VCC = 0 V	
			Power not supplied to standby RAM and USB resume detecting unit (USB0 only)		Power-on reset circuit and low-power consumption function disabled*5	11.5	42	11.5					54
	Power-on reset circuit and low-power consumption function enabled*6			4.9	32	4.9	47						
	Increased by RTC operation		When a low C _L crystal is in use	1	—	1	—						
			When a standard C _L crystal is in use	2	—	2	—						
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use	0.9	—	0.9	—						
				1.6	—	1.6	—						
			When a crystal oscillator for standard clock loads is in use	1.7	—	1.7	—						
				3.3	—	3.3	—						
	Inrush current on returning from deep software standby mode		Inrush current*8	I _{RUSH}	—	130	—	130	mA				
			Energy of inrush current*8	E _{RUSH}	—	1.0	—	1.0		μC			

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripheral modules is stopped in this state.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)

[D version]

I_{CC} Max. = 0.38 × f + 14 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.18 × f + 4 (ICLK 1 MHz max) (normal operation in high-speed operating mode)

I_{CC} Typ. = 0.4 × f + 1.2 (low-speed operating mode 1)

I_{CC} Max. = 0.2 × f + 14 (sleep mode)

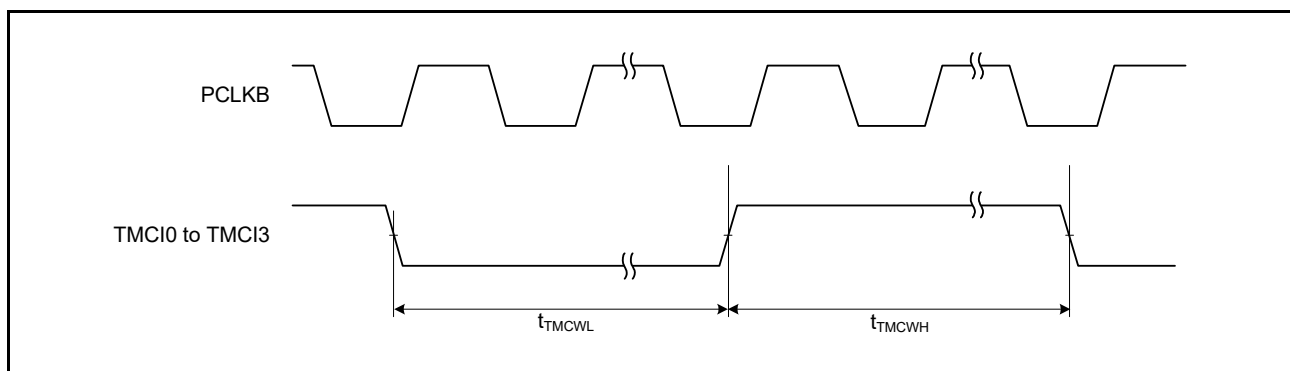
[G version]

Table 5.28 TMR Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH} , t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 5.36
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.36 TMR Clock Input Timing****Table 5.29 CMTW Timing**

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PBcyc}	Figure 5.37
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc} : PCLKB cycle

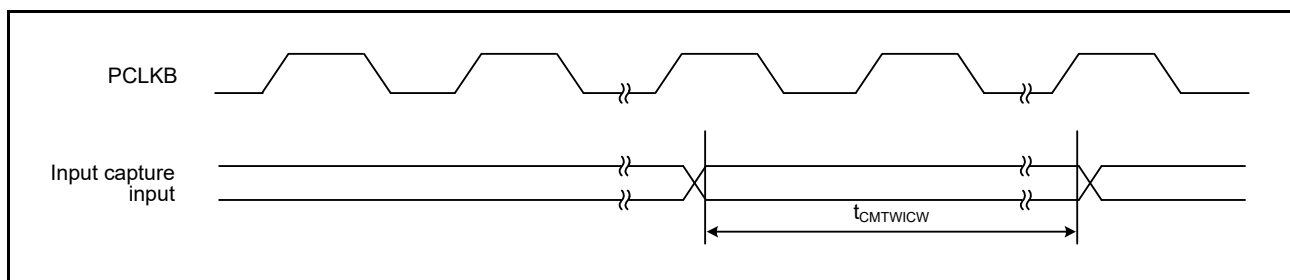
**Figure 5.37 CMTW Input Capture Input Timing**

Table 5.41 ETHERC Timing

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq VREFH0 \leq AVCC0$,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $C = 30$ pF,
High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.56 to Figure 5.58
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII0_xxx*2 setup time	T_{su}	3	—	ns	
	RMII0_xxx*2 hold time	T_{hd}	1	—	ns	
	RMII0_xxx*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.60
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET0_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.61
	ET0_ETXD0 to ET0_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET0_CRS setup time	t_{CRSs}	10	—	ns	
	ET0_CRS hold time	t_{CRSh}	10	—	ns	
	ET0_COL setup time	t_{COLs}	10	—	ns	Figure 5.62
	ET0_COL hold time	t_{COLh}	10	—	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET0_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 5.63
	ET0_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET0_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.64
	ET0_RX_ER hold time	t_{RERh}	10	—	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.65

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0

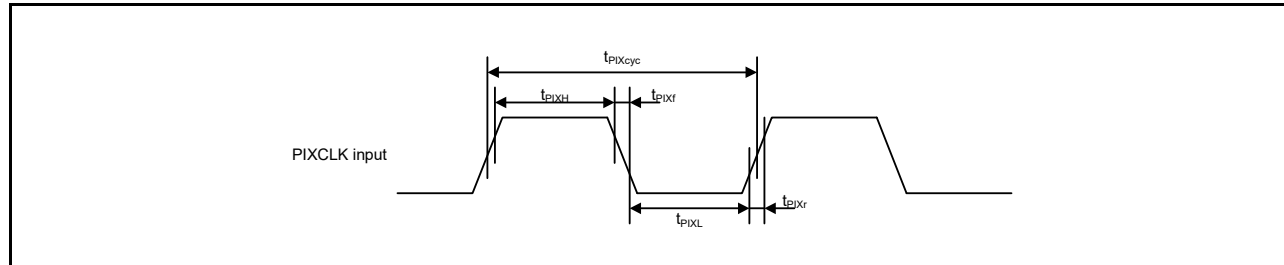
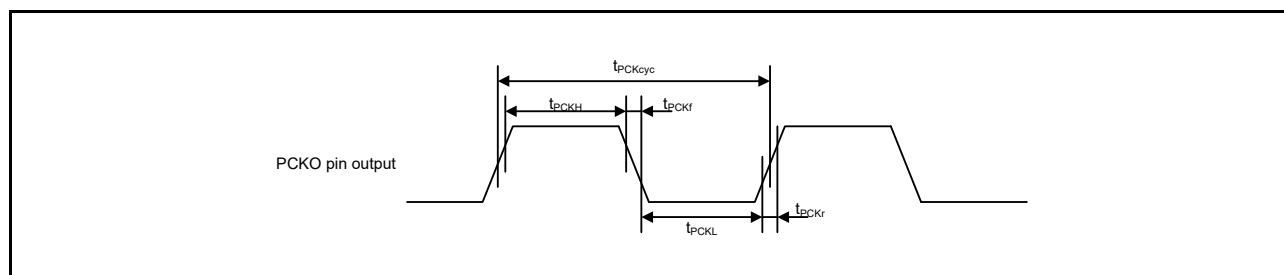
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

Table 5.42 PDC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	—	ns	Figure 5.66
	PIXCLK input high pulse width	t_{PIXH}	10	—	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	—	ns	
	PIXCLK rising time	t_{PIXr}	—	5	ns	
	PIXCLK falling time	t_{PIXf}	—	5	ns	
	PCKO output cycle time	t_{PCKcyc}	$2 \times t_{PBcyc}$	—	ns	Figure 5.67
	PCKO output high pulse width	t_{PCKH}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	—	ns	
	PCKO output low pulse width	t_{PCKL}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	—	ns	
	PCKO rising time	t_{PCKr}	—	5	ns	
	PCKO falling time	t_{PCKf}	—	5	ns	
	VSYNC/HSYNC input setup time	t_{SYNCS}	10	—	ns	Figure 5.68
	VSYNC/HSYNC input hold time	t_{SYNCH}	5	—	ns	
	PIXD input setup time	t_{PIXDS}	10	—	ns	
	PIXD input hold time	t_{PIXDH}	5	—	ns	

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.66 PDC Input Clock Timing****Figure 5.67 PDC Output Clock Timing**

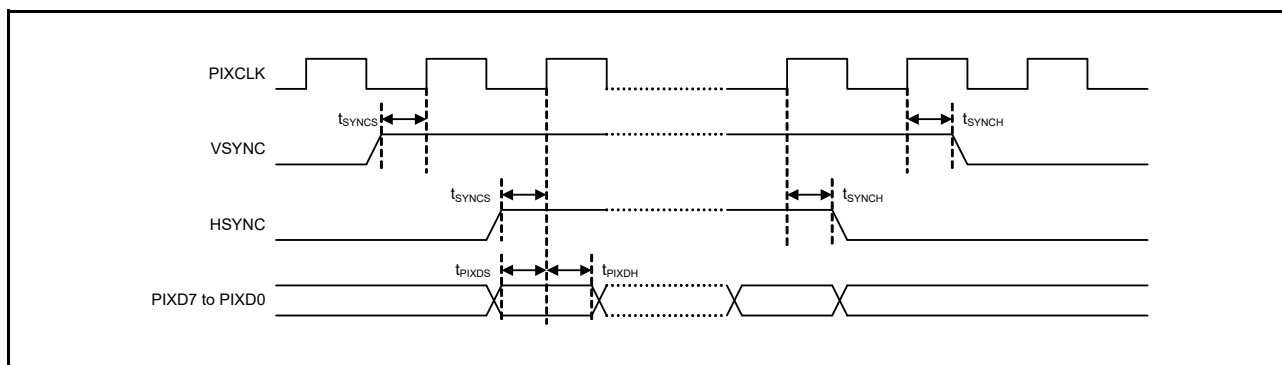


Figure 5.68 PDC AC Timing

Table 5.43 GLCDC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD_EXTCLK Input clock frequency	$t_{E_{cyc}}$	—	—	30*1	MHz	Figure 5.69
LCD_EXTCLK Input clock Low pulse width	t_{WL}	0.45	—	0.55	$t_{E_{cyc}}$	
LCD_EXTCLK Input clock High pulse width	t_{WH}	0.45	—	0.55	$t_{E_{cyc}}$	
LCD_CLK Output clock frequency	$t_{L_{cyc}}$	—	—	30*1	MHz	Figure 5.70
LCD_CLK Output clock Low pulse width	t_{LOL}	0.4	—	0.6	$t_{L_{cyc}}$	
LCD_CLK Output clock High pulse width	t_{LOH}	0.4	—	0.6	$t_{L_{cyc}}$	
LCD data output Delay timing	t_{DD}	-3.5*2	—	4*2	ns	Figure 5.71

Note 1. Parallel RGB888,666,565: Max. 27 MHz
 Serial RGB888: Max. 30 MHz (4x speed)

Note 2. We recommend using pins that have a letter ("A", "-B", etc) to indicate group membership appended to their names as groups.
 For the GLCDC interface, the AC portion of the electrical characteristics is measured for each group.
 If we use group "-A" and "-B" combination, "LCD data output Delay timing (t_{DD})" is Min = -5.0 ns, Max = 5.5 ns.

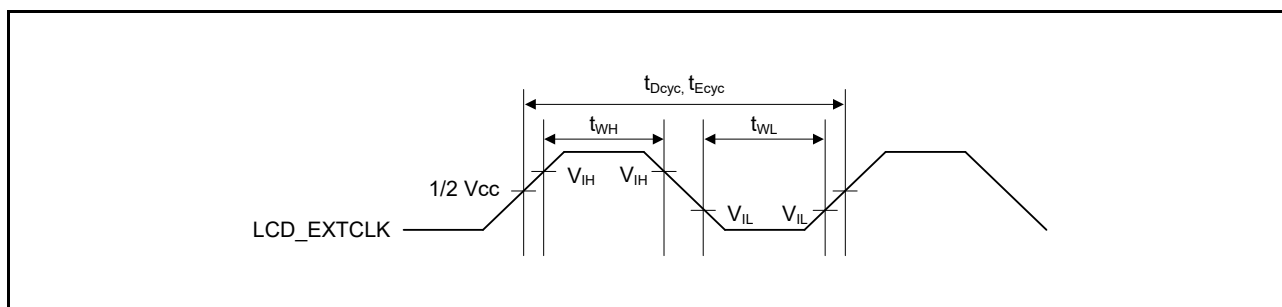


Figure 5.69 LCD_EXTCLK Clock Input Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

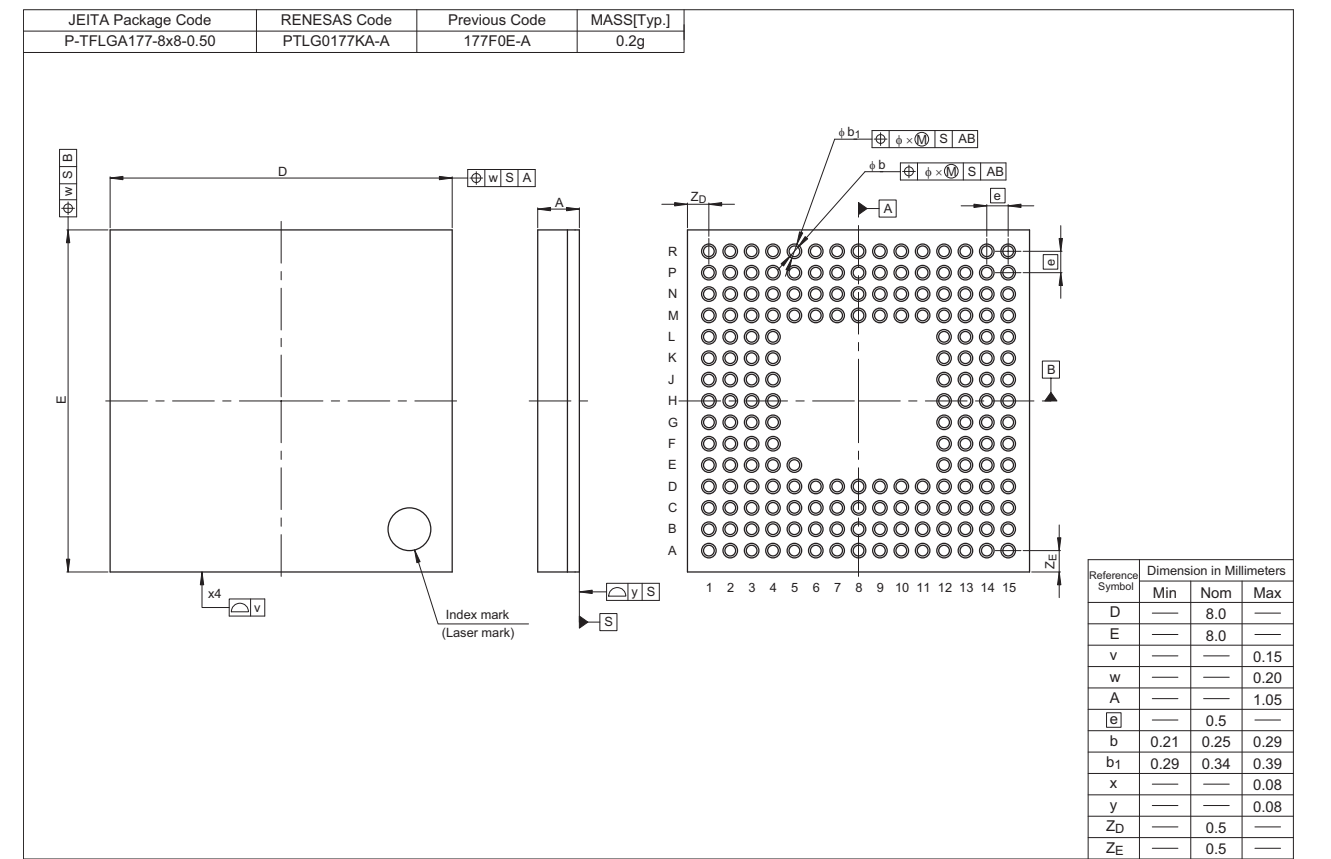


Figure A 177-Pin TFLGA (PTLG0177KA-A)

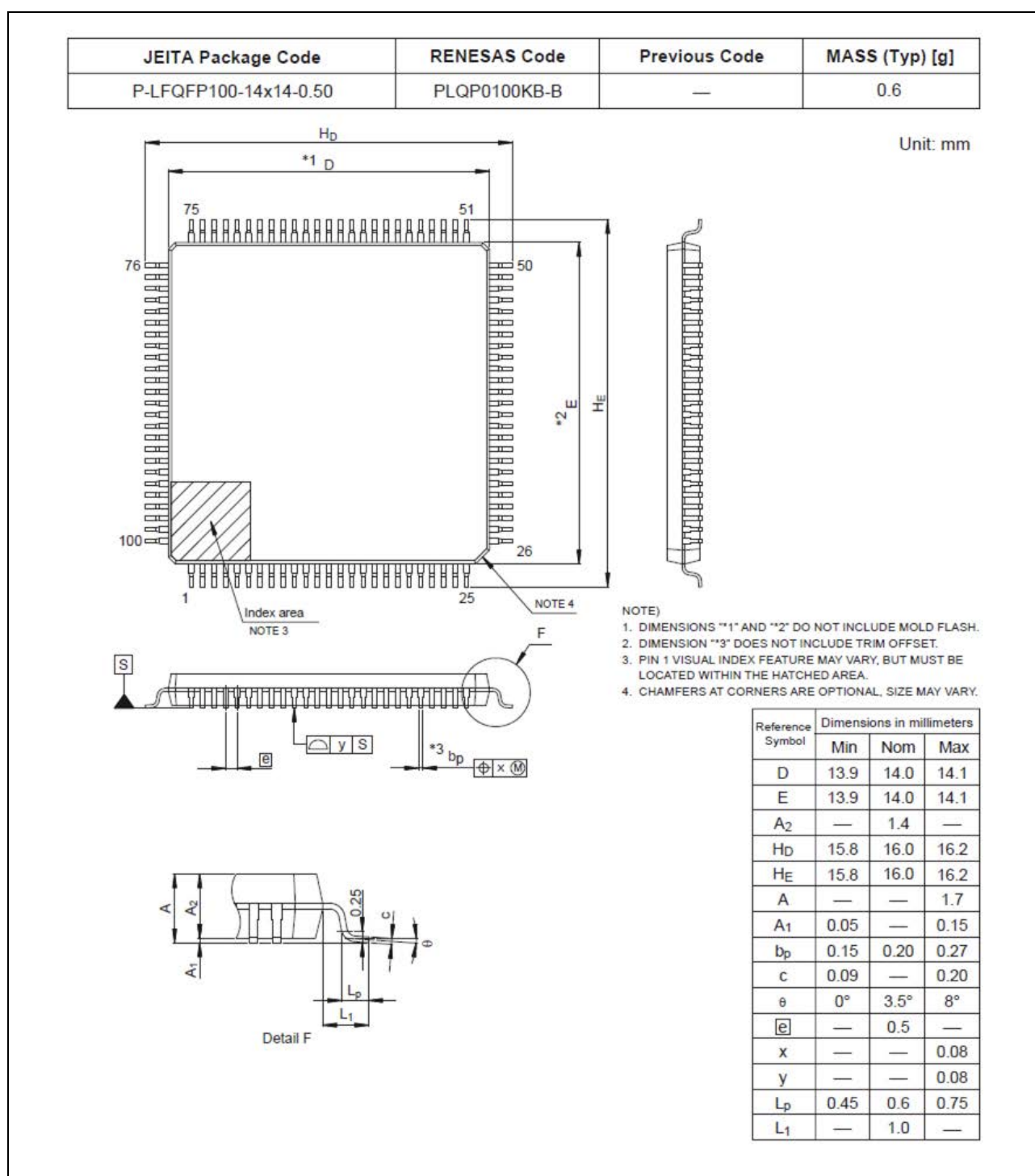


Figure G 100-Pin LFQFP (PLQP0100KB-B)

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