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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56514edfp-30

Table 1.3 List of Products (8/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (G version)	R5F56517EGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F56517FGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F56514AGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F56514BGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F56514EGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F56514FGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F5651EDGFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F5651EHGFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F5651CDGFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F5651CHGFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F56519AGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F56519BGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F56519EGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F56519FGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F56517AGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F56517BGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F56517EGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F56517FGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F56514AGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F56514BGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F56514EGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F56514FGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105

Note 1. In planning

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B/ RSPCKC-A/RSPCKC-B	I/O	Clock input/output pin
	MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B/ MOSIC-A/MOSIC-B	I/O	Inputs or outputs data output from the master
	MISOA-A/MISOA-B/ MISOB-A/MISOB-B/ MISOC-A/MISOC-B	I/O	Inputs or outputs data output from the slave
	SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B/ SSLC0-A/SSLC0-B	I/O	Input or output pin for slave selection
	SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B/ SSLC1-A/SSLC1-B, SSLA2-A/SSLA2-B/ SSLB2-A/SSLB2-B/ SSLC2-A/SSLC2-B, SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B/ SSLC3-A/SSLC3-B	Output	Output pin for slave selection
Quad serial peripheral interface	QSPCLK-A/QSPCLK-B	Output	QSPI clock output pin
	QSSL-A/QSSL-B	Output	QSPI slave output pin
	QMO-A/QMO-B, QIO0-A/QIO0-B	I/O	Master transmit data/data 0
	QMI-A/QMI-B, QIO1-A/QIO1-B	I/O	Master input data/data 1
	QIO2-A/QIO2-B, QIO3-A/QIO3-B	I/O	Data 2, data 3
MMC host interface	MMC_CLK-A/ MMC_CLK-B	Output	MMC clock pin
	MMC_CMD-A/ MMC_CMD-B	I/O	Command/response pin
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pin
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pin
SD host interface	SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C to SDHI_D0-A/ SDHI_D0-B/SDHI_D1-C	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
SD slave interface	SDSI_CLK-A/SDSI_CLK-B	Input	SD clock input pin
	SDSI_CMD-A/SDSI_CMD-B	I/O	SD command input, response output signal pin
	SDSI_D3-A/SDSI_D3-B, SDSI_D2-A/SDSI_D2-B, SDSI_D1-A/SDSI_D1-B, SDSI_D0-A/SDSI_D0-B	I/O	SD data bus pins

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61	RX65N Group, RX651 Group PTBG0176GA-A (176-Pin LFBGA) (Upper Perspective View)							P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_USB	USB0_DP	6
5	P46	P47	P45	P44								PJ2	P12	VCC_USB	USB0_DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (13 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 79F1h	ICU	Software Configurable Interrupt A Source Select Register 241	SLIAR241	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F2h	ICU	Software Configurable Interrupt A Source Select Register 242	SLIAR242	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F3h	ICU	Software Configurable Interrupt A Source Select Register 243	SLIAR243	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F4h	ICU	Software Configurable Interrupt A Source Select Register 244	SLIAR244	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F5h	ICU	Software Configurable Interrupt A Source Select Register 245	SLIAR245	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F6h	ICU	Software Configurable Interrupt A Source Select Register 246	SLIAR246	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F7h	ICU	Software Configurable Interrupt A Source Select Register 247	SLIAR247	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F8h	ICU	Software Configurable Interrupt A Source Select Register 248	SLIAR248	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F9h	ICU	Software Configurable Interrupt A Source Select Register 249	SLIAR249	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FAh	ICU	Software Configurable Interrupt A Source Select Register 250	SLIAR250	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FBh	ICU	Software Configurable Interrupt A Source Select Register 251	SLIAR251	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FCh	ICU	Software Configurable Interrupt A Source Select Register 252	SLIAR252	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FDh	ICU	Software Configurable Interrupt A Source Select Register 253	SLIAR253	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FEh	ICU	Software Configurable Interrupt A Source Select Register 254	SLIAR254	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FFh	ICU	Software Configurable Interrupt A Source Select Register 255	SLIAR255	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7A00h	ICU	Software Configurable Interrupt Source Select Register Write Protect Register	SLIPRCR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 7A01h	ICU	EXDMAC Trigger Select Register	SELEXDR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSMPR	8	8	2, 3 PCLKB	2 ICLK	IWDTa

Table 4.1 List of I/O Registers (Address Order) (25 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A046h	SMCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A049h	SCI2	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Ah	SCI2	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Bh	SCI2	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Ch	SCI2	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Eh	SCI2	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Fh	SCI2	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Eh	SCI2	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A050h	SCI2	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A051h	SCI2	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A050h	SCI2	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A052h	SCI2	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A066h	SMCI3	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli

Table 4.1 List of I/O Registers (Address Order) (32 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A132h	SCI9	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 AC00h	SDHI	Command Register	SDCMD	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC08h	SDHI	Argument Register	SDARG	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC10h	SDHI	Data Stop Register	SDSTOP	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC14h	SDHI	Block Count Register	SDBLKCNT	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC18h	SDHI	Response Register 10	SDRSP10	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC20h	SDHI	Response Register 32	SDRSP32	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC28h	SDHI	Response Register 54	SDRSP54	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC30h	SDHI	Response Register 76	SDRSP76	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC38h	SDHI	SD Status Register 1	SDSTS1	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC3Ch	SDHI	SD Status Register 2	SDSTS2	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC40h	SDHI	SD Interrupt Mask Register 1	SDIMSK1	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC44h	SDHI	SD Interrupt Mask Register 2	SDIMSK2	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC48h	SDHI	SDHI Clock Control Register	SDCLKCR	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC4Ch	SDHI	Transfer Data Size Register	SDSIZE	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC50h	SDHI	Card Access Option Register	SDOPT	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC58h	SDHI	SD Error Status Register 1	SDERSTS1	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC5Ch	SDHI	SD Error Status Register 2	SDERSTS2	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC60h	SDHI	SD Buffer Register	SDBUFR	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC68h	SDHI	SDIO Mode Control Register	SDIOMD	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC6Ch	SDHI	SDIO Status Register	SDIOSTS	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 AC70h	SDHI	SDIO Interrupt Mask Register	SDIOIMSK	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 ADB0h	SDHI	DMA Transfer Enable Register	SDDMAEN	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 ADC0h	SDHI	SDHI Software Reset Register	SDRST	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 ADC4h	SDHI	Version Register	SDVER	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 ADE0h	SDHI	Swap Control Register	SDSWAP	32	32	2, 3 PCLKB	2 ICLK	SDHI
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2, 3 PCLKB	2 ICLK	DOC
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2, 3 PCLKB	2 ICLK	DOC
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2, 3 PCLKB	2 ICLK	DOC
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B101h	ELC	Event Link Setting Register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Ch	ELC	Event Link Setting Register 11	ELSR11	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Eh	ELC	Event Link Setting Register 13	ELSR13	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK	ELC

Table 4.1 List of I/O Registers (Address Order) (38 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C0C1h	PORT1	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C2h	PORT2	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C3h	PORT3	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C4h	PORT4	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C5h	PORT5	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C6h	PORT6	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C7h	PORT7	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C8h	PORT8	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C9h	PORT9	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CAh	PORTA	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CBh	PORTB	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CCh	PORTC	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CDh	PORTD	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CEh	PORTE	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CFh	PORTF	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0D0h	PORTG	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0D2h	PORTJ	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0F0h	PORTG	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC

Table 4.1 List of I/O Registers (Address Order) (52 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1290h	MTU0	Noise Filter Control Register 0	NFCR0	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1291h	MTU1	Noise Filter Control Register 1	NFCR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1292h	MTU2	Noise Filter Control Register 2	NFCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1293h	MTU3	Noise Filter Control Register 3	NFCR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1294h	MTU4	Noise Filter Control Register 4	NFCR4	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1298h	MTU8	Noise Filter Control Register 8	NFCR8	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1299h	MTU0	Noise Filter Control Register C	NFCRC	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1300h	MTU0	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1308h	MTU0	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1320h	MTU0	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1328h	MTU0	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1380h	MTU1	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1388h	MTU1	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1391h	MTU1	Timer Mode Register 3	TMDR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1394h	MTU1	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A0h	MTU1	Timer Longword Counter	TCNTLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A4h	MTU1	Timer Longword General Register	TGRALW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A8h	MTU1	Timer Longword General Register	TGRBLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1400h	MTU2	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (59 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 1300h	GLCDC	Gamma Correction G Block Register Update Control Register	GAMGVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1304h	GLCDC	Gamma Correction Block Function Switch Register	GAMSW	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1308h	GLCDC	Gamma Correction G Table Setting Register 1	GAMGLUT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 130Ch	GLCDC	Gamma Correction G Table Setting Register 2	GAMGLUT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1310h	GLCDC	Gamma Correction G Table Setting Register 3	GAMGLUT3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1314h	GLCDC	Gamma Correction G Table Setting Register 4	GAMGLUT4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1318h	GLCDC	Gamma Correction G Table Setting Register 5	GAMGLUT5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 131Ch	GLCDC	Gamma Correction G Table Setting Register 6	GAMGLUT6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1320h	GLCDC	Gamma Correction G Table Setting Register 7	GAMGLUT7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1324h	GLCDC	Gamma Correction G Table Setting Register 8	GAMGLUT8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1328h	GLCDC	Gamma Correction G Area Setting Register 1	GAMGAREA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 132Ch	GLCDC	Gamma Correction G Area Setting Register 2	GAMGAREA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1330h	GLCDC	Gamma Correction G Area Setting Register 3	GAMGAREA3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1334h	GLCDC	Gamma Correction G Area Setting Register 4	GAMGAREA4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1338h	GLCDC	Gamma Correction G Area Setting Register 5	GAMGAREA5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1340h	GLCDC	Gamma Correction B Block Register Update Control Register	GAMBVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1348h	GLCDC	Gamma Correction B Table Setting Register 1	GAMBLUT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 134Ch	GLCDC	Gamma Correction B Table Setting Register 2	GAMBLUT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1350h	GLCDC	Gamma Correction B Table Setting Register 3	GAMBLUT3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1354h	GLCDC	Gamma Correction B Table Setting Register 4	GAMBLUT4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1358h	GLCDC	Gamma Correction B Table Setting Register 5	GAMBLUT5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 135Ch	GLCDC	Gamma Correction B Table Setting Register 6	GAMBLUT6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1360h	GLCDC	Gamma Correction B Table Setting Register 7	GAMBLUT7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1364h	GLCDC	Gamma Correction B Table Setting Register 8	GAMBLUT8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1368h	GLCDC	Gamma Correction B Area Setting Register 1	GAMBAREA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 136Ch	GLCDC	Gamma Correction B Area Setting Register 2	GAMBAREA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1370h	GLCDC	Gamma Correction B Area Setting Register 3	GAMBAREA3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1374h	GLCDC	Gamma Correction B Area Setting Register 4	GAMBAREA4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1378h	GLCDC	Gamma Correction B Area Setting Register 5	GAMBAREA5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1380h	GLCDC	Gamma Correction R Block Register Update Control Register	GAMRVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1388h	GLCDC	Gamma Correction R Table Setting Register 1	GAMRLUT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 138Ch	GLCDC	Gamma Correction R Table Setting Register 2	GAMRLUT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1390h	GLCDC	Gamma Correction R Table Setting Register 3	GAMRLUT3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1394h	GLCDC	Gamma Correction R Table Setting Register 4	GAMRLUT4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1398h	GLCDC	Gamma Correction R Table Setting Register 5	GAMRLUT5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 139Ch	GLCDC	Gamma Correction R Table Setting Register 6	GAMRLUT6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13A0h	GLCDC	Gamma Correction R Table Setting Register 7	GAMRLUT7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13A4h	GLCDC	Gamma Correction R Table Setting Register 8	GAMRLUT8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13A8h	GLCDC	Gamma Correction R Area Setting Register 1	GAMRAREA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13ACh	GLCDC	Gamma Correction R Area Setting Register 2	GAMRAREA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13B0h	GLCDC	Gamma Correction R Area Setting Register 3	GAMRAREA3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13B4h	GLCDC	Gamma Correction R Area Setting Register 4	GAMRAREA4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13B8h	GLCDC	Gamma Correction R Area Setting Register 5	GAMRAREA5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13C0h	GLCDC	Output Control Block Register Update Control Register	OUTVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13C4h	GLCDC	Output Interface Register	OUTSET	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13C8h	GLCDC	Brightness Adjustment Register 1	BRIGHT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13CCh	GLCDC	Brightness Adjustment Register 2	BRIGHT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC

Table 5.4 DC Characteristics (2)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

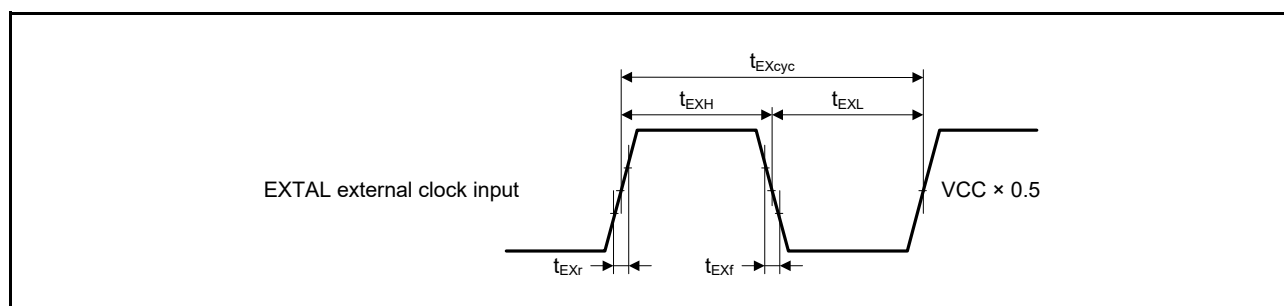
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V _{OH}	VCC – 0.5	—	—	V	I _{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V _{OL}	—	—	0.5	V	I _{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I _{OL} = 3.0 mA
			—	—	0.6		I _{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V _{OL}	—	—	0.4	V	I _{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I _{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V _{OL}	—	—	0.4	V	I _{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	I _{in}	—	—	1.0	μA	V _{in} = 0 V V _{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	I _{TSI}	—	—	1.0	μA	V _{in} = 0 V V _{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V _{in} = 0 V V _{in} = 5.5 V
Input pull-up MOS current	Other than P35	I _p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V _{in} = 0 V
Input pull-down MOS current	EMLE, BSCANP	I _p	10	—	300	μA	V _{in} = VCC
Input capacitance	All input pins (except for ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM)	C _{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T _a = 25°C
	Ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM		—	—	16		

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when $V_{in} = 0$ V.

Table 5.15 EXTAL Clock Timing

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

**Figure 5.4 EXTAL External Clock Input Timing****Table 5.16 Main Clock Timing**

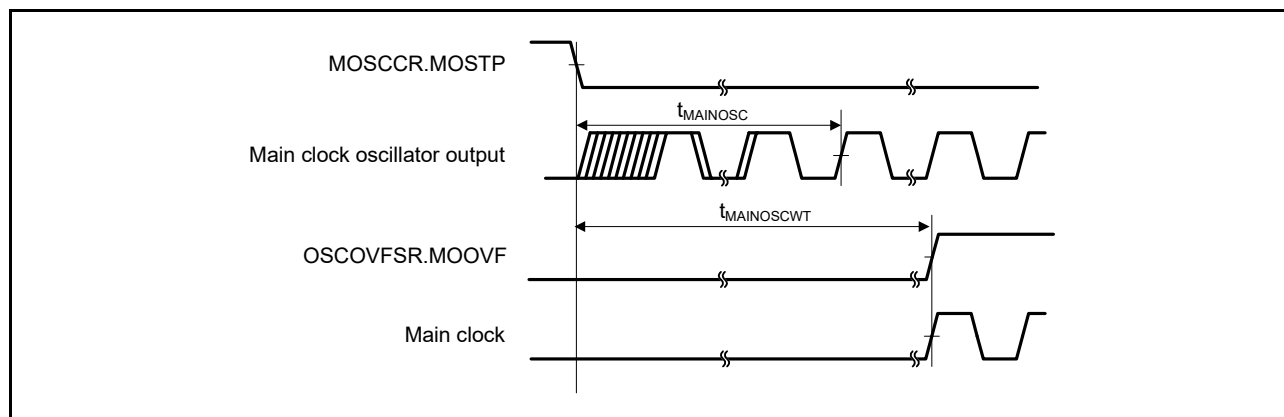
Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	Figure 5.5
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCW}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

$$t_{MAINOSCW} = [(MSTS[7:0] \text{ bits} \times 32) + 10] / f_{LOCO}$$

**Figure 5.5 Main Clock Oscillation Start Timing**

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.21 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq VREFH0 \leq AVCC0$,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}^{*2}$	t_{SBYSEQ}^{*3}		
Recovery time after cancellation of software standby mode*1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	$\{(MSTS[7:0] \text{ bit} \times 32) + 76\} / 0.216$	$100 + 7 / f_{ICLK} + 2n / f_{MAIN}$	μs	Figure 5.12
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			$\{(MSTS[7:0] \text{ bit} \times 32) + 138\} / 0.216$	$100 + 7 / f_{ICLK} + 2n / f_{PLL}$		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	$100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}$		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	$100 + 7 / f_{ICLK} + 2n / f_{PLL}$		
	Sub-clock oscillator operating		t_{SBYSC}			$\{(SSTS[7:0] \text{ bit} \times 16384) + 13\} / 0.216 + 10 / f_{FCLK}$	$100 + 4 / f_{ICLK} + 2n / f_{SUE}$		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	$100 + 7 / f_{ICLK} + 2n / f_{HOCO}$		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	$100 + 7 / f_{ICLK} + 2n / f_{PLL}$		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	$100 + 7 / f_{ICLK} + 2n / f_{LOCO}$		

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).

Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.

Note 3. For n, the greatest value is selected from among the internal clock division settings.

Note 4. This condition applies when $f_{ICLK}:f_{FCLK} = 1:1$, $2:1$, or $4:1$.

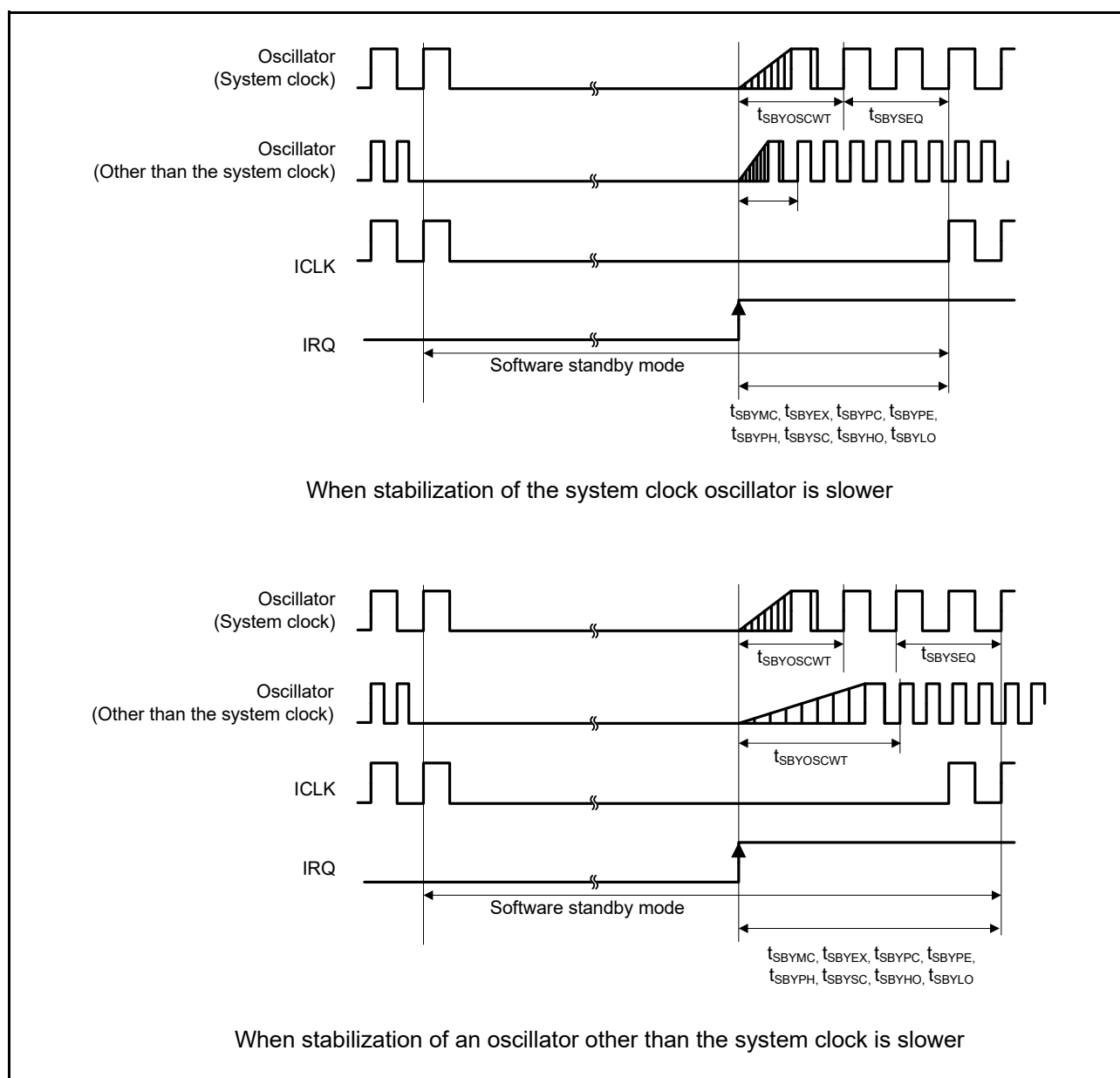


Figure 5.12 Software Standby Mode Cancellation Timing

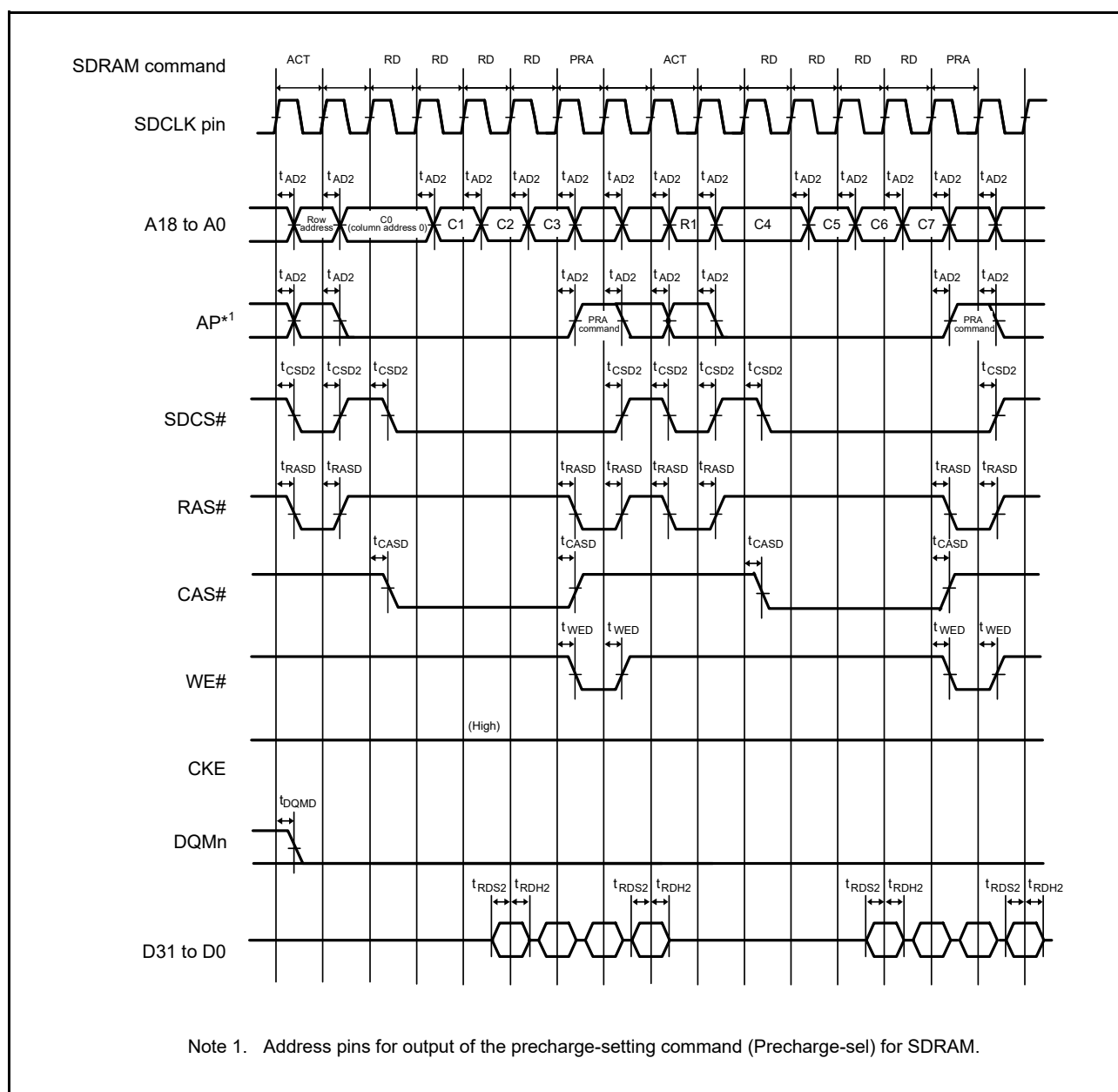
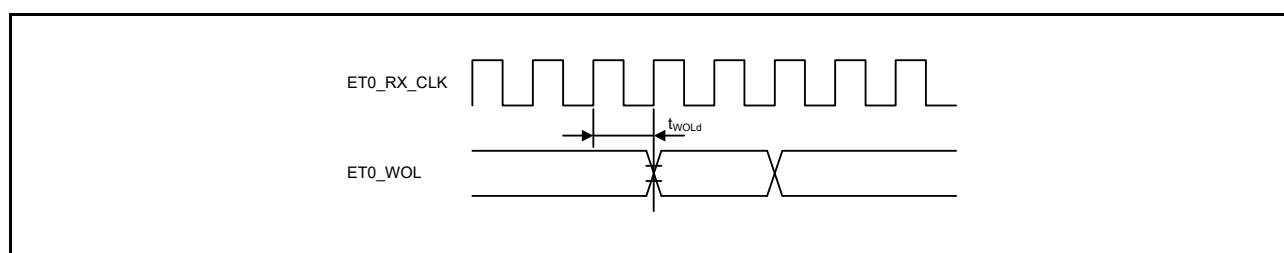


Figure 5.27 SDRAM Space Multiple Read Line Stride Bus Timing

**Figure 5.65 WOL Output Timing (MII)**

5.6 D/A Conversion Characteristics

Table 5.49 D/A Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	12	12	12	Bit	
Unbuffered output	Absolute accuracy	—	—	—	± 6.0	LSB	2-M Ω resistive load 10-bit conversion
	Differential nonlinearity error	DNL	—	± 1.0	± 2.0	LSB	2-M Ω resistive load
	Output resistance	R_O	—	8.6	—	k Ω	
	Setting time	t_s	—	—	3	μ s	20-pF capacitive load
Buffered output	Load resistance	R_L	5	—	—	k Ω	
	Load capacitance	C_L	—	—	50	pF	
	Output voltage	V_O	0.2	—	$AVCC1 - 0.2$	V	
	Differential nonlinearity error	DNL	—	± 1.0	± 2.0	LSB	
	Integral nonlinearity error	INL	—	± 2.0	± 4.0	LSB	
	Setting time	t_s	—	—	4	μ s	

5.7 Temperature Sensor Characteristics

Table 5.50 Temperature Sensor Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	± 1	—	$^{\circ}$ C	
Temperature slope	—	4	—	mV/ $^{\circ}$ C	
Output voltage (at 25 $^{\circ}$ C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	μ s	
Sampling time*1	4.15	—	—	μ s	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

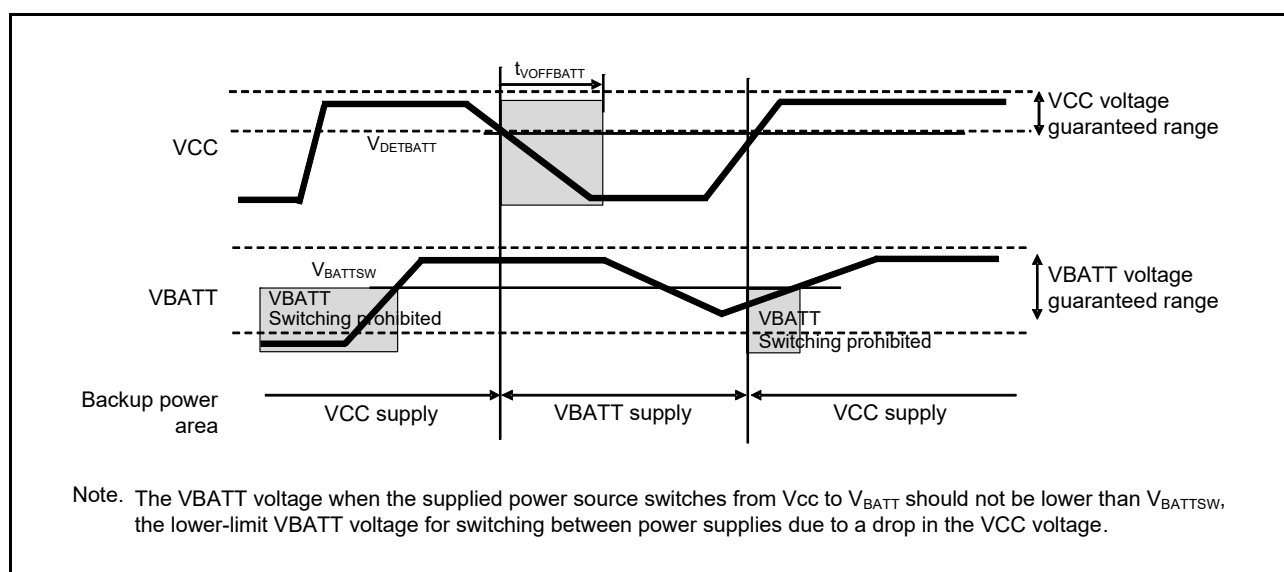
5.10 Battery Backup Function Characteristics

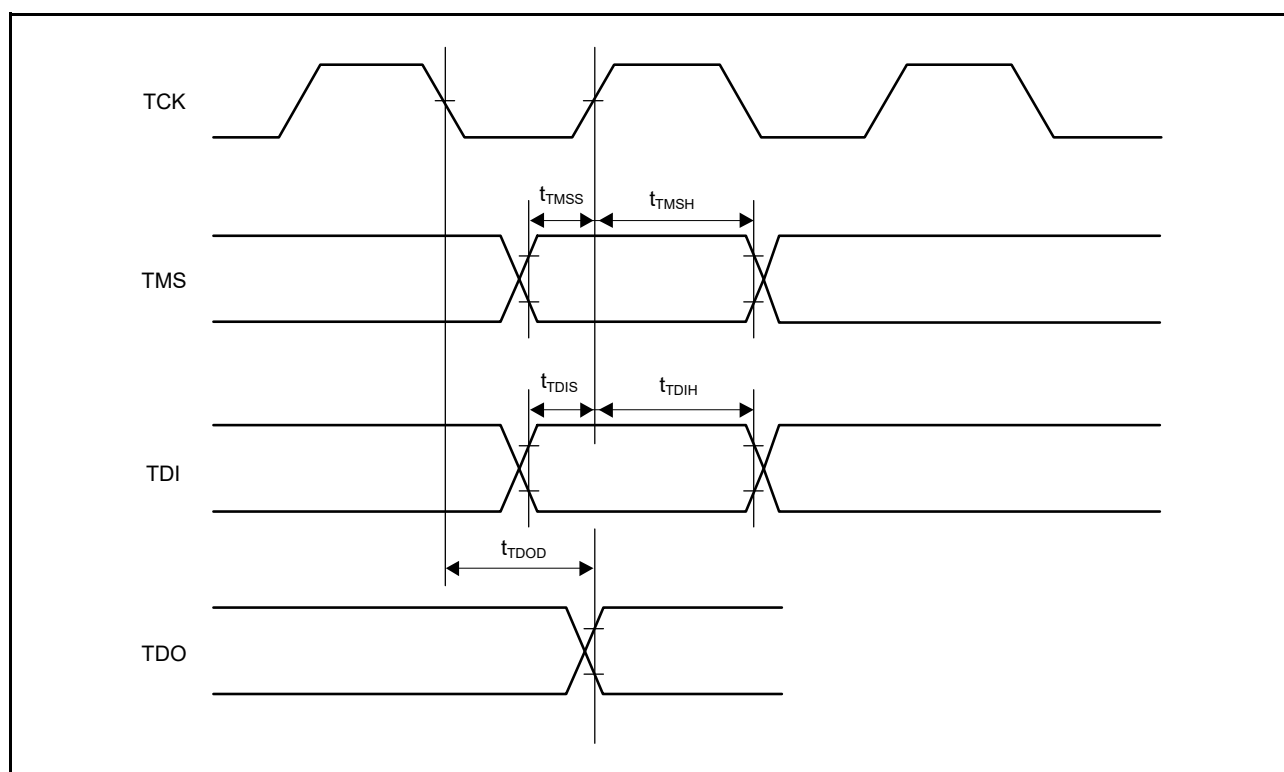
Table 5.53 Battery Backup Function Characteristics

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $V_{BATT} = 2.0$ to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 5.81
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—	—	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	μ s	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

**Figure 5.81 Battery Backup Function Characteristics**

**Figure 5.85** Boundary Scan Input/Output Timing

REVISION HISTORY	RX65N Group, RX651 Group Datasheet
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Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Aug 24, 2016	—	First edition, issued	
2.10	Oct 02, 2017	—	Products with at least 1.5 Mbytes of code flash memory added The conventional products indicated as "products with 1 Mbyte of code flash memory or less"	
		1. Overview		
		6, 9	Table 1.1 Outline of Specifications (5/9), Note added	TN-RX*-A164B/E
		8	Table 1.1 Outline of Specifications (8/9) Description of the 12-bit D/A converter (R12DA) changed	TN-RX*-A165A/E
		4. I/O Registers		
		131	Table 4.1 List of I/O Registers (Address Order) (46 / 61), changed	TN-RX*-A176A/E
		5. Electrical Characteristics		
		147	Table 5.1 Absolute Maximum Rating, changed	
		150	Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed	TN-RX*-A164B/E
		152	Table 5.7 DC Characteristics (4), changed	TN-RX*-A164B/E TN-RX*-A176A/E
		153	Table 5.9 Heat Resistance Value (Reference), added	
		162	Table 5.21 Timing of Recovery from Low Power Consumption Modes (1), changed	TN-RX*-A176A/E
		189	Table 5.35 RSPI Timing, changed	
		212	Table 5.49 D/A Conversion Characteristics, changed	TN-RX*-A165A/E
		218	Table 5.54 Code Flash Memory Characteristics, changed	
		219	Table 5.55 Data Flash Memory Characteristics, changed	

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