Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56517adfp-30

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.

Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, see Table 1.2, Code Flash Memory Capacity and Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	• Capacity: 512 Kbytes/768 Kbytes/1 Mbyte/1.5 Mbytes/2 Mbytes • 50 MHz ≤ No-wait cycle access 100 MHz ≤ 1-wait cycle access 100 MHz ≥ 2-wait cycle access • Instructions hitting the ROM cache or operand = 120 MHz: No-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode) • Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. • A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	• Capacity: 32 Kbytes • Programming/erasing: 100,000 times
	RAM	• Capacity: 256 Kbytes (Products with 1 Mbyte of code flash memory or less) RAM: 256 Kbytes • Capacity: 640 Kbytes (Products with at least 1.5 Mbytes of code flash memory) RAM: 256 Kbytes Expansion RAM: 384 Kbytes • 120 MHz, no-wait access
	Standby RAM	• Capacity: 8 Kbytes • Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Timers	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)*4	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
Communication function	Ethernet controller (ETHERC)	• Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a “wake-on-LAN” signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards
	DMA controller for Ethernet controller (EDMACa)	• Alleviation of CPU load by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 FS host/ function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus power are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required

Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (1/2)

Functions	Products	Products with 1 Mbyte of code flash memory or less		Products with at least 1.5 Mbytes of code flash memory		
	Package	145 Pins, 144 Pins	100 Pins	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
Code Flash Memory	Code Flash Memory Capacity	512 Kbytes/768 Kbytes /1 Mbyte		1.5 Mbytes/2 Mbytes		
	Dual bank function	Not available		Available		
	BGO function	Not available		Available		
Data Flash Memory		Not available		32 Kbytes		
RAM		256 Kbytes		640 Kbytes (256 Kbytes + 384 Kbytes of expansion RAM)		
External bus	External bus width	16/8 bits		32/16/8 bits	16/8 bits	
	SDRAM area controller	Available	Not available	Available		Not available
DMA	DMA controller	Ch. 0 to 7				
	Data transfer controller	Available				
	EXDMA controller	Ch. 0 and 1				
Timers	16-bit timer pulse unit	Ch. 0 to 5				
	Multi-function timer pulse unit 3	Ch. 0 to 8				
	Port output enable 3	Available				
	Programmable pulse generator	Ch. 0 and 1				
	8-bit timers	Ch. 0 to 3				
	Compare match timer	Ch. 0 to 3				
	Compare match timer W	Ch. 0 and 1				
	Realtime clock	Available				
	Watchdog timer	Available				
	Independent watchdog timer	Available				
Communication function	Ethernet controller	Ch. 0 (only for RX65N group)				
	DMA Controller for the Ethernet Controller	Ch. 0 (only for RX65N group)				
	USB 2.0 FS host/function module	Ch. 0				
	Serial communications interfaces (SCIg)	Ch. 0 to 9	Ch. 0 to 3, 5, 6, 8 and 9	Ch. 0 to 9		Ch. 0 to 3, 5, 6, 8 and 9
	Serial communications interfaces (SCIh)	Ch. 12				
	Serial communications interfaces (SCIi)	Ch. 10 and 11				
	I^2C bus interfaces	Ch. 0 and 2		Ch. 0 to 2		Ch. 0 and 2
	Serial peripheral interface	Ch. 0 to 2				
	CAN module	Ch. 0 and 1				
	Quad serial peripheral interface	Ch. 0				
	SD host interface	Available				
	SD slave interface	Available				
	MMC host interface	Available				
	Parallel data capture unit	Available	Not available	Available		Not available
Graphics	Graphic-LCD controller	Not available		Available		
	2D drawing engine	Not available		Available		

Table 1.3 List of Products (3/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N4EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N4FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565NEDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NEHDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565NCDDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NCHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565N9ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N9BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N9EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N9FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565N7ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N7BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N7EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N7FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565N4ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N4BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N4EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N4FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
RX65N (G version)	R5F565NEDGFC	PLQP0176KB-A *1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NEHGFC	PLQP0176KB-A *1	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565NCDGFC	PLQP0176KB-A *1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NCHGFC	PLQP0176KB-A *1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565NEDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NEHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565NCDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NCHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565N9AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F565N9BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F565N9EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F565N9FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105

Table 1.4 Pin Functions (3/8)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins
	TCLKA, TCLKB, TCLKC, TCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK9	I/O	Input/output pins for the clock
	RXD0 to RXD9	Input	Input pins for received data
	TXD0 to TXD9	Output	Output pins for transmitted data
	CTS0# to CTS9#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS9#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL9	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA9	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK9	I/O	Input/output pins for the clock
	SMISO0 to SMISO9	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI9	I/O	Input/output pins for master transmission of data
	SS0# to SS9#	Input	Chip-select input pins

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	RXD10 and RXD11	Input	Input pin for received data
	TXD10 and TXD11	Output	Output pin for transmitted data
	CTS10# and CTS11#	Input	Input pin for controlling the start of transmission and reception
	RTS10# and RTS11#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL10 and SSCL11	I/O	Input/output pin for the I^2C clock
	SSDA10 and SSDA11	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	SMISO10 and SMISO11	I/O	Input/output pin for slave transmission of data
	SMOSI10 and SMOSI11	I/O	Input/output pin for master transmission of data
	SS10# and SS11#	Input	Chip-select input pin
I^2C bus interface	SCL0[FM+], SCL1, SCL2, SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1, SDA2, SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

Table 1.4 Pin Functions (7/8)

Classifications	Pin Name	I/O	Description
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Graphic-LCD controller	LCD_CLK-A, LCD_CLK-B	Output	Panel clock output pin
	LCD_TCON3-A/ LCD_TCON3-B to LCD_TCON0-A/ LCD_TCON0-B	Output	Control signal output pin
	LCD_DATA23-A/ LCD_DATA23-B to LCD_DATA0-A/ LCD_DATA0-B	Output	LCD signal output pin
	LCD_EXTCLK-A, LCD_EXTCLK-B	Input	Panel clock source input pin
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN007, AN100 to AN120	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (1/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
1	AVSS0								
2		P05						IRQ13	DA1
3	AVCC1								
4		P03						IRQ11	DA0
5	AVSS1								
6		P02		TMCI1	SCK6			IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/ SSCL6			IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6			IRQ8	AN118
9		PF5						IRQ4	
10	EMLE								
11		PJ5		POE8#	CTS2#/RTS2#/ SS2#				
12	VSS								
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
14	VCL								
15	VBATT								
16	NC								
17	TRST#	PF4							
18	MD/FINED								
19	XCIN								
20	XCOUT								
21	RES#								
22	XTAL	P37							
23	VSS								
24	EXTAL	P36							
25	VCC								
26	UPSEL	P35						NMI	
27		P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
28		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0	PCKO		IRQ3-DS	
29		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC		IRQ2-DS	
30	TMS	PF3							
31	TDI	PF2			RXD1/SMISO1/ SSCL1				

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (1/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
1	AVCC1								
2	EMLE								
3	AVSS1								
4		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
5	VCL								
6	VBATT								
7	MD/FINED								
8	XCIN								
9	XCOUT								
10	RES#								
11	XTAL	P37							
12	VSS								
13	EXTAL	P36							
14	VCC								
15	UPSEL	P35						NMI	
16	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
17		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0			IRQ3-DS	
18		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN			IRQ2-DS	
19	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
20	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
21	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A				
22	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
23		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3				ADTRG0#
24		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN				
25		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#				

Table 4.1 List of I/O Registers (Address Order) (33 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B131h	ELC	Event Link Setting Register 33	ELSR33	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B133h	ELC	Event Link Setting Register 35	ELSR35	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B134h	ELC	Event Link Setting Register 36	ELSR36	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B135h	ELC	Event Link Setting Register 37	ELSR37	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B136h	ELC	Event Link Setting Register 38	ELSR38	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Dh	ELC	Event Link Setting Register 45	ELSR45	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Fh	ELC	Event Link Option Setting Register F	ELOPF	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B141h	ELC	Event Link Option Setting Register H	ELOPH	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIh

Table 4.1 List of I/O Registers (Address Order) (38 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C0C1h	PORT1	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C2h	PORT2	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C3h	PORT3	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C4h	PORT4	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C5h	PORT5	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C6h	PORT6	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C7h	PORT7	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C8h	PORT8	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C9h	PORT9	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CAh	PORTA	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CBh	PORTB	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CCh	PORTC	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CDh	PORTD	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CEh	PORTE	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CFh	PORTF	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0D0h	PORTG	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0D2h	PORTJ	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0F0h	PORTG	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC

Table 4.1 List of I/O Registers (Address Order) (60 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 13D0h	GLCDC	Contrast Adjustment Register	CONTRAST	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13D4h	GLCDC	Panel Dither Control Register	PANELDTHA	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13E4h	GLCDC	Output Phase Control Register	CLKPHASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1404h	GLCDC	Reference Timing Setting Register	TCONTIM	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1408h	GLCDC	Vertical Timing Setting Register A1	TCONSTVA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 140Ch	GLCDC	Vertical Timing Setting Register A2	TCONSTVA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1410h	GLCDC	Vertical Timing Setting Register B1	TCONSTVB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1414h	GLCDC	Vertical Timing Setting Register B2	TCONSTVB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1418h	GLCDC	Horizontal Timing Setting Register A1	TCONSTHA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 141Ch	GLCDC	Horizontal Timing Setting Register A2	TCONSTHA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1420h	GLCDC	Horizontal Timing Setting Register B1	TCONSTHB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1424h	GLCDC	Horizontal Timing Setting Register B2	TCONSTHB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1428h	GLCDC	Data Enable Polarity Setting Register	TCONDE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1440h	GLCDC	Status Detection Control Register	DTCTEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1444h	GLCDC	Interrupt Request Enable Control Register	INTEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1448h	GLCDC	Detected Status Clear Register	STCLR	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 144Ch	GLCDC	Detected Status Monitor Register	STMON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1450h	GLCDC	Panel Clock Control Register	PANELCLK	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 3000h	DRW2D	Geometry Control Register	CONTROL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3000h	DRW2D	Status Register	STATUS	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3004h	DRW2D	Surface Control Register	CONTROL2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3004h	DRW2D	Hardware Version Register	HWVER	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3010h	DRW2D	Limiter 1 Start Value Register	L1START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3014h	DRW2D	Limiter 2 Start Value Register	L2START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3018h	DRW2D	Limiter 3 Start Value Register	L3START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 301Ch	DRW2D	Limiter 4 Start Value Register	L4START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3020h	DRW2D	Limiter 5 Start Value Register	L5START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3024h	DRW2D	Limiter 6 Start Value Register	L6START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3028h	DRW2D	Limiter 1 X-Axis Increment Register	L1XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 302Ch	DRW2D	Limiter 2 X-Axis Increment Register	L2XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3030h	DRW2D	Limiter 3 X-Axis Increment Register	L3XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3034h	DRW2D	Limiter 4 X-Axis Increment Register	L4XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3038h	DRW2D	Limiter 5 X-Axis Increment Register	L5XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 303Ch	DRW2D	Limiter 6 X-Axis Increment Register	L6XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3040h	DRW2D	Limiter 1 Y-Axis Increment Register	L1YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3044h	DRW2D	Limiter 2 Y-Axis Increment Register	L2YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3048h	DRW2D	Limiter 3 Y-Axis Increment Register	L3YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 304Ch	DRW2D	Limiter 4 Y-Axis Increment Register	L4YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3050h	DRW2D	Limiter 5 Y-Axis Increment Register	L5YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3054h	DRW2D	Limiter 6 Y-Axis Increment Register	L6YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3058h	DRW2D	Limiter 1 Band Width Parameter Register	L1BAND	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 305Ch	DRW2D	Limiter 2 Band Width Parameter Register	L2BAND	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3064h	DRW2D	Base Color Register	COLOR1	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3068h	DRW2D	Secondary Color Register	COLOR2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3074h	DRW2D	Pattern Register	PATTERN	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3078h	DRW2D	Bounding Box Dimension Register	SIZE	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 307Ch	DRW2D	Frame Buffer Pitch Register	PITCH	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3080h	DRW2D	Frame Buffer Base Address Register	ORIGIN	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3090h	DRW2D	U Limiter Start Value Register	LUST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3094h	DRW2D	U Limiter X-Axis Increment Register	LUXADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D

Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.
Note 7. Reference value

Table 5.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item				Symbol	D version		G version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current*1	High-speed operating mode	Max.*2		I_{CC}*3	—	60	—	73	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz
		Normal	Peripheral function clock signal supplied*4		26	—	26	—		
			Peripheral function clock signal stopped*4		13	—	13	—		
		Core Mark	Peripheral function clock signal stopped*4		17	—	17	—		
		Sleep mode: The clock signal to peripheral modules is supplied*4			20	38	20	52		
		All-module-clock-stop mode (reference value)			9	26	9	39		
		Increased by BGO operation *7	Reading from the code flash memory while the data flash memory is being programmed		6	—	6	—		
			Reading from the code flash memory while the code flash memory is being programmed		7	—	7	—		
		Increased by Trusted Secure IP operation			—	12	—	12		
	Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4				1.6	—	1.6	—		All clocks 1 MHz
	Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4				1.6	—	1.6	—		All clocks 32.768 kHz
	Software standby mode				1.6	13	1.6	22.4		
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)			15.5	70	15.5	98	μA	
		Power not supplied to standby RAM and USB resume detecting unit (USB0 only)	Power-on reset circuit and low-power consumption function disabled*5		11.5	42	11.5	54		
			Power-on reset circuit and low-power consumption function enabled*6		4.9	32	4.9	47		
		Increased by RTC operation	When a low C_L crystal is in use		1	—	1	—		
			When a standard C_L crystal is in use		2	—	2	—		
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		0.9	—	0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					1.6	—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		1.7	—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					3.3	—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on returning from deep software standby mode		Inrush current*8	I_{RUSH}	—	130	—	130	mA	
			Energy of inrush current*8	E_{RUSH}	—	1.0	—	1.0	μC	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)
[D version]
I_{CC} Max. = 0.38 × f + 14 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.18 × f + 4 (ICLK 1 MHz max) (normal operation in high-speed operating mode)
I_{CC} Typ. = 0.4 × f + 1.2 (low-speed operating mode 1)
I_{CC} Max. = 0.2 × f + 14 (sleep mode)
[G version]

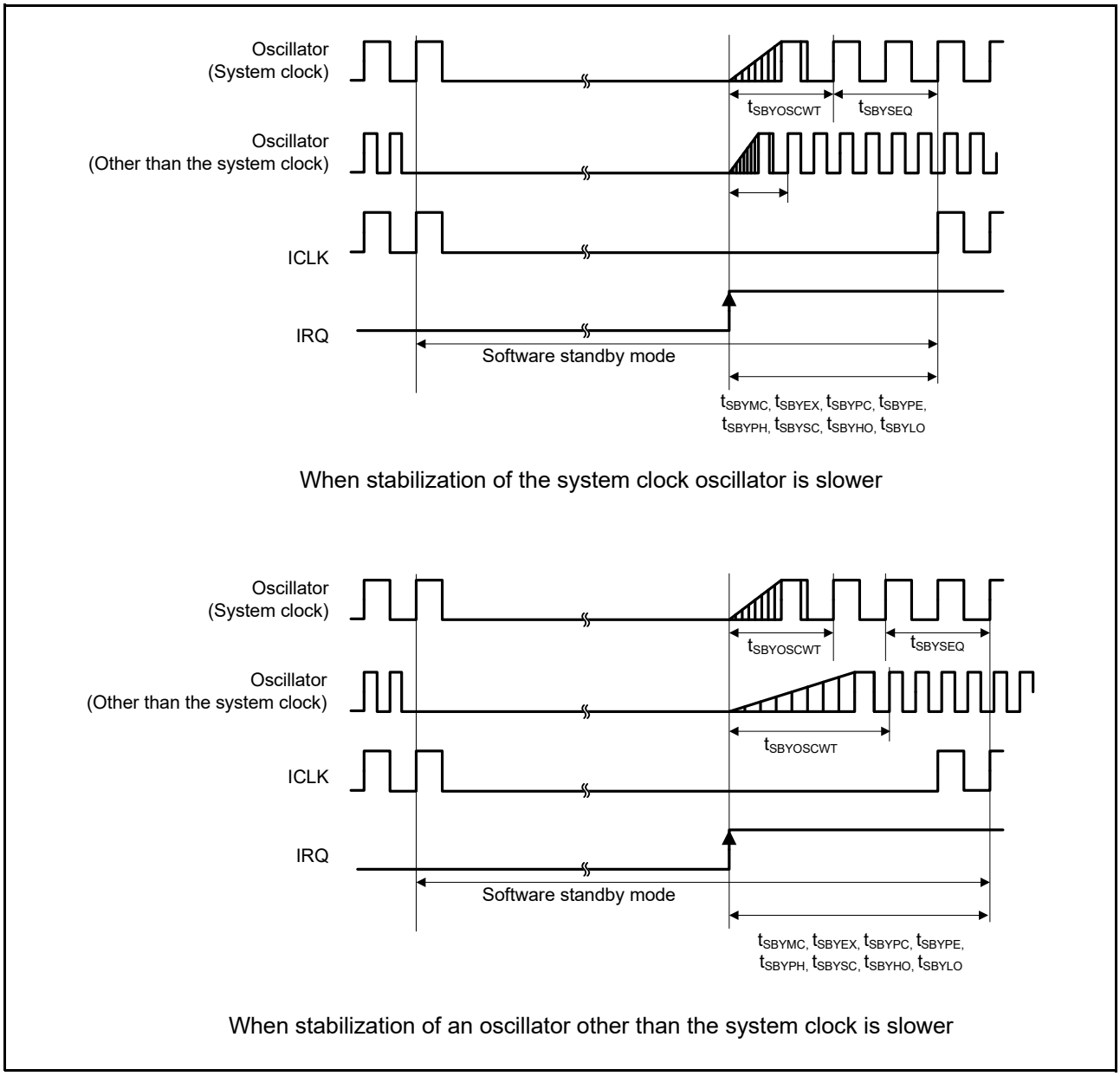


Figure 5.12 Software Standby Mode Cancellation Timing

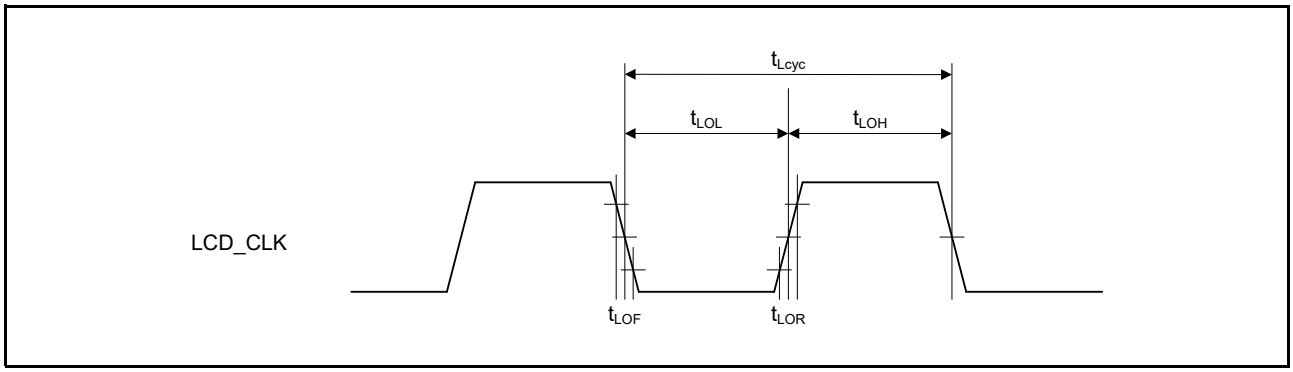


Figure 5.70 LCD_CLK Clock Output Timing

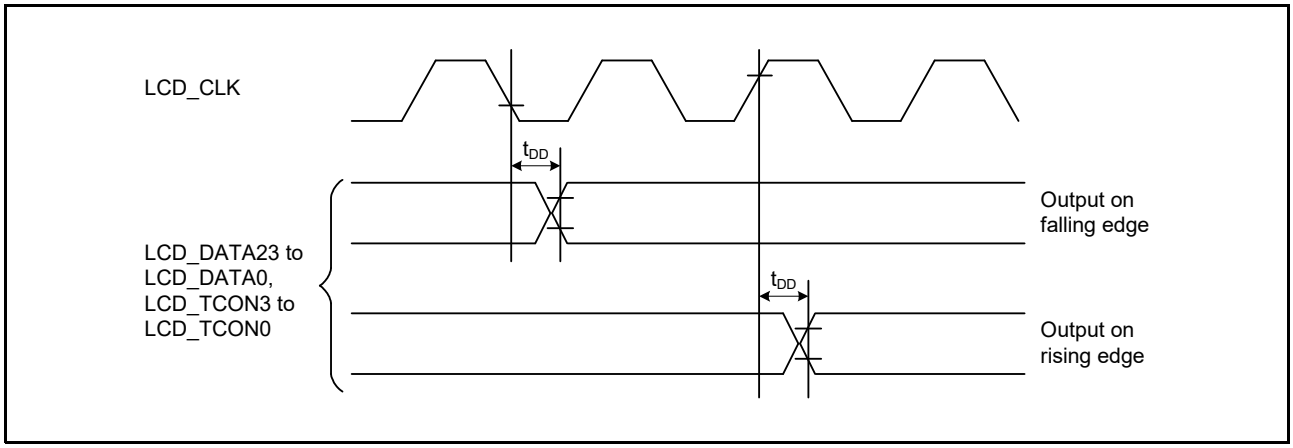


Figure 5.71 LCD Output Data Timing

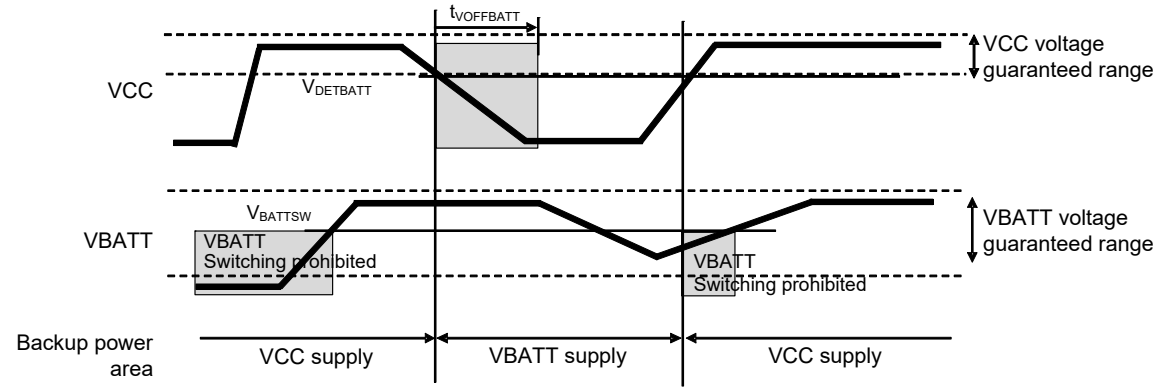
5.10 Battery Backup Function Characteristics

Table 5.53 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 5.81
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).



Note. The VBATT voltage when the supplied power source switches from Vcc to V_{BATT} should not be lower than V_{BATTSW}, the lower-limit VBATT voltage for switching between power supplies due to a drop in the VCC voltage.

Figure 5.81 Battery Backup Function Characteristics

Table 5.55 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.18	1.9	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.9	11	—	1.7	10	ms
	128 bytes	t_{DP128}	—	4.7	27	—	2.9	16	—	2.6	15	ms
	256 bytes	t_{DP256}	—	8.9	50	—	5.4	31	—	4.9	28	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	33	—	—	30	µs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	100000 *2	—	—	Times
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	132	—	—	120	µs
First suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	216	—	—	132	—	—	120	µs
	128 bytes	—	—	—	216	—	—	132	—	—	120	µs
	256 bytes	—	—	—	216	—	—	132	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Suspend delay time during erasing (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

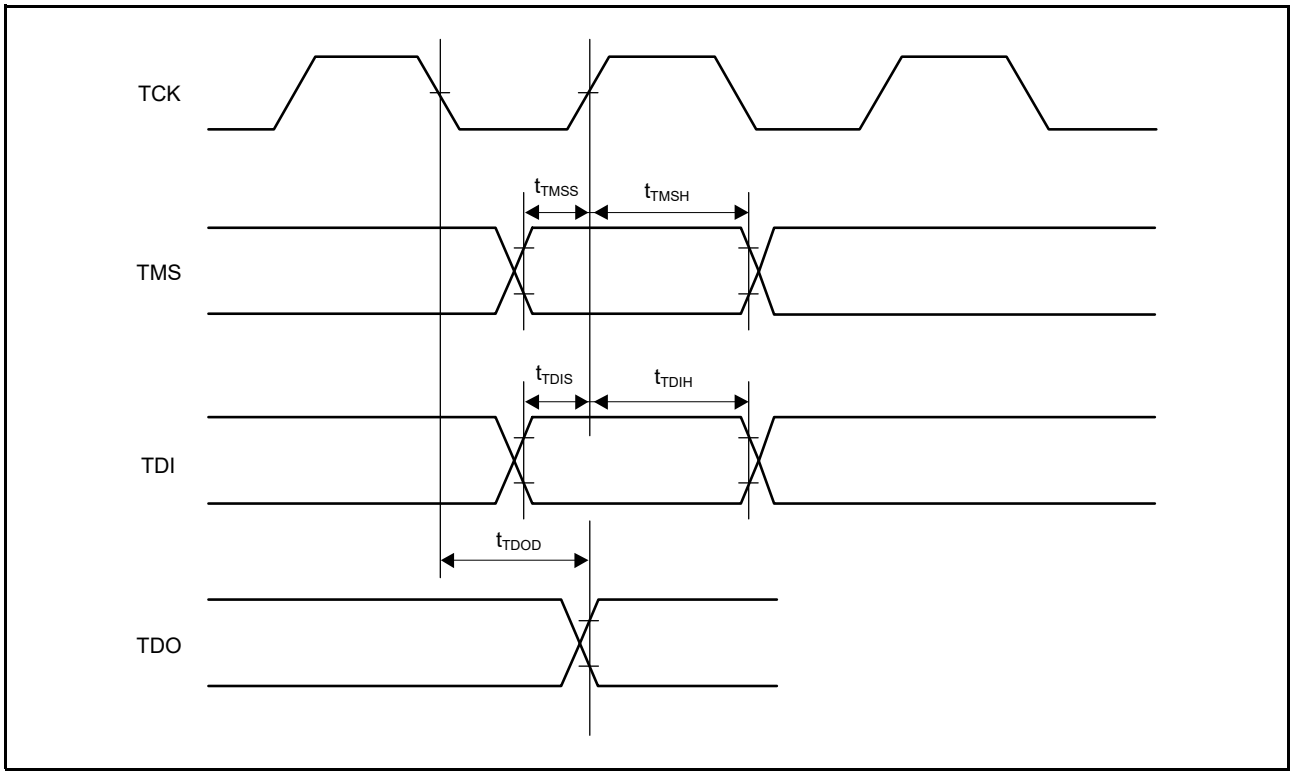
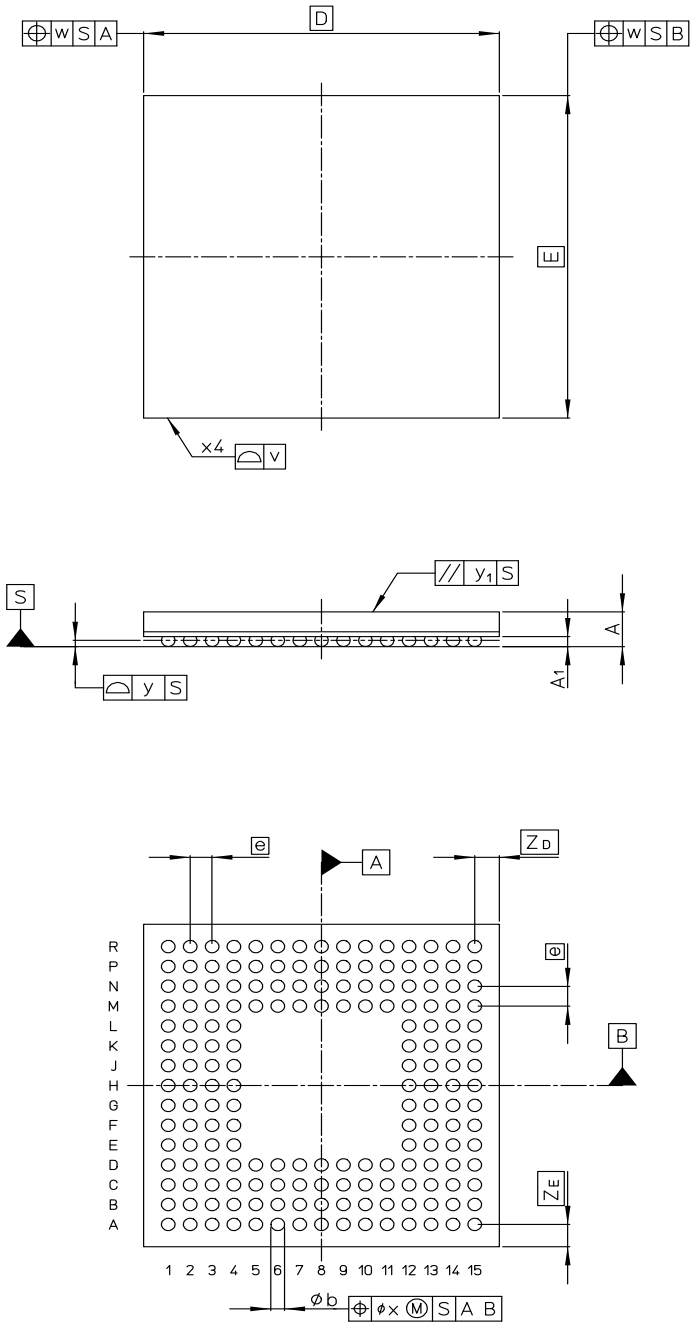


Figure 5.85 Boundary Scan Input/Output Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g

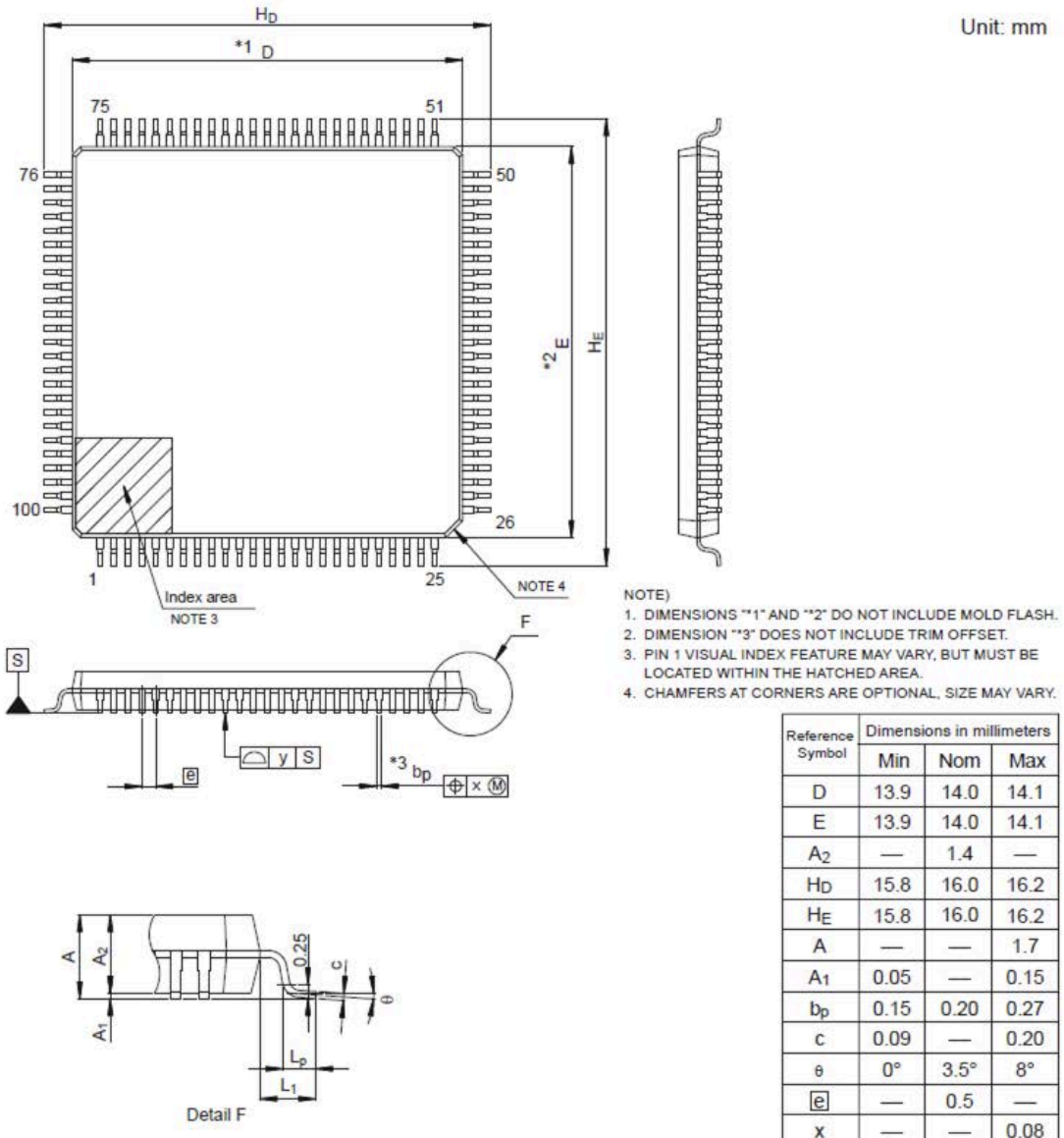


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.2
SD	—	—	—
SE	—	—	—
ZD	—	0.90	—
ZE	—	0.90	—

Figure B 176-Pin LFBGA (PLBG0176GA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure G 100-Pin LFQFP (PLQP0100KB-B)