Renesas Electronics America Inc - R5F56517BDFB#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56517bdfb-30

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
	SD host interface (SDHI)*3	• 1 channel • Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
	SD slave interface (SDSI)*3	• 1 channel • Compliant with the SDIO Card Specification Ver.2.00 (CSA is not supported) • 1-bit SD/4-bit SD/SPI mode • SDIO Proprietary command is supported • SD/SPI Mandatory command is supported • Interrupt requests: 6
	MMC host interface (MMCIF)	• 1 channel • Transfer speed: Data transfer mode (30 MB/s), backward compatible mode (25 MB/s) • Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) • Interface for Multimedia Cards (MMCs) • Device buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt • DMA transfer requests: CE_DATA write and CE_DATA read • Support for card detection, boot operation, high priority interrupt (HPI)
	Parallel data capture unit (PDC)	• 1 channel • Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals • Setting of the image size when clipping of the output for a one-frame image is required
	Graphic-LCD controller (GLCDC)	• 1 channel • Various data formats and LCD panels are supported • Superposition of 3 planes (single-color background, graphic 1, graphic 2) • 32- and 16-bpp color data and 8-, 4-, and 1-bit CLUT data formats are supported
	2D drawing engine (DRW2D)	• 1 channel • Vector drawing (straight lines, triangles, and circles) • Bit blitting (with support for filling, copying, stretching, and rotation) • Bus master function for input and output of frame buffer data 32-, 16-, and 8-bit pixel graphics data are supported • Bus master function for input of texture data Input of texture data (32, 24, 16, 8, 4, 2, or 1 bit) are supported. Run length encoding is supported A CLUT is installed and index data can be converted into color data • Two rendering modes are supported (register mode and display list mode) • Performance counting • Interrupts in response to completion of rendering and processing of the display list

Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (1/2)

Functions	Products	Products with 1 Mbyte of code flash memory or less		Products with at least 1.5 Mbytes of code flash memory		
	Package	145 Pins, 144 Pins	100 Pins	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
Code Flash Memory	Code Flash Memory Capacity	512 Kbytes/768 Kbytes /1 Mbyte		1.5 Mbytes/2 Mbytes		
	Dual bank function	Not available		Available		
	BGO function	Not available		Available		
Data Flash Memory		Not available		32 Kbytes		
RAM		256 Kbytes		640 Kbytes (256 Kbytes + 384 Kbytes of expansion RAM)		
External bus	External bus width	16/8 bits		32/16/8 bits	16/8 bits	
	SDRAM area controller	Available	Not available	Available		Not available
DMA	DMA controller	Ch. 0 to 7				
	Data transfer controller	Available				
	EXDMA controller	Ch. 0 and 1				
Timers	16-bit timer pulse unit	Ch. 0 to 5				
	Multi-function timer pulse unit 3	Ch. 0 to 8				
	Port output enable 3	Available				
	Programmable pulse generator	Ch. 0 and 1				
	8-bit timers	Ch. 0 to 3				
	Compare match timer	Ch. 0 to 3				
	Compare match timer W	Ch. 0 and 1				
	Realtime clock	Available				
	Watchdog timer	Available				
	Independent watchdog timer	Available				
Communication function	Ethernet controller	Ch. 0 (only for RX65N group)				
	DMA Controller for the Ethernet Controller	Ch. 0 (only for RX65N group)				
	USB 2.0 FS host/function module	Ch. 0				
	Serial communications interfaces (SCIg)	Ch. 0 to 9	Ch. 0 to 3, 5, 6, 8 and 9	Ch. 0 to 9		Ch. 0 to 3, 5, 6, 8 and 9
	Serial communications interfaces (SCIh)	Ch. 12				
	Serial communications interfaces (SCIi)	Ch. 10 and 11				
	I^2C bus interfaces	Ch. 0 and 2		Ch. 0 to 2		Ch. 0 and 2
	Serial peripheral interface	Ch. 0 to 2				
	CAN module	Ch. 0 and 1				
	Quad serial peripheral interface	Ch. 0				
	SD host interface	Available				
	SD slave interface	Available				
	MMC host interface	Available				
	Parallel data capture unit	Available	Not available	Available		Not available
Graphics	Graphic-LCD controller	Not available		Available		
	2D drawing engine	Not available		Available		

Table 1.3 List of Products (6/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F56517EDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56517FDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56514ADFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56514BDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56514EDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56514FDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F5651EDDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651EDDLC	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDLC	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDLC	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDLC	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651EDDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F56519ADLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56519BDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56519EDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56519FDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56517ADLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56517BDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56517EDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56517FDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56514ADLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56514BDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56514EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56514FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (1/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
A1	AVSS0								
A2		P07						IRQ15	ADTRG0#
A3		P40						IRQ8-DS	AN000
A4		P42						IRQ10-DS	AN002
A5		P45						IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7				AN114
A7		P92	A18	POE4#	RXD7/SMISO7/SSCL7				AN116
A8		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2-B/MMC_D2-B	LCD_DATA22-B*1	IRQ2	AN110
A9		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/POE4#	SSLC2-A	QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B	LCD_DATA18-B*1	IRQ6	AN106
A10	VSS								
A11		P62	RAS#/D1[A1/D1]*1/CS2#						
A12		PE1	D9[A9/D9]/D1[A1/D1]*1	MTIOC4C/MTIOC3B/PO18	TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B*1		ANEX1
A13		PE3	D11[A11/D11]/D3[A3/D3]*1	MTIOC4B/PO26/TOC3/POE8#	ET0_ERXD3/CTS12#/RTS12#/SS12#	MMC_D7-B	LCD_DATA13-B*1		AN101
B1	AVCC1								
B2	AVCC0								
B3		P05						IRQ13	DA1
B4	VREFL0								
B5		P43						IRQ11-DS	AN003
B6		P47						IRQ15-DS	AN007
B7		P91	A17		SCK7				AN115
B8		PD0	D0[A0/D0]	POE4#			LCD_EXTCLK-B*1	IRQ0	AN108
B9		PD4	D4[A4/D4]	MTIOC8B/POE11#	SSLC0-A	QSSL-B/SDHI_CMD-B/MMC_CMD-B	LCD_DATA20-B*1	IRQ4	AN112
B10	VCC								
B11		P61	SDCS#/D0[A0/D0]*1/CS1#						
B12		PE2	D10[A10/D10]/D2[A2/D2]*1	MTIOC4A/PO23/TIC3	RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B*1	IRQ7-DS	AN100

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/5)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
F2	VCC								
F3	UPSEL	P35						NMI	
F4		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN			IRQ2-DS	
F5		P12		TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
F6		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK6	SDSI_D3-B	LCD_TCON1-B*1		
F7		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6#	SDSI_D2-B	LCD_TCON2-B*1		
F8		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD6/SMISO6/ SSCL6		LCD_DATA0-B*1	IRQ12	
F9		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B*1		
F10	VSS								
G1		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0			IRQ3-DS	
G2	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
G3	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
G4	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A				
G5		P53*2	BCLK						
G6		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
G7		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CLK-B*1		
G8		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B*1		
G9		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6		LCD_TCON3-B*1	IRQ4-DS	
G10	VCC								

Table 4.1 List of I/O Registers (Address Order) (3 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 1248h	RAM	Expansion RAM Error Address Capture Register	EXRAMECAD	32	32	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK		Buses
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK		Buses
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK		DMACAa
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 201Fh	DMAC0	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 205Fh	DMAC1	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 209Fh	DMAC2	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa

Table 4.1 List of I/O Registers (Address Order) (7 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 3852h	BSC	CS5 Control Register	CS5CR	16	16	1, 2 BCLK		Buses
0008 385Ah	BSC	CS5 Recovery Cycle Register	CS5REC	16	16	1, 2 BCLK		Buses
0008 3862h	BSC	CS6 Control Register	CS6CR	16	16	1, 2 BCLK		Buses
0008 386Ah	BSC	CS6 Recovery Cycle Register	CS6REC	16	16	1, 2 BCLK		Buses
0008 3872h	BSC	CS7 Control Register	CS7CR	16	16	1, 2 BCLK		Buses
0008 387Ah	BSC	CS7 Recovery Cycle Register	CS7REC	16	16	1, 2 BCLK		Buses
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK		Buses
0008 3C00h	BSC	SDC Control Register	SDCCR	8	8	1, 2 BCLK		Buses
0008 3C01h	BSC	SDC Mode Register	SDCMOD	8	8	1, 2 BCLK		Buses
0008 3C02h	BSC	SDRAM Access Mode Register	SDAMOD	8	8	1, 2 BCLK		Buses
0008 3C10h	BSC	SDRAM Self-Refresh Control Register	SDSELF	8	8	1, 2 BCLK		Buses
0008 3C14h	BSC	SDRAM Refresh Control Register	SDRFCR	16	16	1, 2 BCLK		Buses
0008 3C16h	BSC	SDRAM Auto-Refresh Control Register	SDRFEN	8	8	1, 2 BCLK		Buses
0008 3C20h	BSC	SDRAM Initialization Sequence Control Register	SDICR	8	8	1, 2 BCLK		Buses
0008 3C24h	BSC	SDRAM Initialization Register	SDIR	16	16	1, 2 BCLK		Buses
0008 3C40h	BSC	SDRAM Address Register	SDADR	8	8	1, 2 BCLK		Buses
0008 3C44h	BSC	SDRAM Timing Register	SDTR	32	32	1, 2 BCLK		Buses
0008 3C48h	BSC	SDRAM Mode Register	SDMOD	16	16	1, 2 BCLK		Buses
0008 3C50h	BSC	SDRAM Status Register	SDSR	8	8	1, 2 BCLK		Buses
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK		MPU
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK		MPU
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK		MPU
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK		MPU
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK		MPU
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK		MPU
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK		MPU
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK		MPU
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK		MPU
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK		MPU
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK		MPU
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK		MPU
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK		MPU
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK		MPU
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK		MPU
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK		MPU
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK		MPU
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK		MPU
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK		MPU
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK		MPU
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK		MPU
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK		MPU
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK		MPU
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK		MPU
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK		MPU
0008 7010h to 0008 70FFh	ICU	Interrupt Request Registers 016 to 255	IR016 to 255	8	8	2 ICLK		ICUB
0008 711Ah to 0008 71FFh	ICU	DTC Transfer Request Enable Registers 026 to 255	DTCER026 to DTCER255	8	8	2 ICLK		ICUB
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Registers 02 to 1F	IER02 to IER1F	8	8	2 ICLK		ICUB

Table 4.1 List of I/O Registers (Address Order) (25 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A046h	SMCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A049h	SCI2	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Ah	SCI2	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Bh	SCI2	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Ch	SCI2	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Eh	SCI2	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Fh	SCI2	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Eh	SCI2	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A050h	SCI2	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A051h	SCI2	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A050h	SCI2	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A052h	SCI2	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A066h	SMCI3	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (61 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 3098h	DRW2D	U Limiter Y-Axis Increment Register	LUYADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 309Ch	DRW2D	V Limiter Start Value Integer Part Register	LVSTI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A0h	DRW2D	V Limiter Start Value Fractional Part Register	LVSTF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A4h	DRW2D	V Limiter X-Axis Increment Integer Part Register	LVXADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A8h	DRW2D	V Limiter Y-Axis Increment Integer Part Register	LVYADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30ACh	DRW2D	V Limiter Increment Fractional Parts Register	LVYXADDF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B4h	DRW2D	Texels Per Texture Line Register	TEXPITCH	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B8h	DRW2D	Texture Mask Register	TEXMSK	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30BCh	DRW2D	Texture Base Address Register	TEXORG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C0h	DRW2D	Interrupt Control Register	IRQCTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C4h	DRW2D	Cache Control Register	CACHECTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C8h	DRW2D	Display List Start Address Register	DLISTST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30CCh	DRW2D	Performance Counter 1	PERFCNT1	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D0h	DRW2D	Performance Counter 2	PERFCNT2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D4h	DRW2D	Performance Counters Control Register	PERFTRG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30DCh	DRW2D	CLUT Start Address Register	TEXCLADDR	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E0h	DRW2D	CLUT Data Register	TEXCLDATA	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E4h	DRW2D	CLUT Offset Register	TEXCLOFST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E8h	DRW2D	Chroma Key Register	COLKEY	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
007F C040h	FLASH	Data Flash Memory Access Frequency Setting Register	EEPFCLK	8	8	2 FCLK		Flash
FE7F 7D7Ch	TEMPS	Temperature Sensor Calibration Data Register	TSCDR	32	32	1 to 3 ICLK		TEMPS
FE7F 7D90h	FLASH	Unique ID Register 0	UIDR0	32	32	1 to 3 ICLK		Flash
FE7F 7D94h	FLASH	Unique ID Register 1	UIDR1	32	32	1 to 3 ICLK		Flash
FE7F 7D98h	FLASH	Unique ID Register 2	UIDR2	32	32	1 to 3 ICLK		Flash
FE7F 7D9Ch	FLASH	Unique ID Register 3	UIDR3	32	32	1 to 3 ICLK		Flash

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 0008 81ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 0008 81EEh and 0008 81ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 0008 81EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 0008 81EFh and 0008 81EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 0008 81FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 0008 81FEh and 0008 81FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 0008 81FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 0008 81FFh and 0008 81FDh, respectively.

Note 5. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 6. The address must end with 0h, 4h, 8h, or Ch when access is made in 32-bit units. The address must end with 0h, 2h, 4h, 6h, 8h, Ah, Ch, or Eh when access is made in 16-bit units.

Note 7. When the register is accessed while the GLCDC is operating, a delay may be generated in accessing.

Table 5.4 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Input pull-up MOS current	Other than P35	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μA	V_{in} = VCC
Input capacitance	All input pins (except for ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	Ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM		—	—	16		

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

Table 5.17 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.63	4.16	3.78	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 5.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	9.26	8.33	7.57	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 5.7

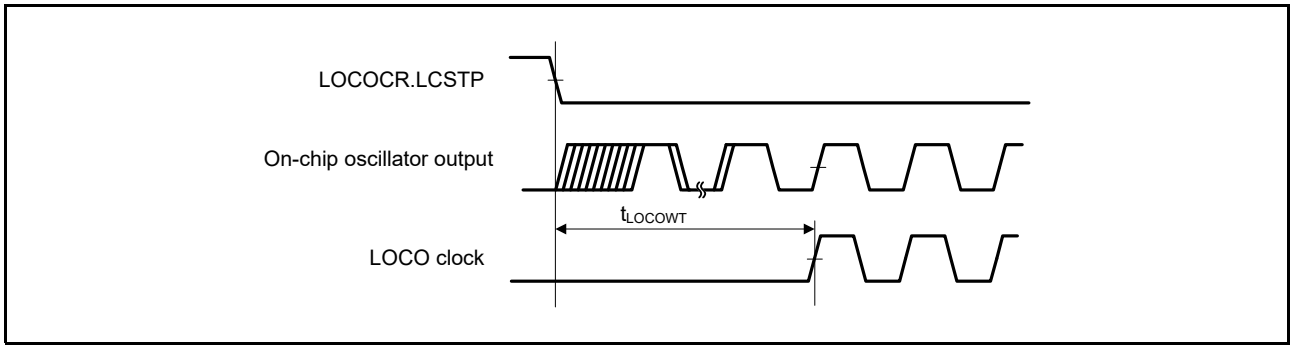


Figure 5.6 LOCO Clock Oscillation Start Timing

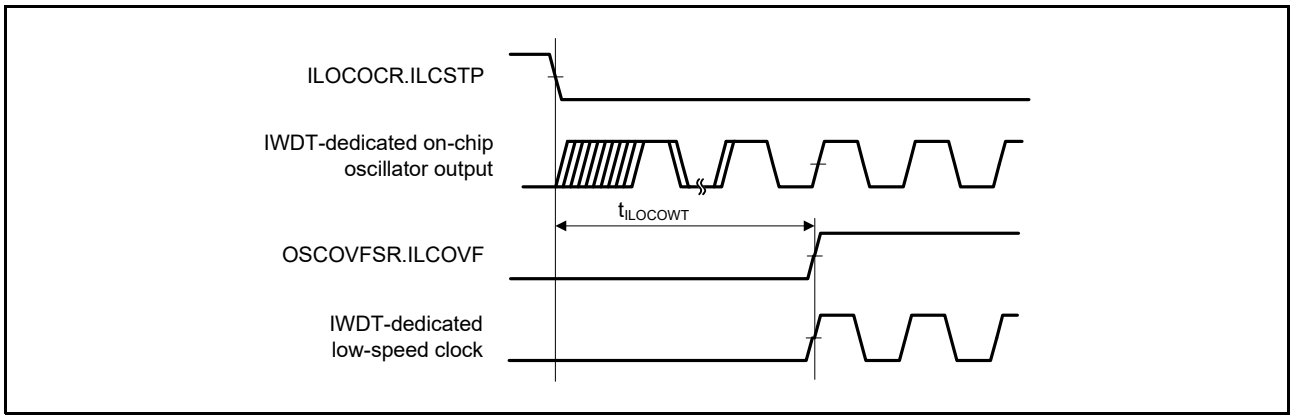


Figure 5.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

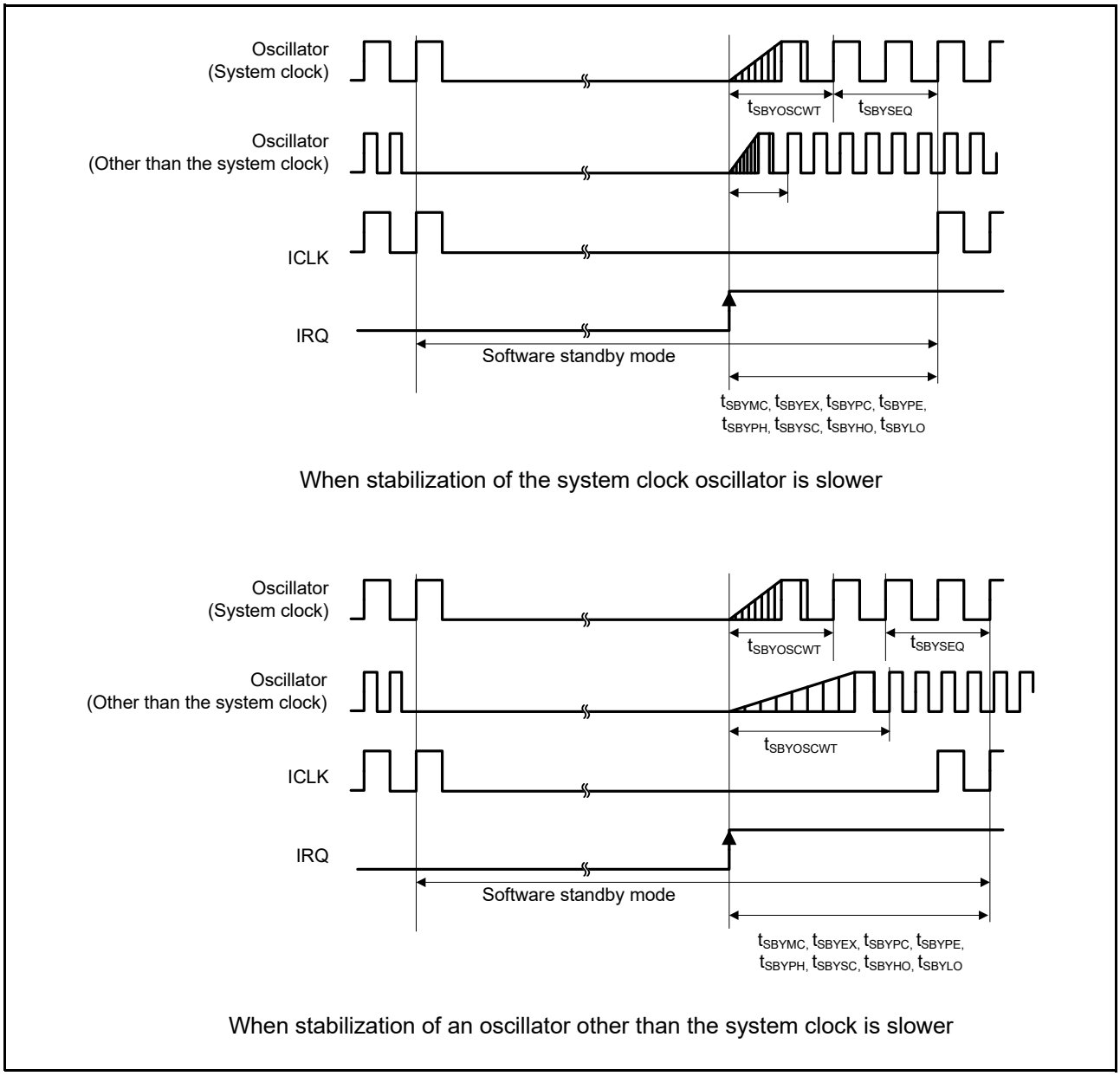


Figure 5.12 Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.23 Control Signal Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 5.14
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 5.14
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 5.15
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 5.15

Note 1. t_{PBcyc}: PCLKB cycle

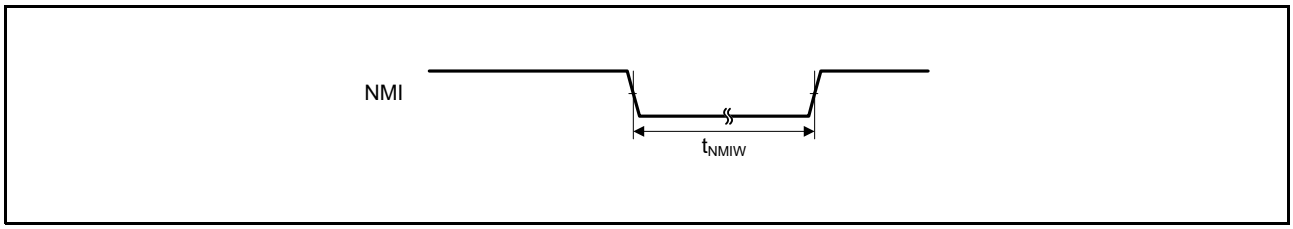


Figure 5.14 NMI Interrupt Input Timing

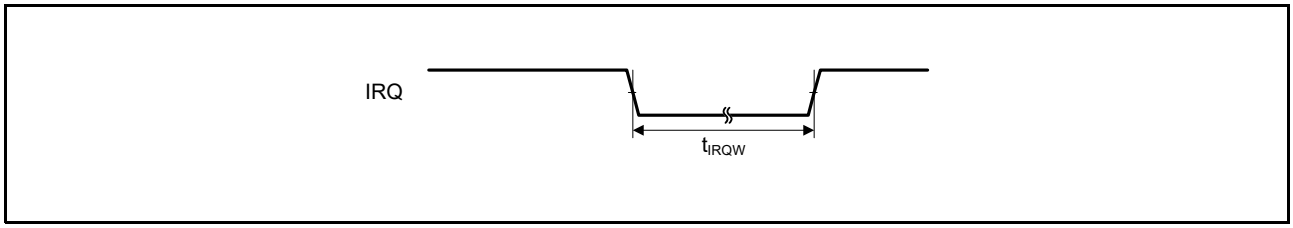
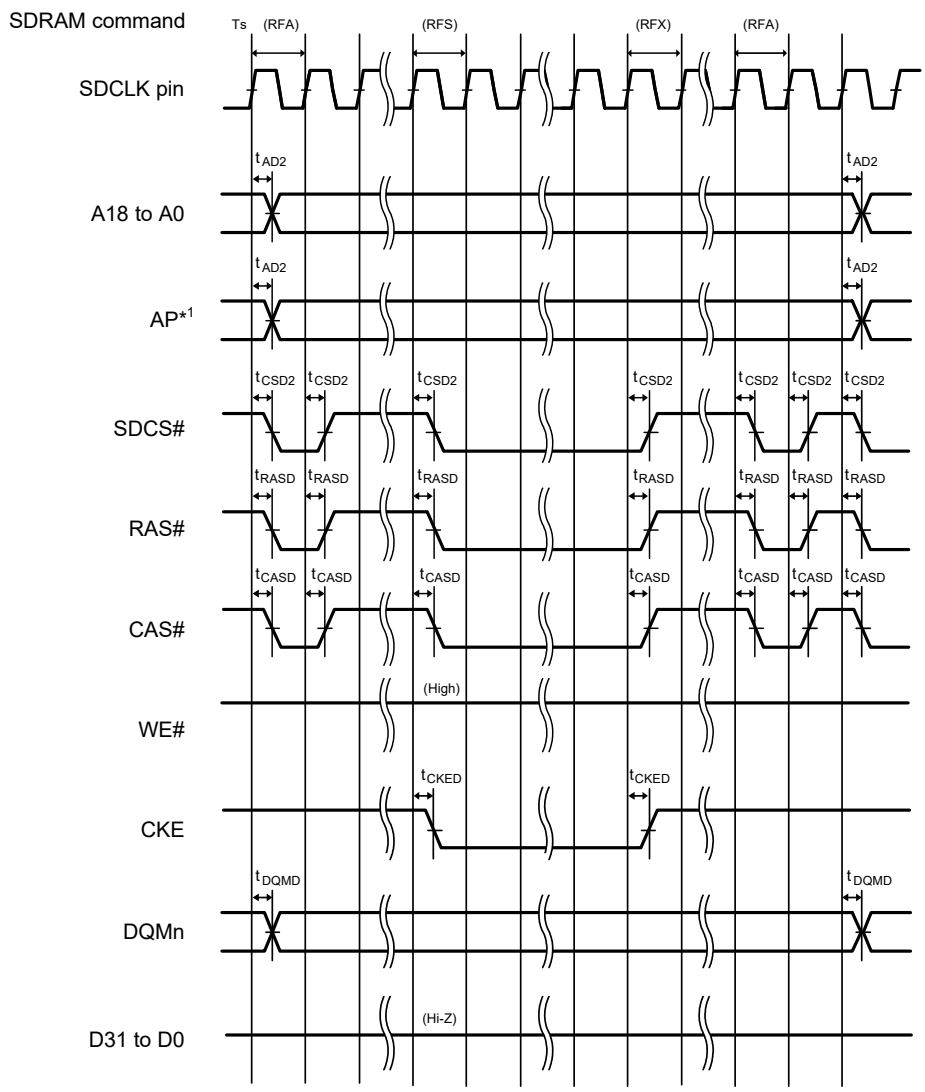


Figure 5.15 IRQ Interrupt Input Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.29 SDRAM Space Self-Refresh Bus Timing

Table 5.36 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{PAcyc}	Figure 5.44
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 5.45 to Figure 5.50
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{PBcyc}	Figure 5.49, Figure 5.50
	Slave output release time	t_{REL}	—	5	t_{PBcyc}	

Note 1. t_{PAcyc}: PCLKA cycle, t_{PBcyc}: PCLKB cycle

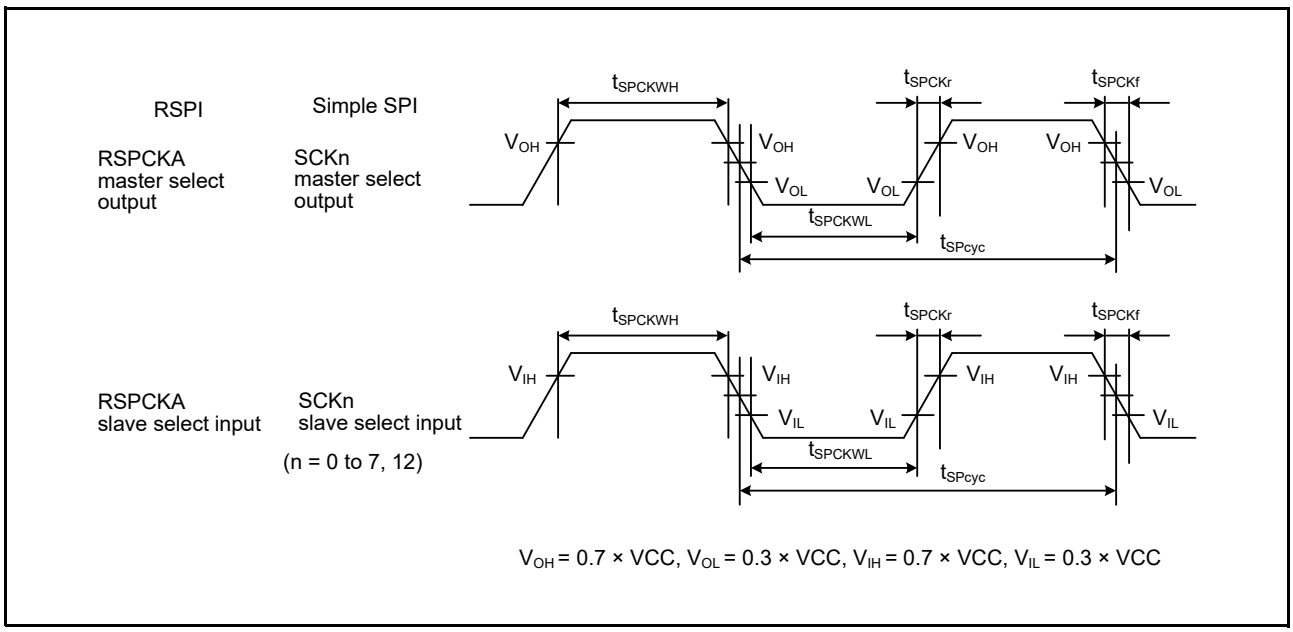


Figure 5.44 RSPI Clock Timing and Simple SPI Clock Timing

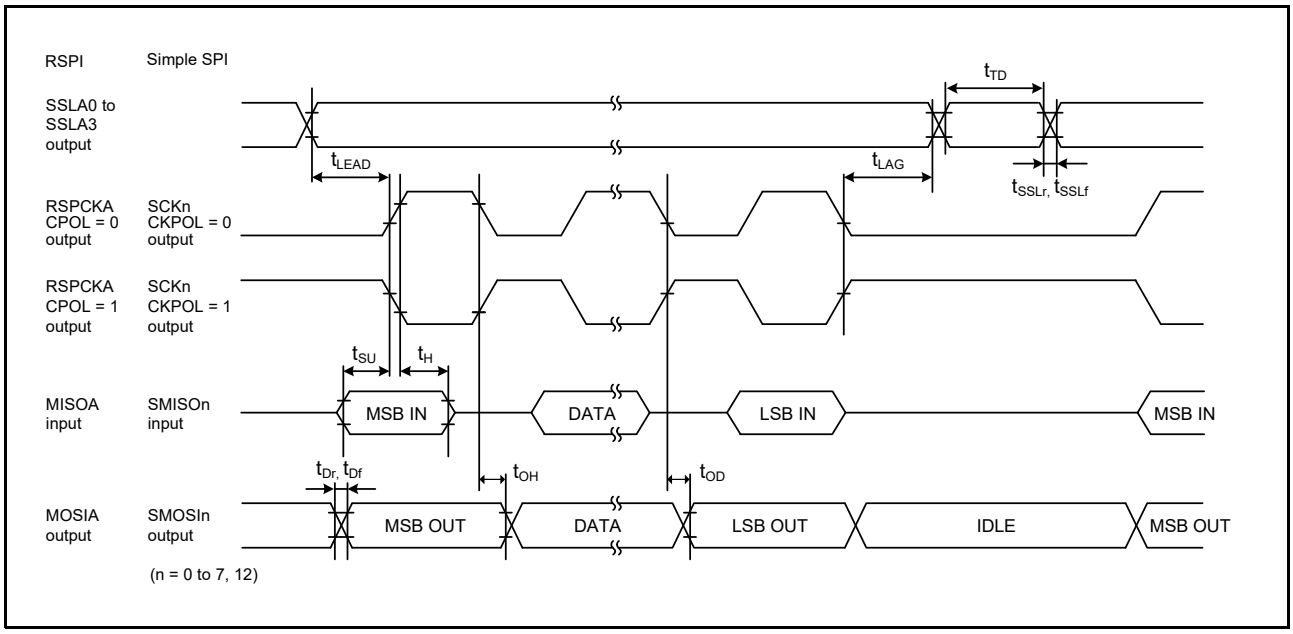


Figure 5.45 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1)

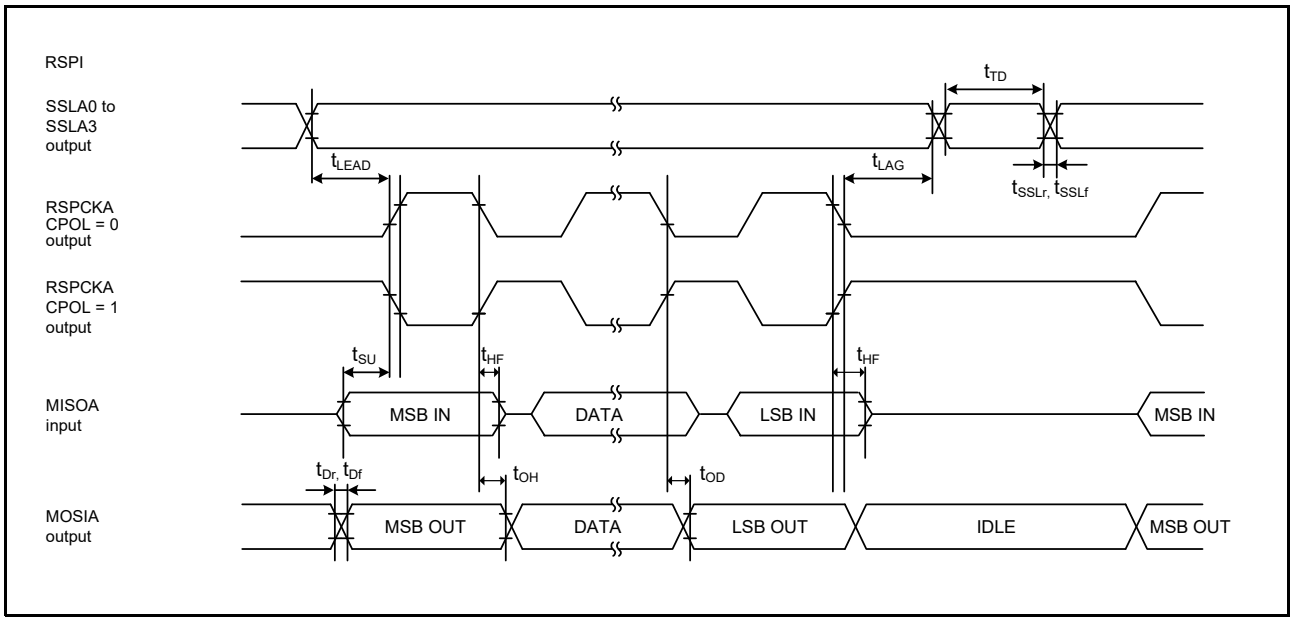


Figure 5.46 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

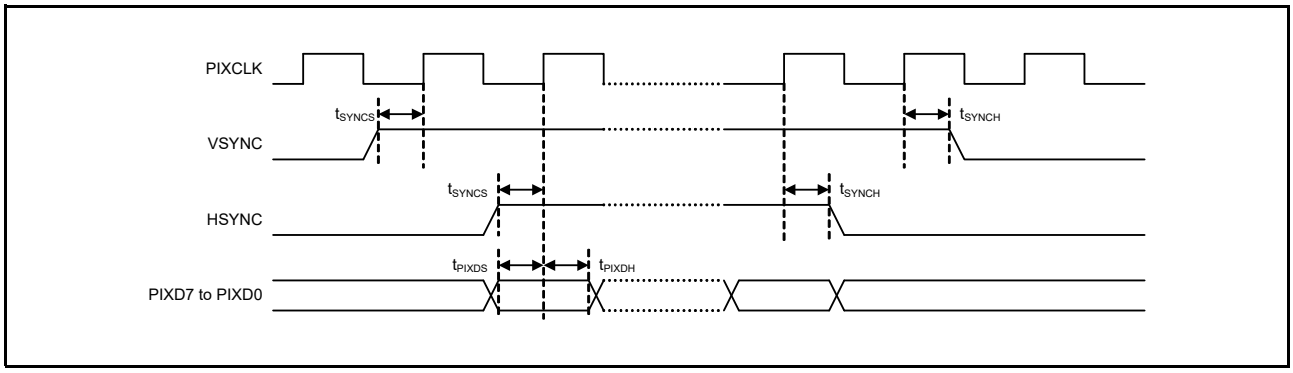


Figure 5.68 PDC AC Timing

Table 5.43 GLCDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD_EXTCLK Input clock frequency	t_{Ecyc}	—	—	30*1	MHz	Figure 5.69
LCD_EXTCLK Input clock Low pulse width	t_{WL}	0.45	—	0.55	t_{Ecyc}	
LCD_EXTCLK Input clock High pulse width	t_{WH}	0.45	—	0.55		
LCD_CLK Output clock frequency	t_{Lcyc}	—	—	30*1	MHz	Figure 5.70
LCD_CLK Output clock Low pulse width	t_{LOL}	0.4	—	0.6	t_{Lcyc}	
LCD_CLK Output clock High pulse width	t_{LOH}	0.4	—	0.6	t_{Lcyc}	
LCD data output Delay timing	t_{DD}	–3.5*2	—	4*2	ns	Figure 5.71

Note 1. Parallel RGB888,666,565: Max. 27 MHz
Serial RGB888: Max. 30 MHz (4x speed)

Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc) to indicate group membership appended to their names as groups.
For the GLCDC interface, the AC portion of the electrical characteristics is measured for each group.
If we use group “-A” and “-B” combination, “LCD data output Delay timing (t_{DD})” is Min = –5.0 ns, Max = 5.5 ns.

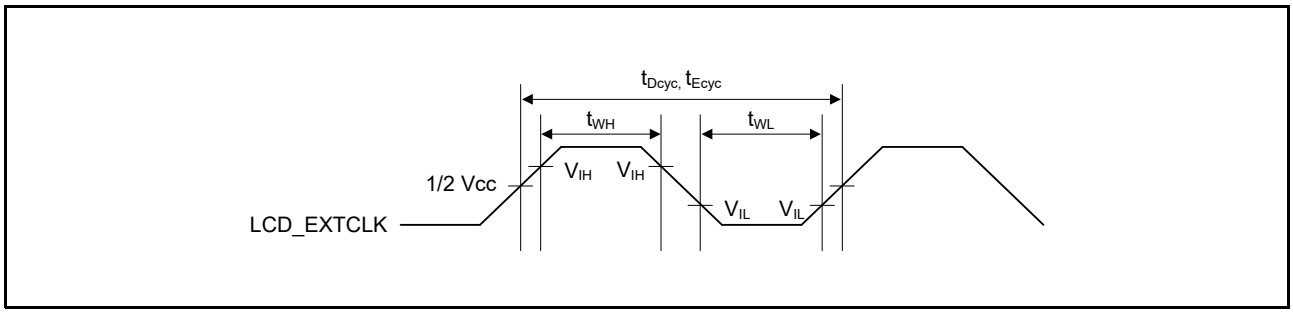


Figure 5.69 LCD_EXTCLK Clock Input Timing

5.4 USB Characteristics

Table 5.44 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 5.72
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

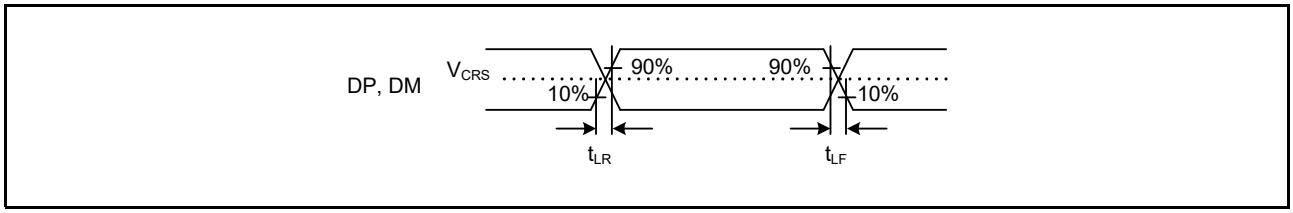


Figure 5.72 DP and DM Output Timing (Low Speed)

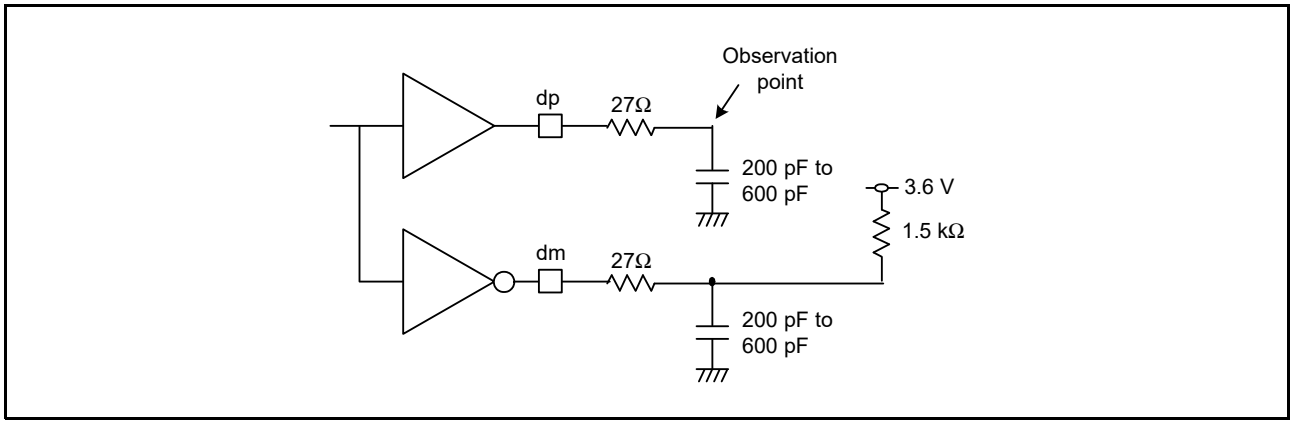


Figure 5.73 Test Circuit (Low Speed)

Table 5.47 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 1 MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Conversion time*1 (Operation at PCLK = 60 MHz)	Permissible signal source impedance (max.) = 1.0 kΩ	0.88 (0.633)*2	—	—	µs	Sampling in 38 states (ADSAM.SAM = 1)
Conversion time*1 (Operation at PCLK = 30 MHz)		1 (0.500)*2	—	—	µs	Sampling in 15 states (ADSAM.SAM = 1)
Analog input capacitance		—	—	30	pF	
Offset error		—	±2.0	±3.5	LSB	
Full-scale error		—	±2.0	±3.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±4.0	±6.0	LSB	
DNL differential nonlinearity error (Operation at PCLK = 60 MHz)		—	±1.5	±4.0	LSB	
DNL differential nonlinearity error (Operation at PCLK = 30 MHz)		—	±1.5	±2.5	LSB	
INL integral nonlinearity error (Operation at PCLK = 60 MHz)		—	±2.0	±4.0	LSB	
INL integral nonlinearity error (Operation at PCLK = 30 MHz)		—	±2.0	±3.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 5.48 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 60 MHz, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.13	1.18	1.23	V	

5.9 Oscillation Stop Detection Timing

Table 5.52 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.80

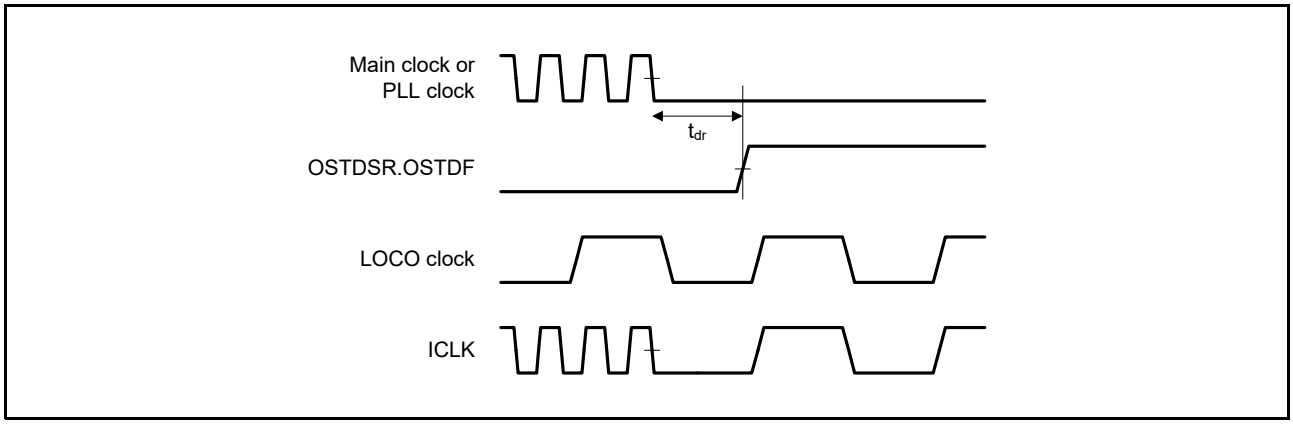


Figure 5.80 Oscillation Stop Detection Timing