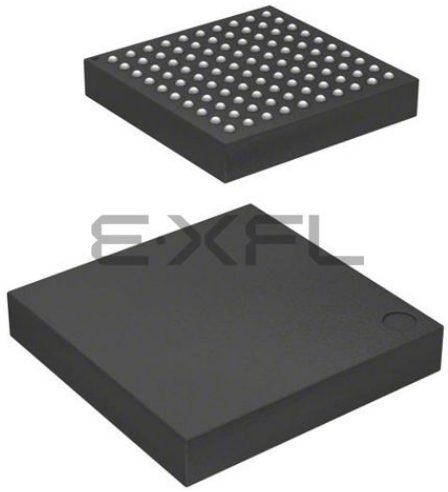

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56517bdlj-20

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
A1	AVSS0								
A2	AVCC0								
A3	VREFL0								
A4		P42						IRQ10-DS	AN002
A5		P46						IRQ14-DS	AN006
A6	VCC								
A7	VSS								
A8		P94	D20/A20						
A9	VCC								
A10	TRSYNC1	P97	D23/A23						
A11		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106
A12		P60	CS0#						
A13		P63	CAS#/ D2[A2/D2]/ CS3#						
A14		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B		ANEX1
A15		PE2	D10[A10/ D10]/D2[A2/ D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100
B1		P05						IRQ13	DA1
B2		P07						IRQ15	ADTRG0#
B3		P40						IRQ8-DS	AN000
B4		P41						IRQ9-DS	AN001
B5		P47						IRQ15-DS	AN007
B6		P91	D17/A17		SCK7				AN115
B7		P92	D18/A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B	IRQ1	AN109
B9	TRDATA5	P96	D22/A22						
B10		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
B11	TRDATA7	PG1	D25						
B12	VSS								
B13		P64	WE#/D3[A3/ D3]/CS4#						
B14		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B		ANEX0

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
B13		PE4	D12[A12/D12]/D4[A4/D4]*1	MTIOC4D/MTIOC1A/PO28	ET0_ERXD2/SSLB0-B		LCD_DATA12-B*1		AN102
C1	AVSS1								
C2		P02		TMCI1	SCK6			IRQ10	AN120
C3	VREFH0								
C4		P41						IRQ9-DS	AN001
C5		P46						IRQ14-DS	AN006
C6	VSS								
C7		PD1	D1[A1/D1]	MTIOC4B/POE0#	MOSIC-A/CTX0		LCD_DATA23-B*1	IRQ1	AN109
C8		PD3	D3[A3/D3]	MTIOC8D/TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DATA21-B*1	IRQ3	AN111
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3-A	QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B	LCD_DATA17-B*1	IRQ7	AN107
C10		P63	CAS#/D2[A2/D2]*1/CS3#						
C11		PE0	D8[A8/D8]/D0[A0/D0]*1	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B*1		ANEX0
C12		P70	SDCLK						
C13	VSS								
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6			IRQ8	AN118
D2		PF5						IRQ4	
D3		P03						IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6			IRQ9	AN119
D5	VCC								
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#				AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/POE10#	SSLC1-A	QSPCLK-B/SDHI_CLK-B/MMC_CLK-B	LCD_DATA19-B*1	IRQ5	AN113
D8		P60	CS0#						
D9		P64	WE#/D3[A3/D3]*1/CS4#						
D10		PE7	D15[A15/D15]/D7[A7/D7]*1	MTIOC6A/TOC1	MISOB-B	SDHI_WP/MMC_RES#-B	LCD_DATA9-B*1	IRQ7	AN105
D11	VCC								
D12		PE5	D13[A13/D13]/D5[A5/D5]*1	MTIOC4C/MTIOC2B	ET0_RX_CLK/REF50CK0/RSPCKB-B		LCD_DATA11-B*1	IRQ5	AN103
D13		PE6	D14[A14/D14]/D6[A6/D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/MMC_CD-B	LCD_DATA10-B*1	IRQ6	AN104
E1	VSS								
E2	VCL								
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#				

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
E4	EMLE								
E5		P44						IRQ12-DS	AN004
E10		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DATA8-B*1		
E11		P66	DQM0/CS6#	MTIOC7D					
E12		P65	CKE/CS5#						
E13		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	XCIN								
F2	XCOUT								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
F4	VBATT								
F10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DATA5-B*1	IRQ6-DS	
F11	VSS								
F12		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DATA7-B*1	IRQ11	
F13		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DATA6-B*1		
G1	XTAL	P37							
G2	RES#								
G3	MD/FINED								
G4	BSCANP								
G10		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B*1		
G11		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B*1		
G12	VCC								
G13		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DATA4-B*1	IRQ5-DS	
H1	EXTAL	P36							
H2	VCC								
H3	VSS								
H4	UPSEL	P35						NMI	
H10		P72	A19/CS2#		ET0_MDC				
H11		P71	A18/CS1#		ET0_MDIO				

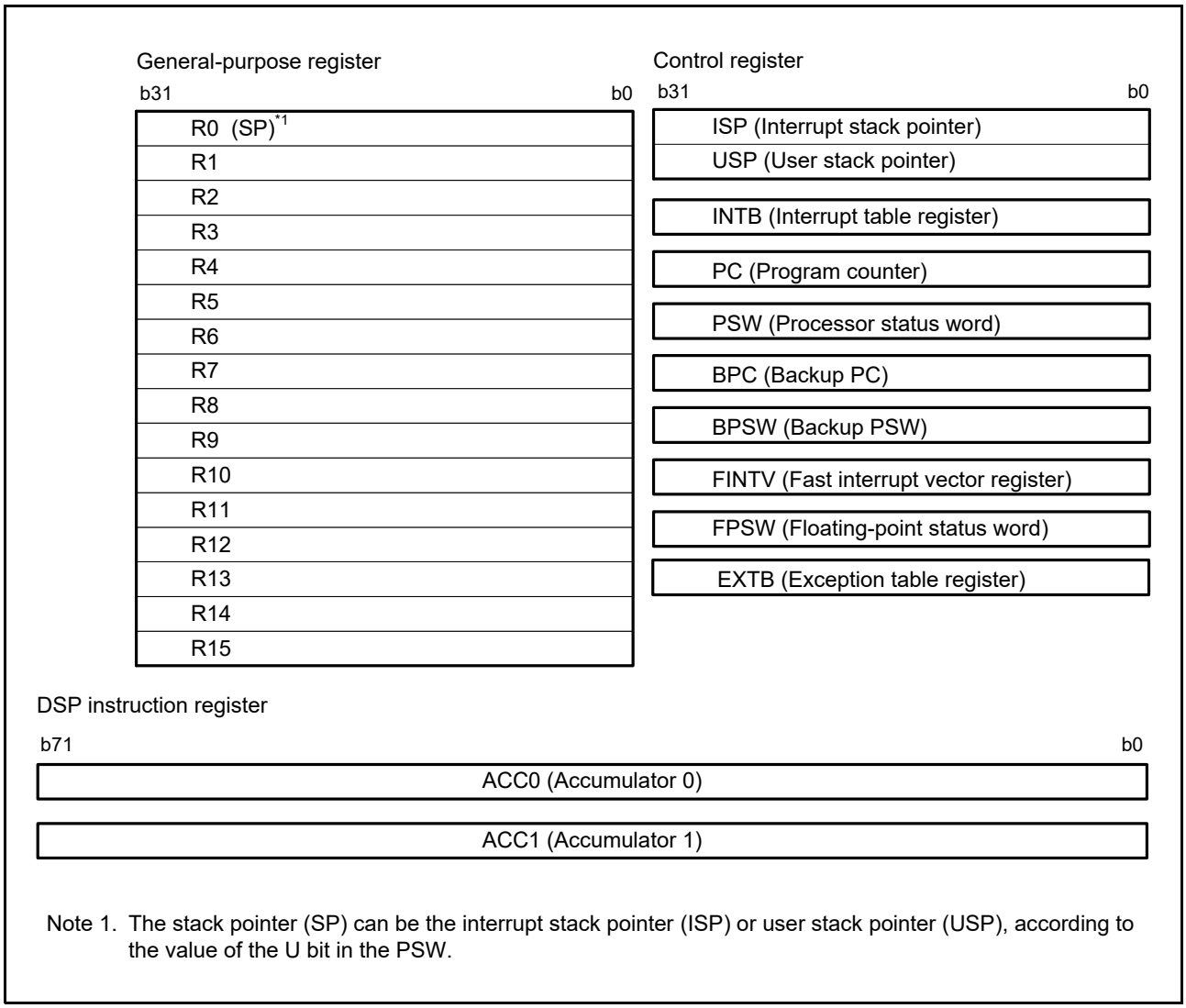
Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (5/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
79		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DATA17-B*1	IRQ7	AN107
80		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B*1	IRQ6	AN106
81		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B*1	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B*1	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DATA21-B*1	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2-B/MMC_D2-B	LCD_DATA22-B*1	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B*1	IRQ1	AN109
86		PD0	D0[A0/D0]	POE4#			LCD_EXTCLK-B*1	IRQ0	AN108
87		P47						IRQ15-DS	AN007
88		P46						IRQ14-DS	AN006
89		P45						IRQ13-DS	AN005
90		P44						IRQ12-DS	AN004
91		P43						IRQ11-DS	AN003
92		P42						IRQ10-DS	AN002
93		P41						IRQ9-DS	AN001
94	VREFL0								
95		P40						IRQ8-DS	AN000
96	VREFH0								
97	AVCC0								
98		P07						IRQ15	ADTRG0#
99	AVSS0								
100		P05						IRQ13	DA1

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

2. CPU

Figure 2.1 shows register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK		Operating Modes
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK		Operating Modes
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK		Low Power Consumption
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK		Low Power Consumption
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK		Low Power Consumption
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK		Low Power Consumption
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK		Clock Generation Circuit
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK		Clock Generation Circuit
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK		Clock Generation Circuit
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK		Clock Generation Circuit
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK		Clock Generation Circuit
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK		Clock Generation Circuit
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK		Clock Generation Circuit

Table 4.1 List of I/O Registers (Address Order) (4 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 20DFh	DMAC3	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2100h	DMAC4	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2104h	DMAC4	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2108h	DMAC4	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 211Fh	DMAC4	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 215Fh	DMAC5	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 219Fh	DMAC6	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 21DCh	DMAC7	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 21DDh	DMAC7	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 21DEh	DMAC7	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 21DFh	DMAC7	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2200h	DMAC	DMAC Module Start Register	DMAST	8	8	2 ICLK		DMACAa
0008 2204h	DMAC	DMAC74 Interrupt Status Monitor Register	DMIST	8	8	2 ICLK		DMACAa
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK		DTCb
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK		DTCb
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK		DTCb

Table 4.1 List of I/O Registers (Address Order) (14 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8040h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	R12DA
0008 8042h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK	R12DA
0008 8044h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8045h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8046h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8048h	DA	D/A Output Amplifier Control Register	DAAMPCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 805Ch	DA	D/A Output Amplifier Stabilization Wait Control Register	DAASWCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8100h	TPUA	Timer Start Register	TSTR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8101h	TPUA	Timer Synchronous Register	TSYR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8111h	TPU0	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8112h	TPU0	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8113h	TPU0	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8114h	TPU0	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8115h	TPU0	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8116h	TPU0	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8118h	TPU0	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa

Table 4.1 List of I/O Registers (Address Order) (23 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A006h	SMCI0	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (40 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C16Eh	MPC	P56 Pin Function Control Register	P56PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C16Fh	MPC	P57 Pin Function Control Register	P57PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C176h	MPC	P66 Pin Function Control Register	P66PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C177h	MPC	P67 Pin Function Control Register	P67PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C17Fh	MPC	P77 Pin Function Control Register	P77PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C183h	MPC	P83 Pin Function Control Register	P83PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C184h	MPC	P84 Pin Function Control Register	P84PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C185h	MPC	P85 Pin Function Control Register	P85PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C186h	MPC	P86 Pin Function Control Register	P86PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C187h	MPC	P87 Pin Function Control Register	P87PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC

Table 4.1 List of I/O Registers (Address Order) (58 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 0400h to 000E 07FCh	GLCDC	Graphic 1 Color Look-up Table 1[0 to 255]	GR1CLUT1[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 0800h to 000E 0BFCh	GLCDC	Graphic 2 Color Look-up Table 0[0 to 255]	GR2CLUT0[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 0C00h to 000E 0FFCh	GLCDC	Graphic 2 Color Look-up Table 1[0 to 255]	GR2CLUT1[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 1000h	GLCDC	Background Generating Block Operation Control Register	BGEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1004h	GLCDC	Free-Running Period Register	BGPERI	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1008h	GLCDC	Synchronization Position Register	BGSYNC	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 100Ch	GLCDC	Vertical Size Register	BGVSIZE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1010h	GLCDC	Horizontal Size Register	BGHSIZE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1014h	GLCDC	Background Color Register	BGCOLOR	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1018h	GLCDC	Background Generating Block Status Monitor Register	BGMON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1100h	GLCDC	Graphic 1 Register Update Control Register	GR1VEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1104h	GLCDC	Graphic 1 Frame Buffer Read Control Register	GR1FLMRD	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 110Ch	GLCDC	Graphic 1 Frame Buffer Control Register 2	GR1FLM2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1110h	GLCDC	Graphic 1 Frame Buffer Control Register 3	GR1FLM3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1118h	GLCDC	Graphic 1 Frame Buffer Control Register 5	GR1FLM5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 111Ch	GLCDC	Graphic 1 Frame Buffer Control Register 6	GR1FLM6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1120h	GLCDC	Graphic 1 Alpha Blending Control Register 1	GR1AB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1124h	GLCDC	Graphic 1 Alpha Blending Control Register 2	GR1AB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1128h	GLCDC	Graphic 1 Alpha Blending Control Register 3	GR1AB3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 112Ch	GLCDC	Graphic 1 Alpha Blending Control Register 4	GR1AB4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1130h	GLCDC	Graphic 1 Alpha Blending Control Register 5	GR1AB5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1134h	GLCDC	Graphic 1 Alpha Blending Control Register 6	GR1AB6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1138h	GLCDC	Graphic 1 Alpha Blending Control Register 7	GR1AB7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 113Ch	GLCDC	Graphic 1 Alpha Blending Control Register 8	GR1AB8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1140h	GLCDC	Graphic 1 Alpha Blending Control Register 9	GR1AB9	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 114Ch	GLCDC	Graphic 1 Background Color Control Register	GR1BASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1150h	GLCDC	Graphic 1 CLUT/Interrupt Control Register	GR1CLUTINT	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1154h	GLCDC	Graphic 1 Status Monitor Register	GR1MON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1200h	GLCDC	Graphic 2 Register Update Control Register	GR2VEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1204h	GLCDC	Graphic 2 Frame Buffer Read Control Register	GR2FLMRD	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 120Ch	GLCDC	Graphic 2 Frame Buffer Control Register 2	GR2FLM2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1210h	GLCDC	Graphic 2 Frame Buffer Control Register 3	GR2FLM3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1218h	GLCDC	Graphic 2 Frame Buffer Control Register 5	GR2FLM5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 121Ch	GLCDC	Graphic 2 Frame Buffer Control Register 6	GR2FLM6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1220h	GLCDC	Graphic 2 Alpha Blending Control Register 1	GR2AB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1224h	GLCDC	Graphic 2 Alpha Blending Control Register 2	GR2AB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1228h	GLCDC	Graphic 2 Alpha Blending Control Register 3	GR2AB3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 122Ch	GLCDC	Graphic 2 Alpha Blending Control Register 4	GR2AB4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1230h	GLCDC	Graphic 2 Alpha Blending Control Register 5	GR2AB5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1234h	GLCDC	Graphic 2 Alpha Blending Control Register 6	GR2AB6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1238h	GLCDC	Graphic 2 Alpha Blending Control Register 7	GR2AB7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 123Ch	GLCDC	Graphic 2 Alpha Blending Control Register 8	GR2AB8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1240h	GLCDC	Graphic 2 Alpha Blending Control Register 9	GR2AB9	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 124Ch	GLCDC	Graphic 2 Background Color Control Register	GR2BASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1250h	GLCDC	Graphic 2 CLUT/Interrupt Control Register	GR2CLUTINT	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1254h	GLCDC	Graphic 2 Status Monitor Register	GR2MON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC

I_{CC} Max. = 0.44 × f + 20 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.18 × f + 4 (ICLK 1 MHz max) (normal operation in high-speed operating mode)
I_{CC} Typ. = 0.4 × f + 1.2 (low-speed operating mode 1)
I_{CC} Max. = 0.27 × f + 20 (sleep mode)

Note 4. Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D.
The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).
Note 5. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.
Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.
Note 7. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 8. Reference value

Table 5.7 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	D version			G version			Unit	Test Conditions
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.8	1	—	0.8	1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with the channel-dedicated sample-and-hold circuits for 3 channels operating			—	1.7	2.5	—	1.7	2.5	mA	IAVCC0_AD+SH
	During 12-bit A/D conversion (unit 1)			—	0.6	1	—	0.6	1	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) with the temperature sensor operating			—	0.7	1.1	—	0.7	1.1	mA	IAVCC1_AD+TEMP
	During D/A conversion (per unit)	Unbuffered output		—	0.25	0.4	—	0.25	0.4	mA	IAVCC1_DA
		Buffered output		—	0.57	0.8	—	0.57	0.8	mA	
	Waiting for A/D, D/A, or temperature sensor conversion (all units)			—	0.9	1.4	—	0.9	1.4	mA	IAVCC0 + IAVCC1
	A/D, D/A converter, temperature sensor in standby mode (all units)			—	1.4	6.7	—	1.4	9.0	µA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)		AI_{REFH}	—	38	60	—	38	60	µA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5	—	0.07	0.6	µA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)			—	0.07	0.4	—	0.07	0.5	µA	IVREFH0
USB operating current	Low speed	USB0	$I_{CCUSBLS}$	—	3.7	6.5	—	3.7	6.5	mA	VCC_USB
	Full speed	USB0	$I_{CCUSBFS}$	—	4.2	10	—	4.2	10	mA	VCC_USB
RAM hold voltage			V_{RAM}	2.7	—	—	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	8.4	—	20000	µs/V	
VCC falling gradient*2			SfVCC	8.4	—	—	8.4	—	—	µs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D conversion (unit 1) and D/A conversion.
Note 2. This applies when V_{BATT} is used.

Table 5.8 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}	—	—	3.8	mA
	All output pins*3	High-speed interface high-drive	I_{OL}	—	—	7.5	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}	—	—	7.6	mA
	All output pins*3	High-speed interface high-drive	I_{OL}	—	—	15	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–3.8	mA
	All output pins*3	High-speed interface high-drive	I_{OH}	—	—	–7.5	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–7.6	mA
	All output pins*3	High-speed interface high-drive	I_{OH}	—	—	–15	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

Table 5.9 Heat Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Heat resistance	176-pin LFQFP (PLQP0176KB-A)	θ_{ja}	48.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		50.9		
	100-pin LFQFP (PLQP0100KB-B)		52.5		
	177-pin TFLGA (PTLG0177KA-A)		36.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		35.4		
	145-pin TFLGA (PTLG0145KA-A)		34.6		
	100-pin TFLGA (PTLG0100JA-A)		34.1		
	176-pin LFQFP (PLQP0176KB-A)	Ψ_{jt}	1.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		1.5		
	100-pin LFQFP (PLQP0100KB-B)		1.5		
	177-pin TFLGA (PTLG0177KA-A)		0.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		0.3		
	145-pin TFLGA (PTLG0145KA-A)		0.4		
	100-pin TFLGA (PTLG0100JA-A)		0.4		

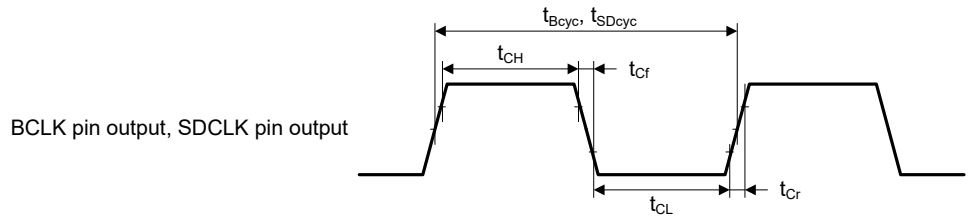
Note: The values are reference values when the 4-layer board is used. Heat resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

5.3.2 Clock Timing

Table 5.14 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	Figure 5.3
	100-pin package		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, C = 30 pF

Figure 5.3 BCLK Pin and SDCLK Pin Output Timing

Table 5.15 EXTAL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

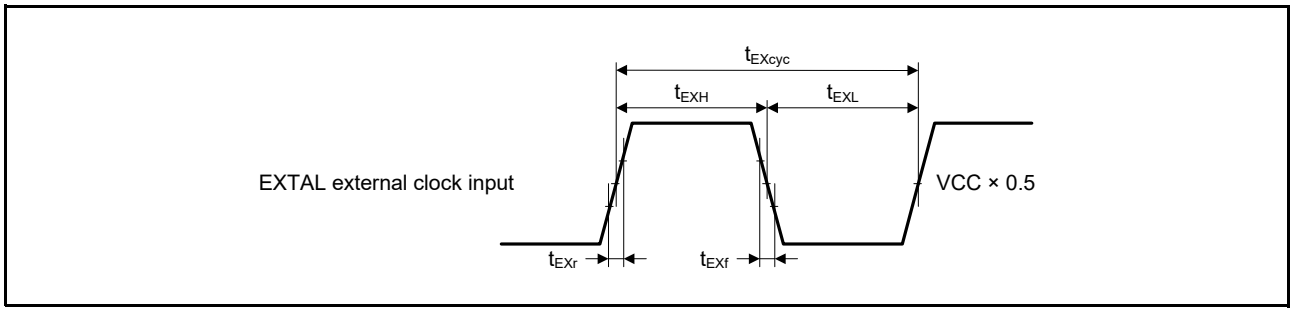


Figure 5.4 EXTAL External Clock Input Timing

Table 5.16 Main Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 5.5
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / f_{LOCO}

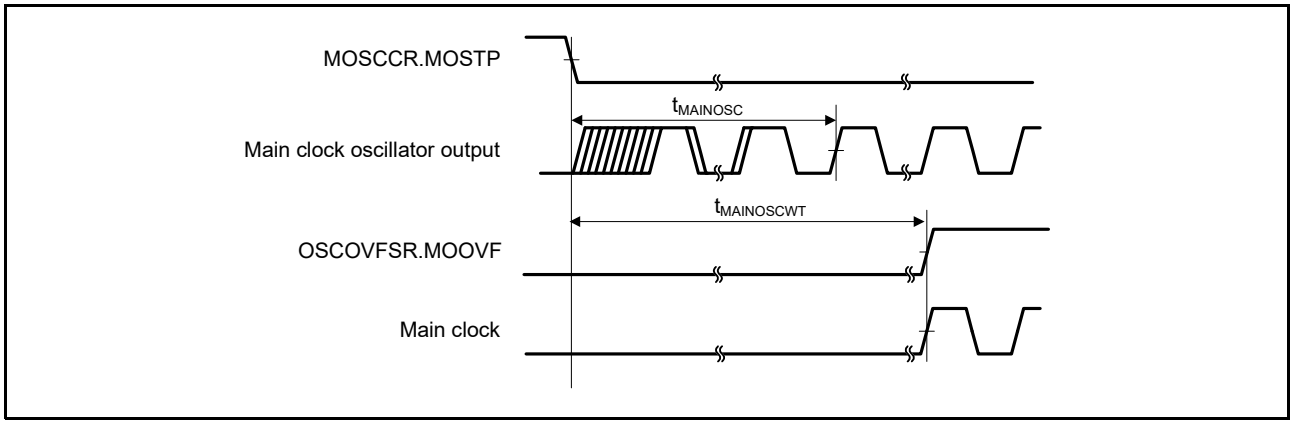


Figure 5.5 Main Clock Oscillation Start Timing

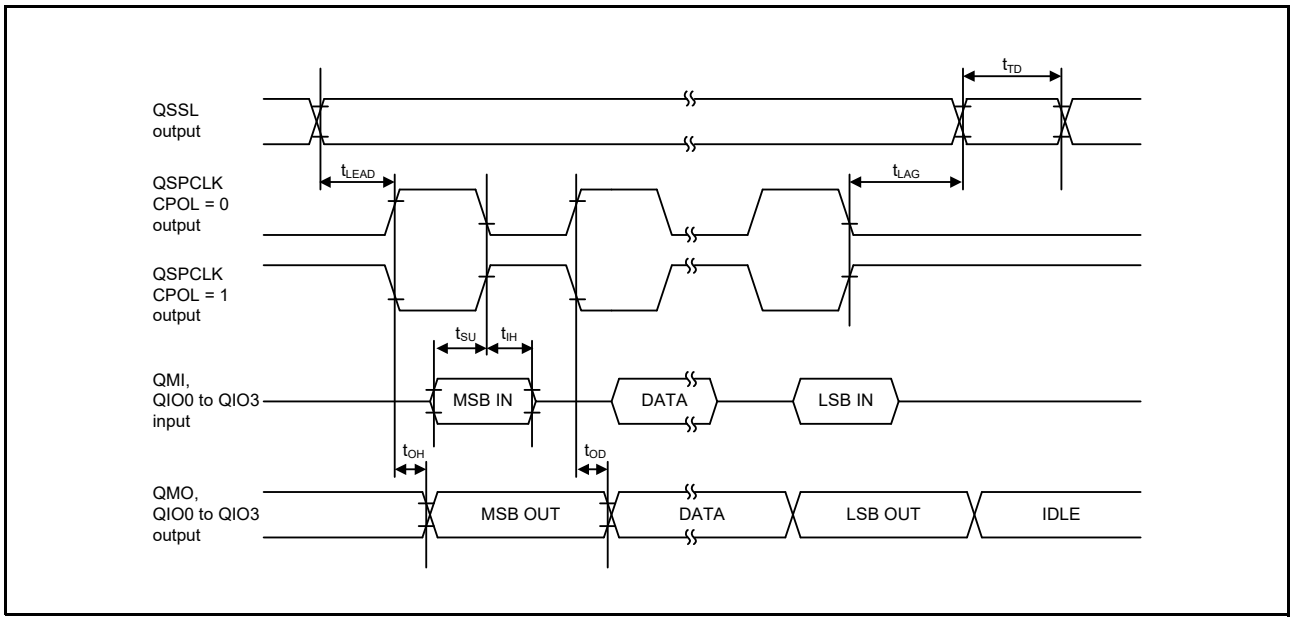


Figure 5.53 Transmit/Receive Timing (CPHA = 1)

Table 5.38 RIIC Timing (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 5.54
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

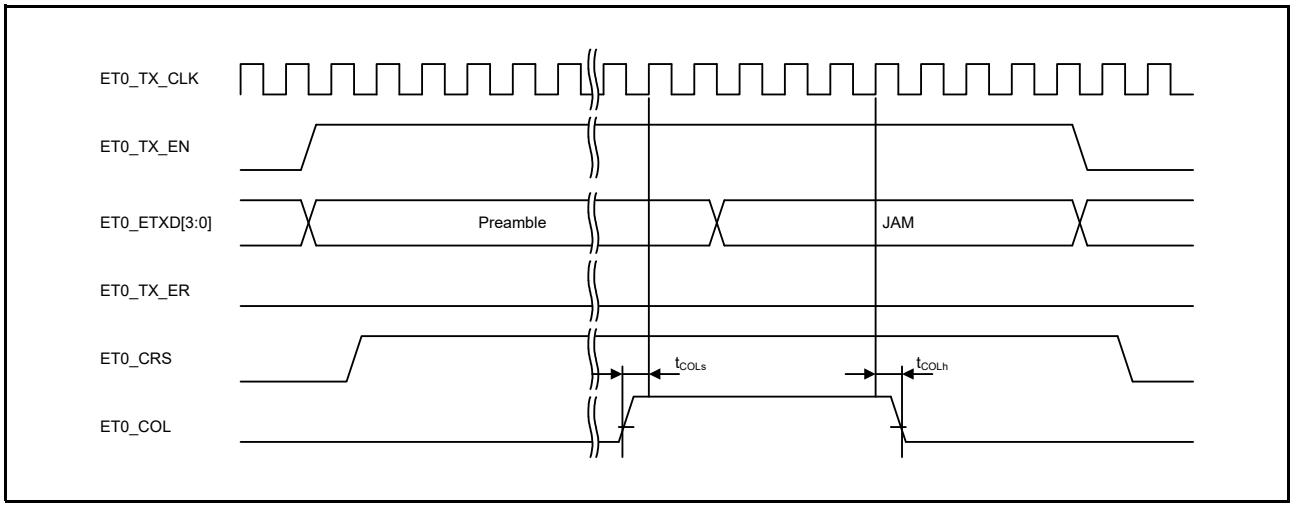


Figure 5.62 MII Transmission Timing (Conflict Occurrence)

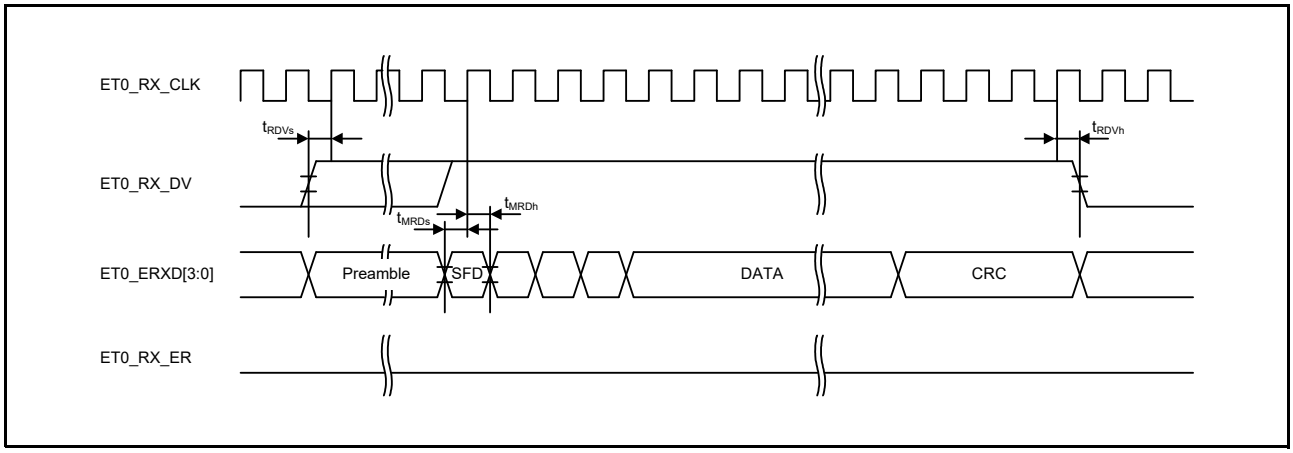


Figure 5.63 MII Reception Timing (Normal Operation)

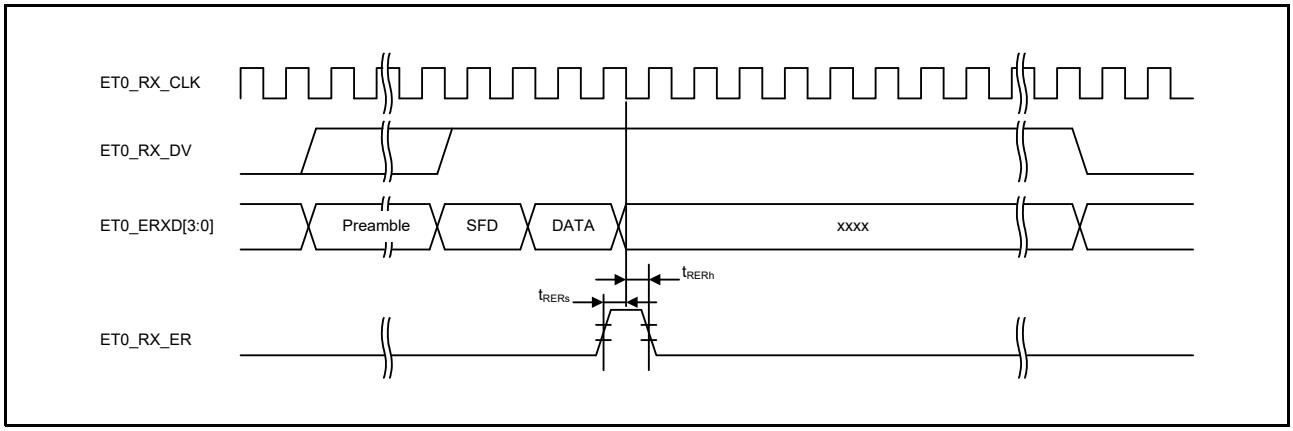


Figure 5.64 MII Reception Timing (Error Occurrence)

REVISION HISTORY	RX65N Group, RX651 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Aug 24, 2016	—	First edition, issued	
2.10	Oct 02, 2017	—	Products with at least 1.5 Mbytes of code flash memory added The conventional products indicated as “products with 1 Mbyte of code flash memory or less”	
		1. Overview		
		6, 9	Table 1.1 Outline of Specifications (5/9), Note added	TN-RX*-A164B/E
		8	Table 1.1 Outline of Specifications (8/9) Description of the 12-bit D/A converter (R12DA) changed	TN-RX*-A165A/E
		4. I/O Registers		
		131	Table 4.1 List of I/O Registers (Address Order) (46 / 61), changed	TN-RX*-A176A/E
		5. Electrical Characteristics		
		147	Table 5.1 Absolute Maximum Rating, changed	
		150	Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed	TN-RX*-A164B/E
		152	Table 5.7 DC Characteristics (4), changed	TN-RX*-A164B/E TN-RX*-A176A/E
		153	Table 5.9 Heat Resistance Value (Reference), added	
		162	Table 5.21 Timing of Recovery from Low Power Consumption Modes (1), changed	TN-RX*-A176A/E
		189	Table 5.35 RSPI Timing, changed	
		212	Table 5.49 D/A Conversion Characteristics, changed	TN-RX*-A165A/E
		218	Table 5.54 Code Flash Memory Characteristics, changed	
		219	Table 5.55 Data Flash Memory Characteristics, changed	