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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56519bdfp-30

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Safety	Clock frequency accuracy measurement circuit (CAC)	Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDG-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Encryption function	AESa*2	- Key lengths: 128, 192, and 256 bits - Support for CFB, OFB, and CMAC operating modes - Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles - Compliant with FIPS PUB 197
	True random number generator (RNG)*2	- Length of random numbers: 16 bits - Generation of random-number-generated interrupts after a number is generated - Random number generation time: 1.9 ms (typ)
	Trusted Secure IP (TSIP)*2	- Security algorithm - Common key encryption: AES (compliant with NIST FIPS PUB 197), 3DES, ARC4 - Non-common key encryption: RSA - Other features - TRNG (true-random number generator) - Hash value generation: SHA1, SHA224, SHA256, GHASH - Support of unique ID
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$, V _{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: -40 to +85°C G-version: -40 to +105°C
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-B) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-B)
On-chip debugging system		- E1 emulator (JTAG and FINE interfaces) - E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. The product part number differs according to whether or not the MCU includes the encryption function.

Note 3. The product part number differs according to whether or not the MCU includes an SDHI (SD host interface)/SDSI (SD slave interface) (products with 1 Mbyte of code flash memory or less).

Note 4. When the realtime clock is not used, initialize the registers in the time clock according to description in section 31.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.

Table 1.3 List of Products (5/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F5651EDDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651EHDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F5651CDDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651CHDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F5651EDDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651EHDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F5651CDDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651CHDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F56519ADFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56519BDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56519EDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56519FDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56517ADFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56517BDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56517EDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56517FDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56514ADFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56514BDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56514EDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56514FDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F5651EDDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651EHDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F5651CDDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651CHDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F56519ADFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56519BDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56519EDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56519FDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56517ADFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56517BDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85

Table 1.4 Pin Functions (5/8)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK0	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.
	RMII0_CRS_DV	Input	Indicate that there are carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode
	RMII0_RX_ER	Input	Indicate an error has occurred during reception of data in RMII mode.
	ET0_CRS	Input	Carrier detection/data reception enable pins
	ET0_RX_DV	Input	Indicate that there are valid receive data on ET0_ERXD3 to ET0_ERXD0.
	ET0_EXOUT	Output	General-purpose external output pins
	ET0_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable pins. Function as signals indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0.
	ET0_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY-LSI of an error during transmission.
	ET0_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timings from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER.
	ET0_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timings to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER.
	ET0_COL	Input	Input collision detection signals.
	ET0_WOL	Output	Receive Magic packets.
	ET0_MDC	Output	Output reference clock signals for information transfer via ET0_MDIO.
	ET0_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.
USB 2.0 host/function module	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB0_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA/ USB0_OVRCURB	Input	USB overcurrent pins
CAN module	USB0_VBUS	Input	USB cable connection/disconnection detection input pins
	CRX0, CRX1, CRX1-DS	Input	Input pins
	CTX0, CTX1	Output	Output pins

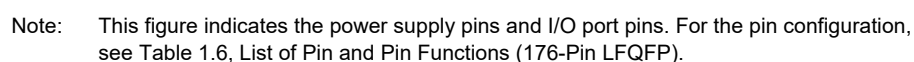


Figure 1.5 Pin Assignment (176-Pin LFQFP)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (2/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
32		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
33		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
34	TCK	PF1			SCK1				
35	TDO	PF0			TXD1/SMOSI1/ SSDA1				
36		P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB- A				
37		P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
38		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0 #
39	VCC								
40		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
41	VSS								
42		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C/PIXD7			
43		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C/PIXD6			
44		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN	SDHI_CLK-C/ PIXD5		IRQ9	
45		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID	SDHI_CMD-C/ PIXD4		IRQ8	
46		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C/PIXD3		IRQ7	ADTRG1 #
47		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C/PIXD2			
48		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
49		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
50		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface			
145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCI, RSPI, RIIC, CAN, USB)	(QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
L11		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A			
L12	TRDATA4	P73	CS3#	PO16	ET0_WOL				
L13	VSS								
M1		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C*1/ PIXD6			
M2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C*1/ PIXD3		IRQ7	ADTRG1 #
M3		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
M4		P12		TMC11	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
M5	VCC_USB								
M6	VSS_USB								
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
M8		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMC12/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A		IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A			
M10	TRDATA7	P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A			
M11		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
M12		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
M13	VCC								
N1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN	SDHI_CLK-C*1/ PIXD5		IRQ9	
N2		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID	SDHI_CMD-C*1/ PIXD4		IRQ8	
N3		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C*1/ PIXD2			
N4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
N5					USB0_DM				
N6					USB0_DP				

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (3/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
49	VSS_USB								
50		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7*1				
51	TRDATA3	P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7*1/ SMOSI7*1/ SSDA7*1/CRX1			IRQ10	
52	TRDATA2	P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMC11	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
53		P53*2	BCLK						
54		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
55		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
56		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
57	VSS								
58	TRCLK	P83	EDACK1	MTIOC4C	ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10#				
59	VCC								
60	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A	MMC_D7-A		IRQ14	
61		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMC12/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A		IRQ13	
62		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A	MMC_D5-A			
63	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10	MMC_D4-A			
64	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A			
65	TRDATA0	P80	EDREQ0	MTIOC3B/ PO26	ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10#	QIO2-A/SDHI_WP/ MMC_D2-A			
66		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMC11/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A	QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A			
67		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5	QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A			
68	TRDATA7	P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A			

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
69	TRDATA6	P76	CS6#	PO22	ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11	QSSL-A/ SDHI_CMD-A/ SDSDI_CMD-A/ MMC_CMD-A			
70		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSDI_D3-A/ MMC_CD-A			
71	TRSYNC1	P75	CS5#	PO20	ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11#	SDHI_D2-A/ SDSDI_D2-A/ MMC_RES#-A			
72	TRDATA5	P74	A20/CS4#	PO19	ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11#				
73		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
74	VCC								
75		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
76	VSS								
77	TRDATA4	P73	CS3#	PO16	ET0_WOL				
78		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSDI_D1-B			
79		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSDI_D0-B			
80		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSDI_CLK-B	LCD_CL K-B*1		
81		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSDI_CMD-B	LCD_TC ON0-B*1		
82		PB3	A11	MTIOC0A/ MTIOC4A/ TIOC3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6	SDSDI_D3-B	LCD_TC ON1-B*1		
83		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSDI_D2-B	LCD_TC ON2-B*1		
84		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		LCD_TC ON3-B*1	IRQ4-DS	
85		P72	A19/CS2#		ET0_MDC				
86		P71	A18/CS1#		ET0_MDIO				

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
45	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A			IRQ14	
46		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A			IRQ13	
47		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A				
48		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A				
49		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5				
50		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A				
51		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
52		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
53		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
54		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
55		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CL K-B*1		
56		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TC ON0-B*1		
57		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK6	SDSI_D3-B	LCD_TC ON1-B*1		
58		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6#	SDSI_D2-B	LCD_TC ON2-B*1		
59		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6		LCD_TC ON3-B*1	IRQ4-DS	

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).

The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
 Number of divided clock synchronization cycles +
 Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

(5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

Table 4.1 List of I/O Registers (Address Order) (9 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7709h	ICU	Software Configurable Interrupt B Request Register 9	PIBR9	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 770Ah	ICU	Software Configurable Interrupt B Request Register A	PIBRA	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 770Bh	ICU	Software Configurable Interrupt B Request Register B	PIBRB	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7780h	ICU	Software Configurable Interrupt B Source Select Register X128	SLIBXR128	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7781h	ICU	Software Configurable Interrupt B Source Select Register X129	SLIBXR129	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7782h	ICU	Software Configurable Interrupt B Source Select Register X130	SLIBXR130	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7783h	ICU	Software Configurable Interrupt B Source Select Register X131	SLIBXR131	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7784h	ICU	Software Configurable Interrupt B Source Select Register X132	SLIBXR132	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7785h	ICU	Software Configurable Interrupt B Source Select Register X133	SLIBXR133	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7786h	ICU	Software Configurable Interrupt B Source Select Register X134	SLIBXR134	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7787h	ICU	Software Configurable Interrupt B Source Select Register X135	SLIBXR135	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7788h	ICU	Software Configurable Interrupt B Source Select Register X136	SLIBXR136	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7789h	ICU	Software Configurable Interrupt B Source Select Register X137	SLIBXR137	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Ah	ICU	Software Configurable Interrupt B Source Select Register X138	SLIBXR138	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Bh	ICU	Software Configurable Interrupt B Source Select Register X139	SLIBXR139	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Ch	ICU	Software Configurable Interrupt B Source Select Register X140	SLIBXR140	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Dh	ICU	Software Configurable Interrupt B Source Select Register X141	SLIBXR141	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Eh	ICU	Software Configurable Interrupt B Source Select Register X142	SLIBXR142	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Fh	ICU	Software Configurable Interrupt B Source Select Register X143	SLIBXR143	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7790h	ICU	Software Configurable Interrupt B Source Select Register 144	SLIBR144	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7791h	ICU	Software Configurable Interrupt B Source Select Register 145	SLIBR145	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7792h	ICU	Software Configurable Interrupt B Source Select Register 146	SLIBR146	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7793h	ICU	Software Configurable Interrupt B Source Select Register 147	SLIBR147	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7794h	ICU	Software Configurable Interrupt B Source Select Register 148	SLIBR148	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7795h	ICU	Software Configurable Interrupt B Source Select Register 149	SLIBR149	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7796h	ICU	Software Configurable Interrupt B Source Select Register 150	SLIBR150	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7797h	ICU	Software Configurable Interrupt B Source Select Register 151	SLIBR151	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7798h	ICU	Software Configurable Interrupt B Source Select Register 152	SLIBR152	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7799h	ICU	Software Configurable Interrupt B Source Select Register 153	SLIBR153	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Ah	ICU	Software Configurable Interrupt B Source Select Register 154	SLIBR154	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Bh	ICU	Software Configurable Interrupt B Source Select Register 155	SLIBR155	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Ch	ICU	Software Configurable Interrupt B Source Select Register 156	SLIBR156	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (25 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A046h	SMCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A049h	SCI2	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Ah	SCI2	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Bh	SCI2	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Ch	SCI2	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Eh	SCI2	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Fh	SCI2	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Eh	SCI2	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A050h	SCI2	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A051h	SCI2	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A050h	SCI2	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A052h	SCI2	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A066h	SMCI3	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli

Table 5.12 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	32	—	264	kHz
	Peripheral module clock (PCLKA)			—	—	264	
	Peripheral module clock (PCLKB)			—	—	264	
	Peripheral module clock (PCLKC)* ¹			—	—	264	
	Peripheral module clock (PCLKD)* ¹			—	—	264	
	Flash-IF clock (FCLK)			32	—	264	
	External bus clock (BCLK)	Other than 100-pin package		—	—	264	
		100-pin package		—	—	264	
	BCLK pin output	Other than 100-pin package		—	—	264	
		100-pin package		—	—	264	
	SDRAM clock (SDCLK)	Other than 100-pin package		—	—	264	
	SDCLK pin output	Other than 100-pin package		—	—	264	

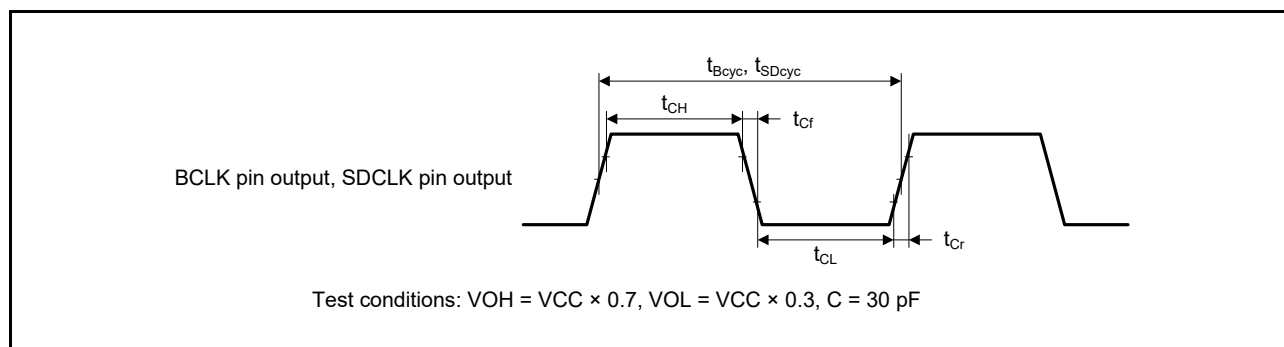
Note 1. The 12-bit A/D converter cannot be used.

5.3.2 Clock Timing

Table 5.14 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	Figure 5.3
	100-pin package		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	

**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

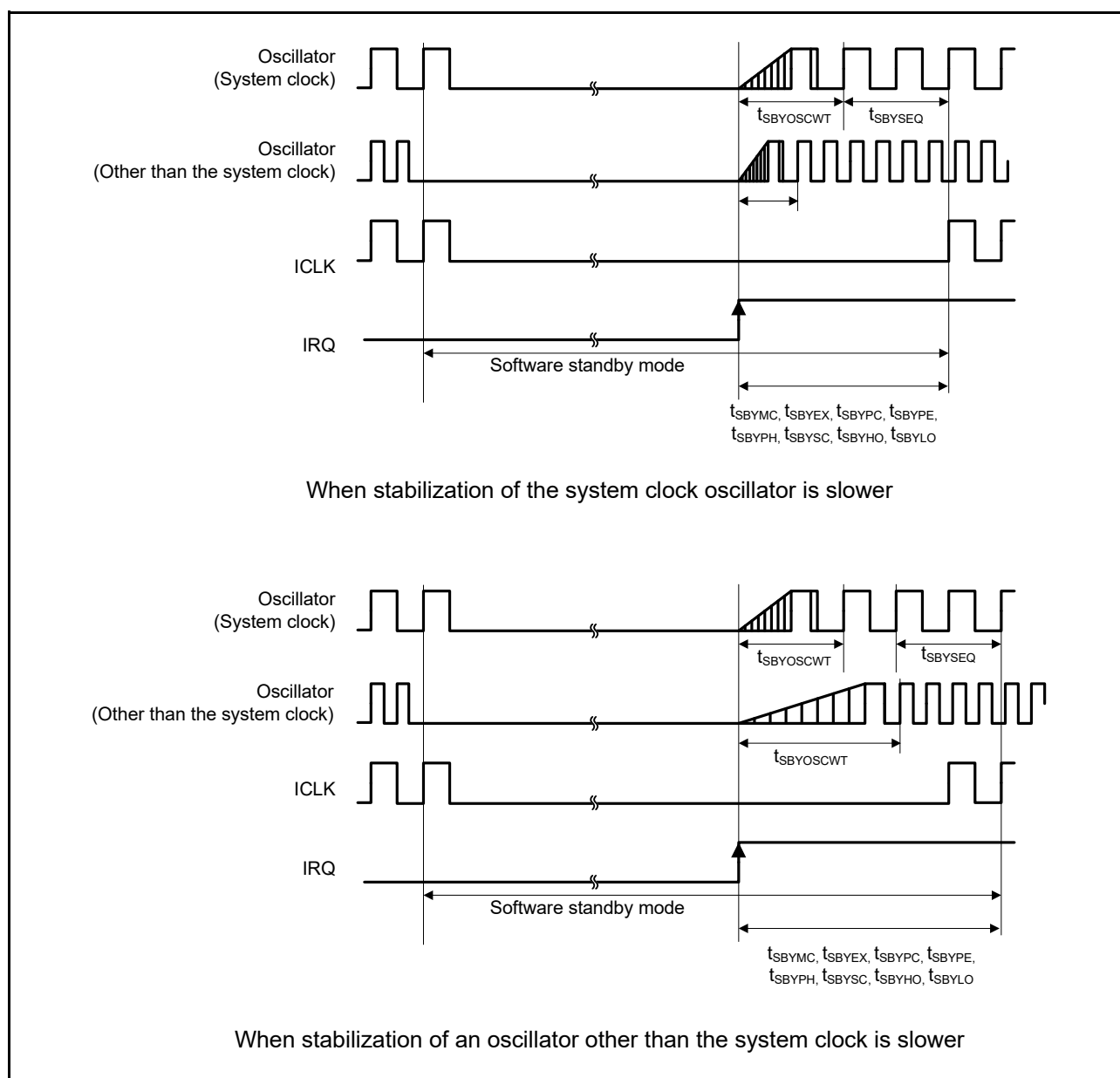


Figure 5.12 Software Standby Mode Cancellation Timing

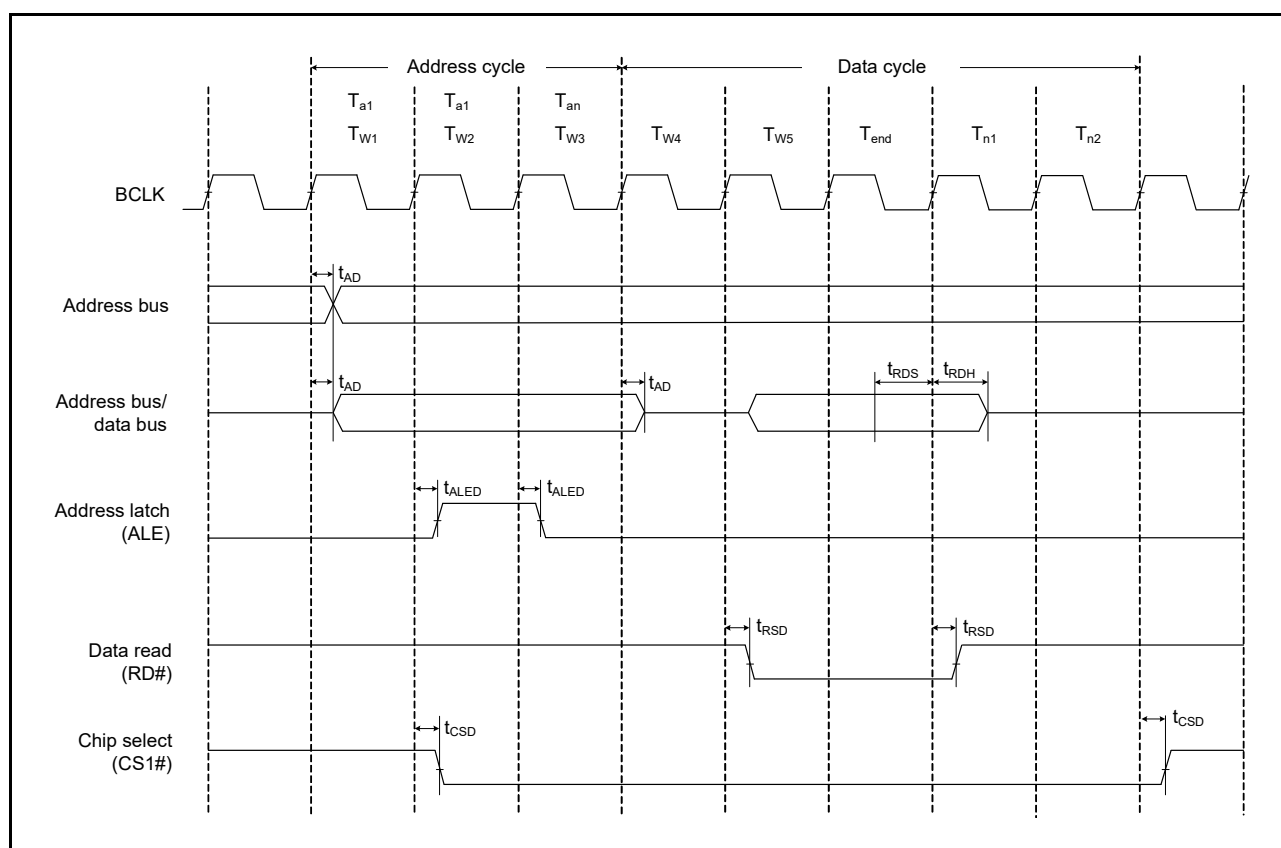


Figure 5.16 Address/Data Multiplexed Bus Read Access Timing

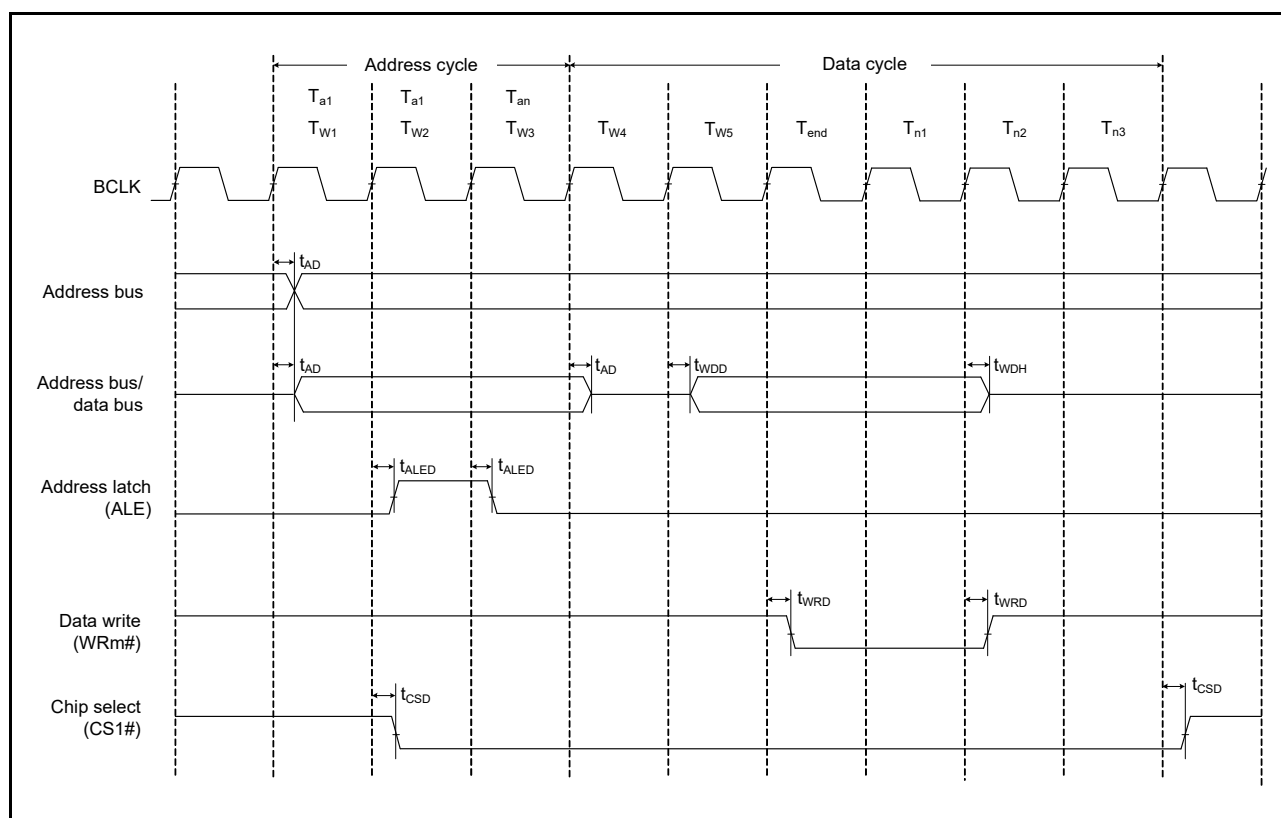


Figure 5.17 Address/Data Multiplexed Bus Write Access Timing

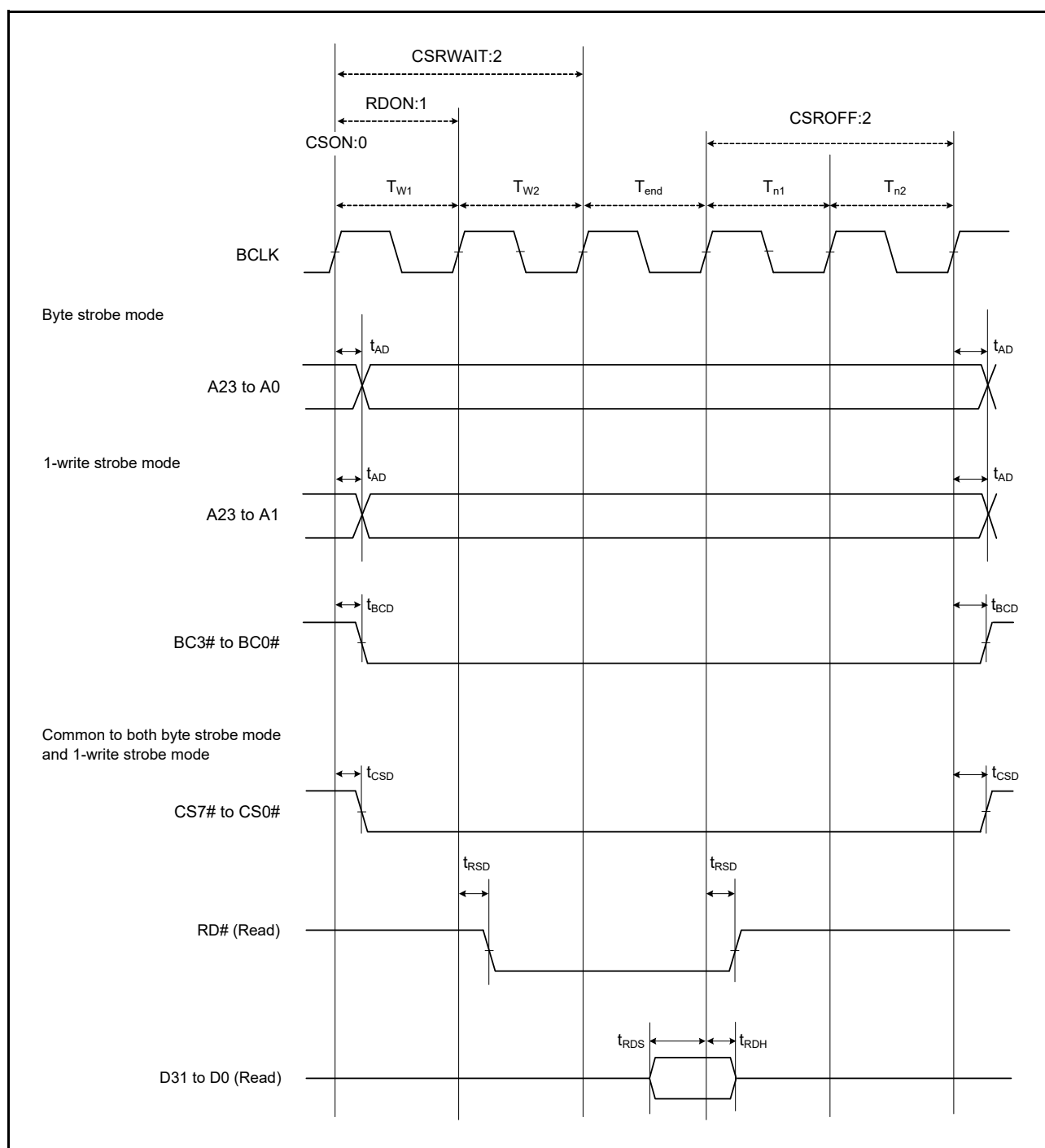
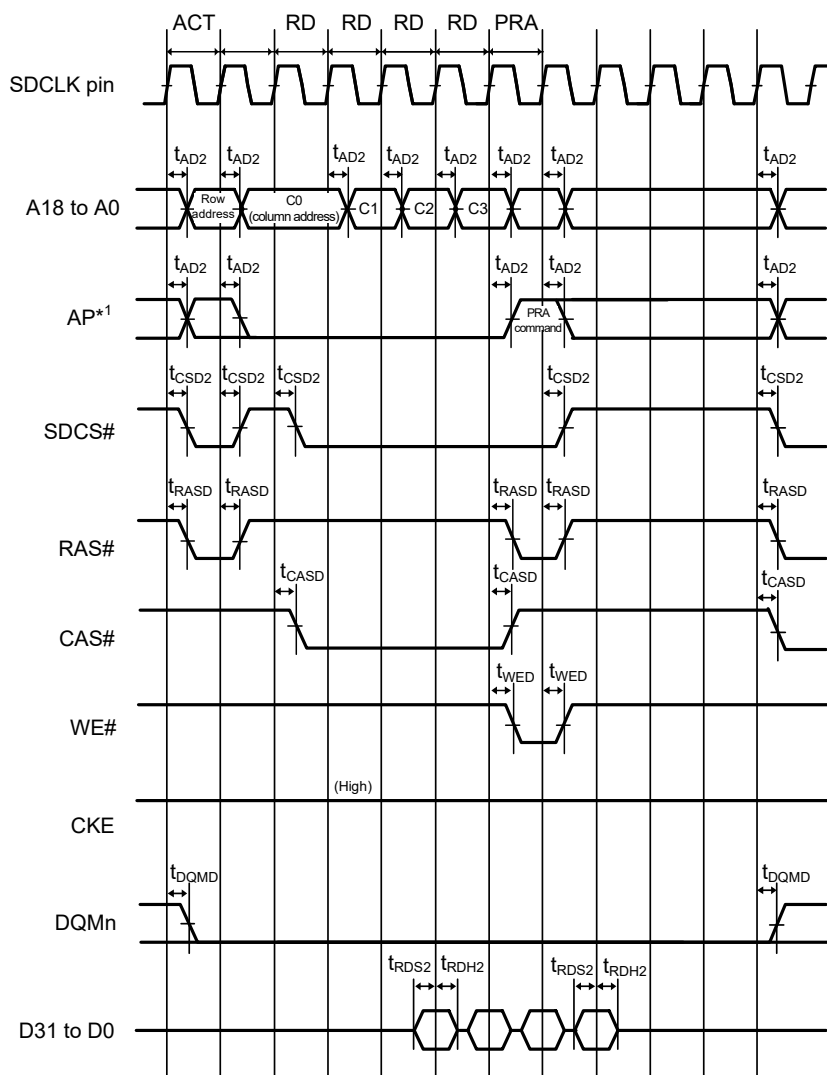


Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.25 SDRAM Space Multiple Read Bus Timing

Table 5.47 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKB = PCLKD = 1$ MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Conversion time*1 (Operation at PCLK = 60 MHz)	Permissible signal source impedance (max.) = 1.0 kΩ	0.88 (0.633)*2	—	—	μs	Sampling in 38 states (ADSAM.SAM = 1)
Conversion time*1 (Operation at PCLK = 30 MHz)		1 (0.500)*2	—	—	μs	Sampling in 15 states (ADSAM.SAM = 1)
Analog input capacitance		—	—	30	pF	
Offset error		—	±2.0	±3.5	LSB	
Full-scale error		—	±2.0	±3.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±4.0	±6.0	LSB	
DNL differential nonlinearity error (Operation at PCLK = 60 MHz)		—	±1.5	±4.0	LSB	
DNL differential nonlinearity error (Operation at PCLK = 30 MHz)		—	±1.5	±2.5	LSB	
INL integral nonlinearity error (Operation at PCLK = 60 MHz)		—	±2.0	±4.0	LSB	
INL integral nonlinearity error (Operation at PCLK = 30 MHz)		—	±2.0	±3.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.48 A/D Internal Reference Voltage Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKB = PCLKD = 60$ MHz, $T_a = T_{opr}$

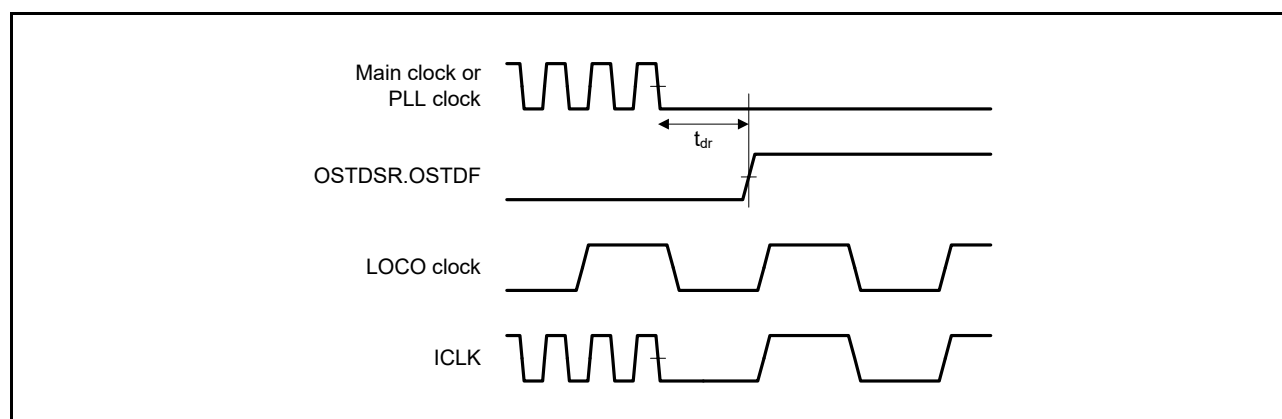
Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.13	1.18	1.23	V	

5.9 Oscillation Stop Detection Timing

Table 5.52 Oscillation Stop Detection Circuit Characteristics

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq VREFH0 \leq AVCC0$,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.80

**Figure 5.80 Oscillation Stop Detection Timing**