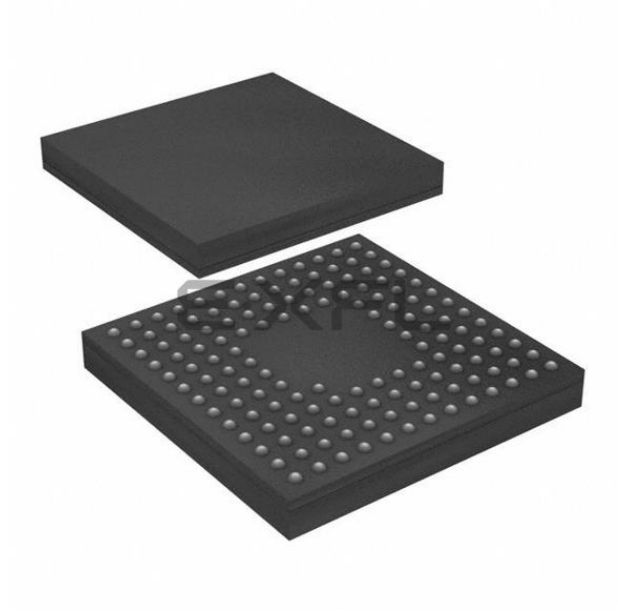

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56519bdlk-20

Table 1.3 List of Products (4/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (G version)	R5F565N7AGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F565N7BGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F565N7EGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F565N7FGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F565N4AGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F565N4BGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F565N4EGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F565N4FGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F565NEDGFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NEHGFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565NCDGFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NCHGFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565N9AGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F565N9BGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F565N9EGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F565N9FGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F565N7AGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F565N7BGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F565N7EGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F565N7FGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F565N4AGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F565N4BGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F565N4EGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F565N4FGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105

Table 1.3 List of Products (5/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F5651EDDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651EDDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F56519ADFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56519BDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56519EDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56519FDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56517ADFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56517BDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56517EDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56517FDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56514ADFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56514BDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56514EDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56514FDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F5651EDDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F56519ADFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56519BDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56519EDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56519FDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56517ADFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56517BDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (5/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
92	VSS								
93		P73	CS3#	PO16	ET0_WOL		LCD_EXTCLK-A		
94		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
95		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
96		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CLK-B		
97		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B		
98		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6	SDSI_D3-B	LCD_TCON1-B		
99		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2-B	LCD_TCON2-B		
100		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		LCD_TCON3-B	IRQ4-DS	
101		P72	A19/CS2#		ET0_MDC		LCD_DATA23-A		
102		P71	A18/CS1#		ET0_MDIO				
103	VCC								
104		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DATA0-B	IRQ12	
105	VSS								
106		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B		
107		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B		
108		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B		

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)

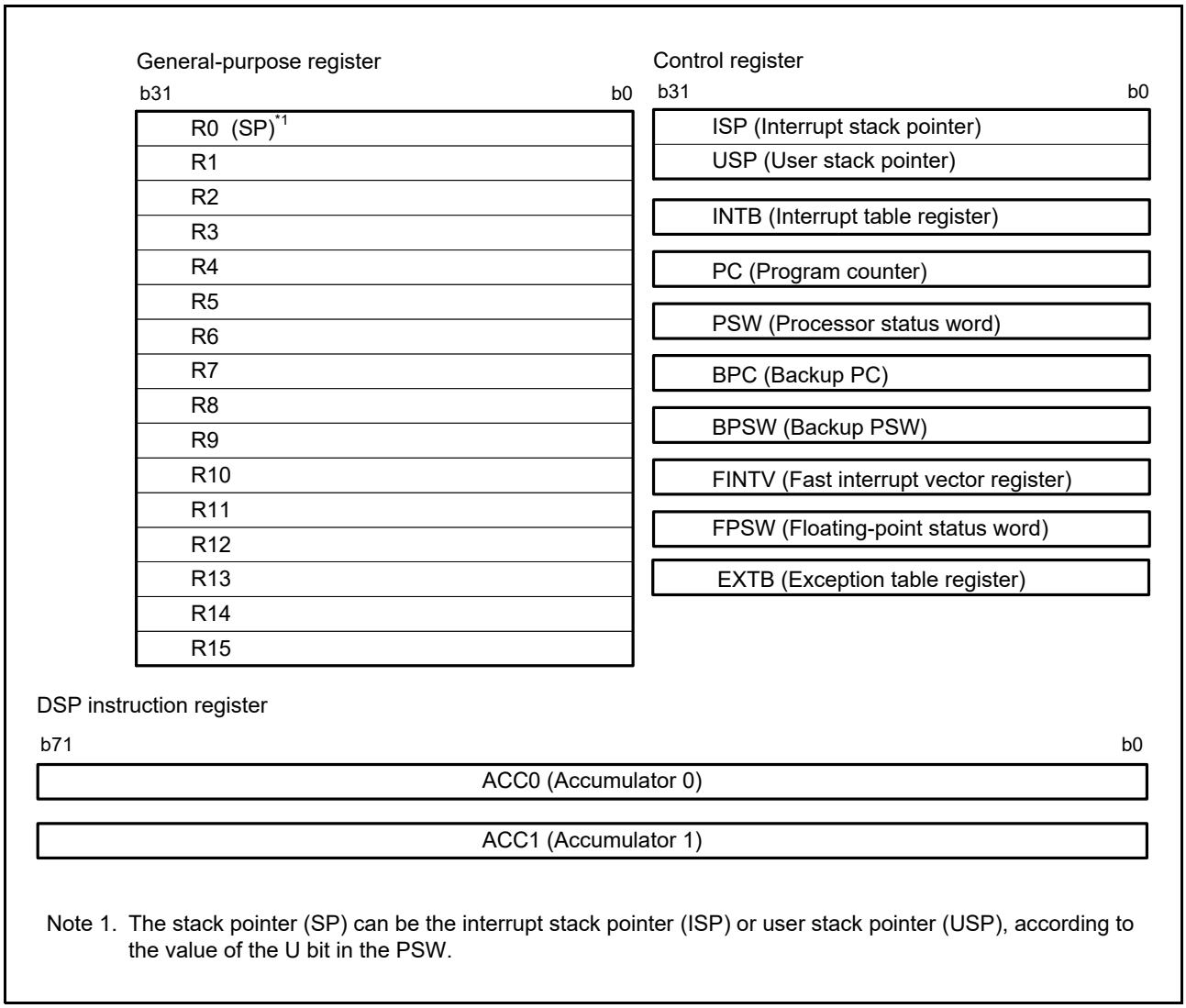
Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
E4	EMLE								
E5		P44						IRQ12-DS	AN004
E10		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DATA8-B*1		
E11		P66	DQM0/CS6#	MTIOC7D					
E12		P65	CKE/CS5#						
E13		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	XCIN								
F2	XCOUT								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
F4	VBATT								
F10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DATA5-B*1	IRQ6-DS	
F11	VSS								
F12		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DATA7-B*1	IRQ11	
F13		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DATA6-B*1		
G1	XTAL	P37							
G2	RES#								
G3	MD/FINED								
G4	BSCANP								
G10		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B*1		
G11		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B*1		
G12	VCC								
G13		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DATA4-B*1	IRQ5-DS	
H1	EXTAL	P36							
H2	VCC								
H3	VSS								
H4	UPSEL	P35						NMI	
H10		P72	A19/CS2#		ET0_MDC				
H11		P71	A18/CS1#		ET0_MDIO				

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
45	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A			IRQ14	
46		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A			IRQ13	
47		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A				
48		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A				
49		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5				
50		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A				
51		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
52		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
53		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
54		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
55		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CLK-B*1		
56		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B*1		
57		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK6	SDSI_D3-B	LCD_TCON1-B*1		
58		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6#	SDSI_D2-B	LCD_TCON2-B*1		
59		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6		LCD_TCON3-B*1	IRQ4-DS	

2. CPU

Figure 2.1 shows register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (8 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK		ICUB
0008 72E1h	ICU	Software Interrupt 2 Generation Register	SWINT2R	8	8	2 ICLK		ICUB
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK		ICUB
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Registers 000 to 255	IPR000 to IPR255	8	8	2 ICLK		ICUB
0008 7400h	ICU	DMAC Trigger Select Register 0	DMRSR0	8	8	2 ICLK		ICUB
0008 7404h	ICU	DMAC Trigger Select Register 1	DMRSR1	8	8	2 ICLK		ICUB
0008 7408h	ICU	DMAC Trigger Select Register 2	DMRSR2	8	8	2 ICLK		ICUB
0008 740Ch	ICU	DMAC Trigger Select Register 3	DMRSR3	8	8	2 ICLK		ICUB
0008 7410h	ICU	DMAC Trigger Select Register 4	DMRSR4	8	8	2 ICLK		ICUB
0008 7414h	ICU	DMAC Trigger Select Register 5	DMRSR5	8	8	2 ICLK		ICUB
0008 7418h	ICU	DMAC Trigger Select Register 6	DMRSR6	8	8	2 ICLK		ICUB
0008 741Ch	ICU	DMAC Trigger Select Register 7	DMRSR7	8	8	2 ICLK		ICUB
0008 7500h to 0008 750Fh	ICU	IRQ Control Registers 0 to 15	IRQCR0 to 15	8	8	2 ICLK		ICUB
0008 7520h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUB
0008 7521h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK		ICUB
0008 7528h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK		ICUB
0008 752Ah	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK		ICUB
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK		ICUB
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK		ICUB
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK		ICUB
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK		ICUB
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK		ICUB
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK		ICUB
0008 7600h	ICU	Group BE0 Interrupt Request Register	GRPBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7630h	ICU	Group BL0 Interrupt Request Register	GRPBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7634h	ICU	Group BL1 Interrupt Request Register	GRPBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7638h	ICU	Group BL2 Interrupt Request Register	GRPBL2	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7640h	ICU	Group BE0 Interrupt Request Enable Register	GENBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7670h	ICU	Group BL0 Interrupt Request Enable Register	GENBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7674h	ICU	Group BL1 Interrupt Request Enable Register	GENBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7678h	ICU	Group BL2 Interrupt Request Enable Register	GENBL2	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7680h	ICU	Group BE0 Interrupt Clear Register	GCRBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7700h	ICU	Software Configurable Interrupt B Request Register 0	PIBR0	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7701h	ICU	Software Configurable Interrupt B Request Register 1	PIBR1	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7702h	ICU	Software Configurable Interrupt B Request Register 2	PIBR2	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7703h	ICU	Software Configurable Interrupt B Request Register 3	PIBR3	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7704h	ICU	Software Configurable Interrupt B Request Register 4	PIBR4	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7705h	ICU	Software Configurable Interrupt B Request Register 5	PIBR5	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7706h	ICU	Software Configurable Interrupt B Request Register 6	PIBR6	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7707h	ICU	Software Configurable Interrupt B Request Register 7	PIBR7	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7708h	ICU	Software Configurable Interrupt B Request Register 8	PIBR8	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (38 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C0C1h	PORT1	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C2h	PORT2	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C3h	PORT3	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C4h	PORT4	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C5h	PORT5	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C6h	PORT6	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C7h	PORT7	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C8h	PORT8	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C9h	PORT9	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CAh	PORTA	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CBh	PORTB	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CCh	PORTC	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CDh	PORTD	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CEh	PORTE	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CFh	PORTF	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0D0h	PORTG	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0D2h	PORTJ	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0F0h	PORTG	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC

Table 4.1 List of I/O Registers (Address Order) (55 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 0044h	SCI10	Serial Status Register	SSR/ SSRFIFO	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0045h	SCI10	Receive Data Register	RDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0046h	SMCI10	Smart Card Mode Register	SCMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0047h	SCI10	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0048h	SCI10	Noise Filter Setting Register	SNFR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0049h	SCI10	I2C Mode Register 1	SIMR1	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Ah	SCI10	I2C Mode Register 2	SIMR2	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Bh	SCI10	I2C Mode Register 3	SIMR3	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Ch	SCI10	I2C Status Register	SISR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Dh	SCI10	SPI Mode Register	SPMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Eh	SCI10	Transmit Data Register H	TDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Fh	SCI10	Transmit Data Register L	TDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Eh	SCI10	Transmit Data Register HL	TDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 004Eh	SCI10	Transmit FIFO Data Register	FTDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Fh	SCI10	Transmit FIFO Data Register	FTDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Eh	SCI10	Transmit FIFO Data Register	FTDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0050h	SCI10	Receive Data Register H	RDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0051h	SCI10	Receive Data Register L	RDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0050h	SCI10	Receive Data Register HL	RDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0050h	SCI10	Receive FIFO Data Register	FRDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0051h	SCI10	Receive FIFO Data Register	FRDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0050h	SCI10	Receive FIFO Data Register	FRDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0052h	SCI10	Modulation Duty Register	MDDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0053h	SCI10	Data Comparison Control Register	DCCR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0054h	SCI10	FIFO Control Register	FCR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0055h	SCI10	FIFO Control Register	FCR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0054h	SCI10	FIFO Control Register	FCR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0056h	SCI10	FIFO Data Count Register	FDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0057h	SCI10	FIFO Data Count Register	FDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0056h	SCI10	FIFO Data Count Register	FDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0058h	SCI10	Line Status Register	LSR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0059h	SCI10	Line Status Register	LSR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0058h	SCI10	Line Status Register	LSR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 005Ah	SCI10	Comparison Data Register	CDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 005Bh	SCI10	Comparison Data Register	CDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 005Ah	SCI10	Comparison Data Register	CDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 005Ch	SCI10	Serial Port Register	SPTR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0060h	SCI11	Serial Mode Register	SMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0061h	SCI11	Bit Rate Register	BRR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0062h	SCI11	Serial Control Register	SCR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0063h	SCI11	Transmit Data Register	TDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0064h	SCI11	Serial Status Register	SSR/ SSRFIFO	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0065h	SCI11	Receive Data Register	RDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0066h	SMCI11	Smart Card Mode Register	SCMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0067h	SCI11	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0068h	SCI11	Noise Filter Setting Register	SNFR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0069h	SCI11	I2C Mode Register 1	SIMR1	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Ah	SCI11	I2C Mode Register 2	SIMR2	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Bh	SCI11	I2C Mode Register 3	SIMR3	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi

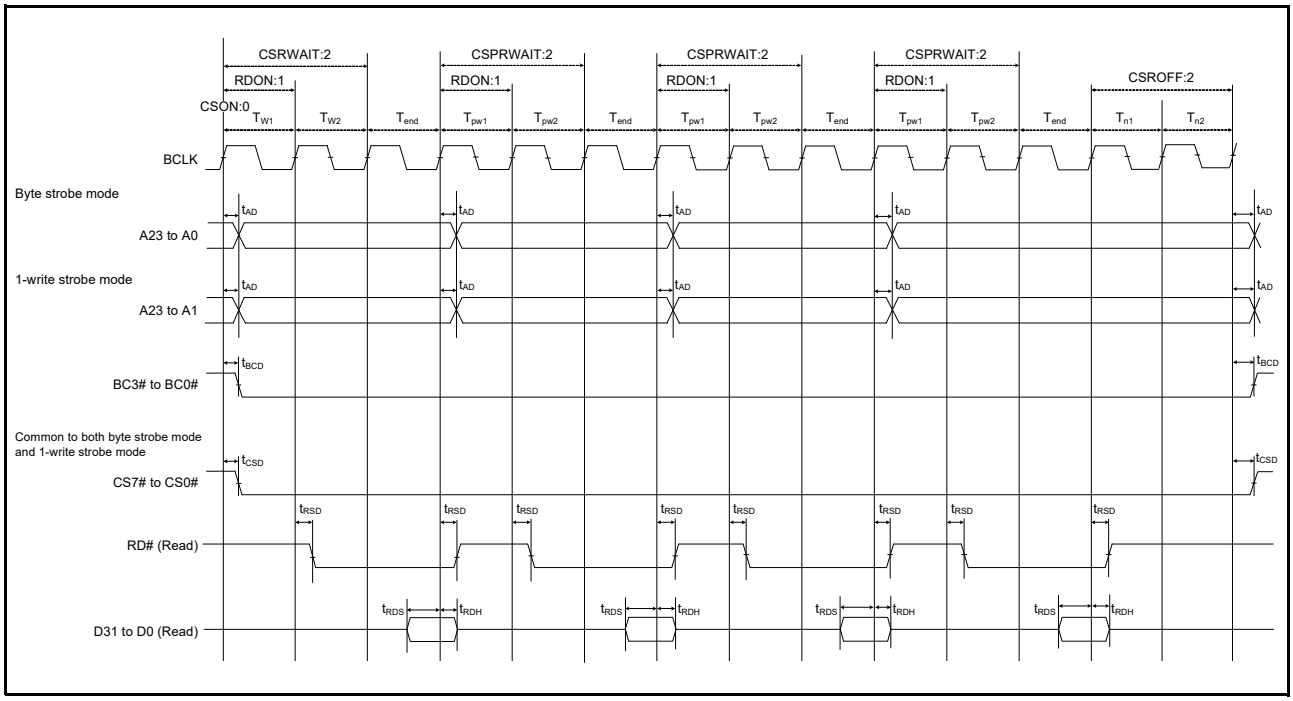


Figure 5.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

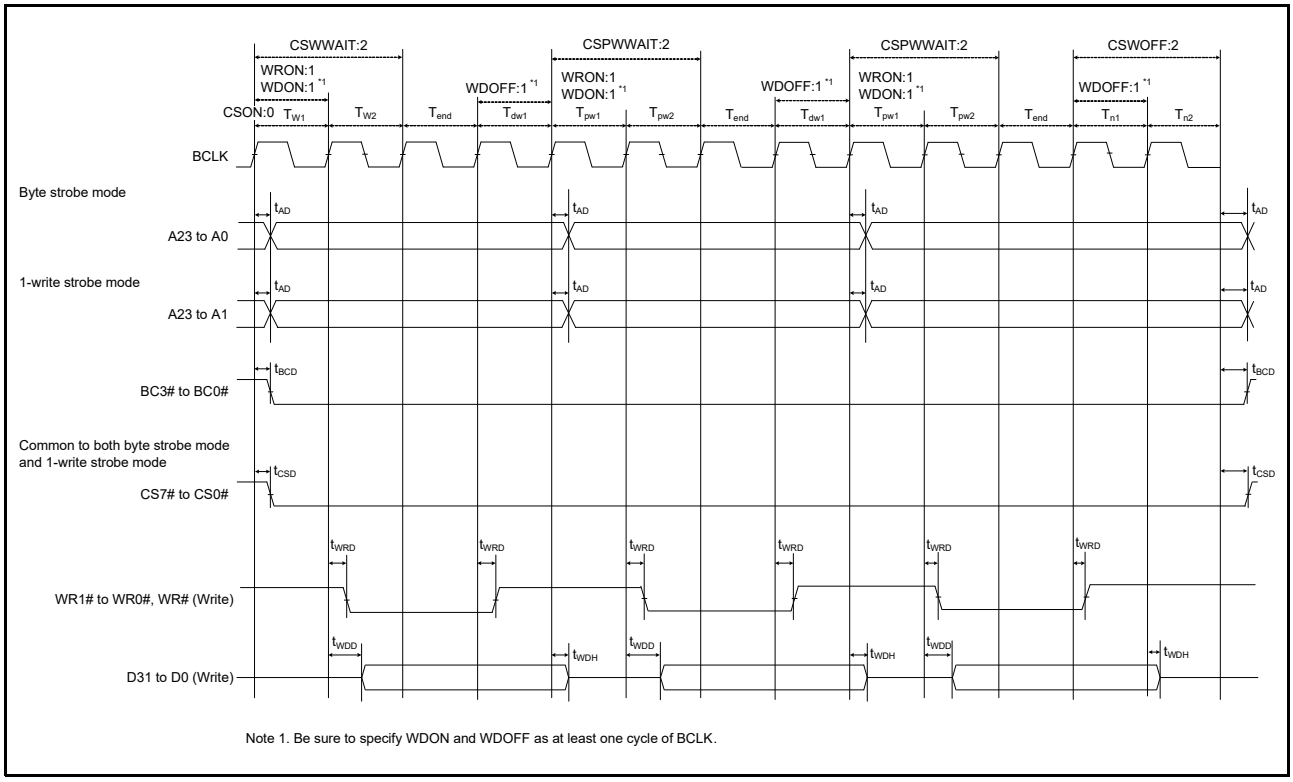


Figure 5.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

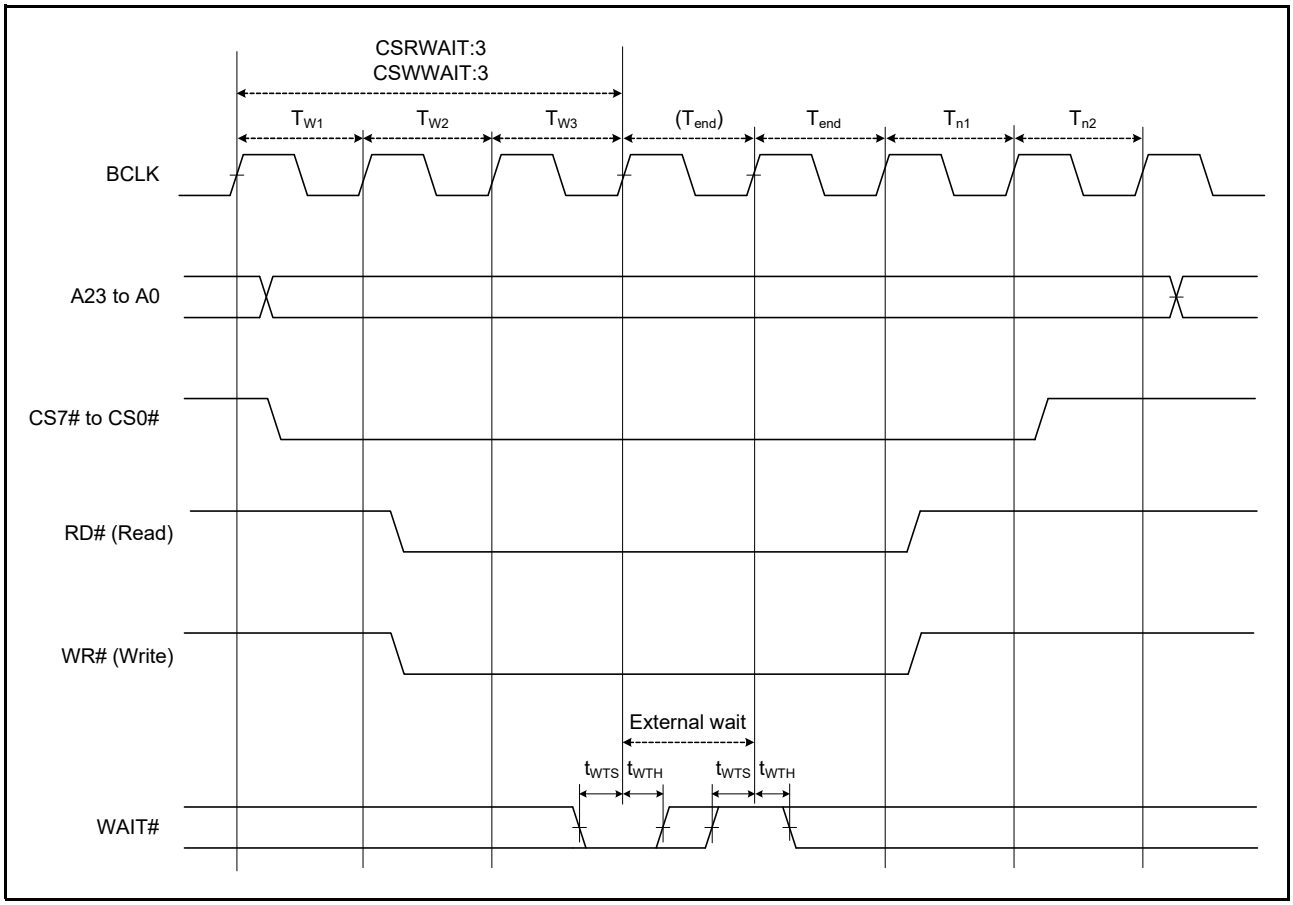


Figure 5.22 External Bus Timing/External Wait Control

Table 5.41 ETHERC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.56 to Figure 5.58
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII0_xxxx*2 setup time	T_{su}	3	—	ns	
	RMII0_xxxx*2 hold time	T_{hd}	1	—	ns	
	RMII0_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.60
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET0_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.61
	ET0_ETXD0 to ET0_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET0_CRS setup time	t_{CRSs}	10	—	ns	
	ET0_CRS hold time	t_{CRSh}	10	—	ns	
	ET0_COL setup time	t_{COLs}	10	—	ns	Figure 5.62
	ET0_COL hold time	t_{COLh}	10	—	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET0_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 5.63
	ET0_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET0_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.64
	ET0_RX_ER hold time	t_{RERh}	10	—	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.65

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

Table 5.42 PDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	—	ns	Figure 5.66
	PIXCLK input high pulse width	t_{PIXH}	10	—	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	—	ns	
	PIXCLK rising time	t_{PIXr}	—	5	ns	
	PIXCLK falling time	t_{PIXf}	—	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	—	ns	Figure 5.67
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO rising time	t_{PCKr}	—	5	ns	
	PCKO falling time	t_{PCKf}	—	5	ns	
	VSYNC/HSYNC input setup time	t_{SYNCS}	10	—	ns	Figure 5.68
	VSYNC/HSYNC input hold time	t_{SYNCH}	5	—	ns	
	PIXD input setup time	t_{PIXDS}	10	—	ns	
	PIXD input hold time	t_{PIXDH}	5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

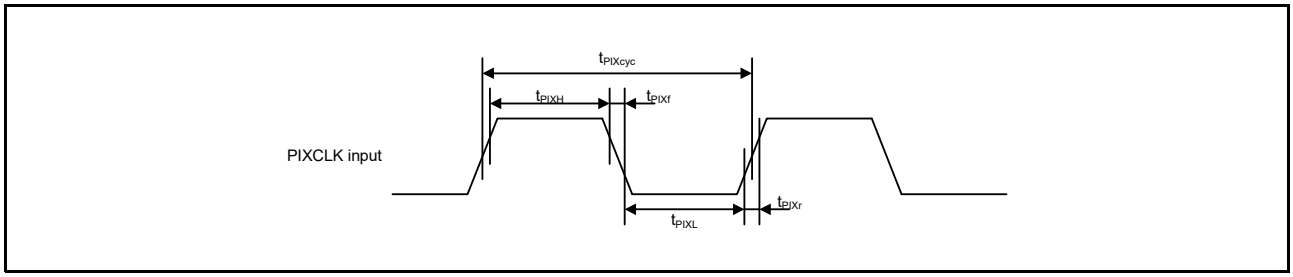


Figure 5.66 PDC Input Clock Timing

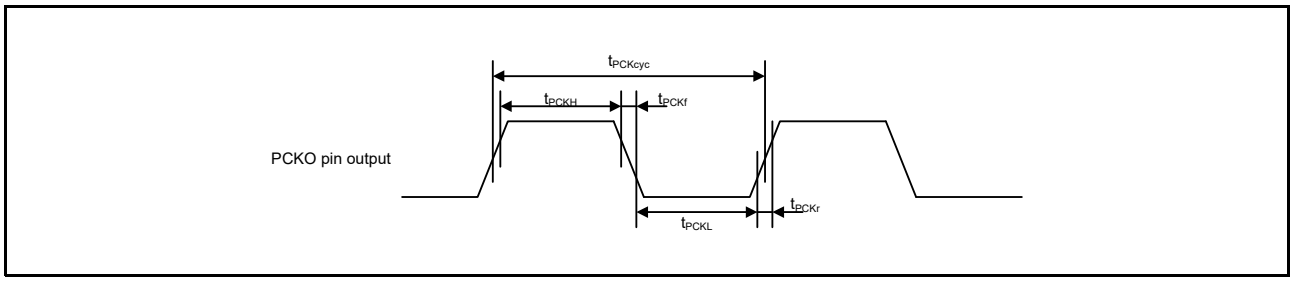


Figure 5.67 PDC Output Clock Timing

5.6 D/A Conversion Characteristics

Table 5.49 D/A Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	12	12	12	Bit	
Unbuffered output	Absolute accuracy	—	—	—	±6.0	LSB	2-MΩ resistive load 10-bit conversion
	Differential nonlinearity error	DNL	—	±1.0	±2.0	LSB	2-MΩ resistive load
	Output resistance	R_O	—	8.6	—	kΩ	
	Setting time	t_S	—	—	3	μs	20-pF capacitive load
Buffered output	Load resistance	R_L	5	—	—	kΩ	
	Load capacitance	C_L	—	—	50	pF	
	Output voltage	V_O	0.2	—	AVCC1 – 0.2	V	
	Differential nonlinearity error	DNL	—	±1.0	±2.0	LSB	
	Integral nonlinearity error	INL	—	±2.0	±4.0	LSB	
	Setting time	t_S	—	—	4	μs	

5.7 Temperature Sensor Characteristics

Table 5.50 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4	—	mV/°C	
Output voltage (at 25°C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	μs	
Sampling time*1	4.15	—	—	μs	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

5.9 Oscillation Stop Detection Timing

Table 5.52 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.80

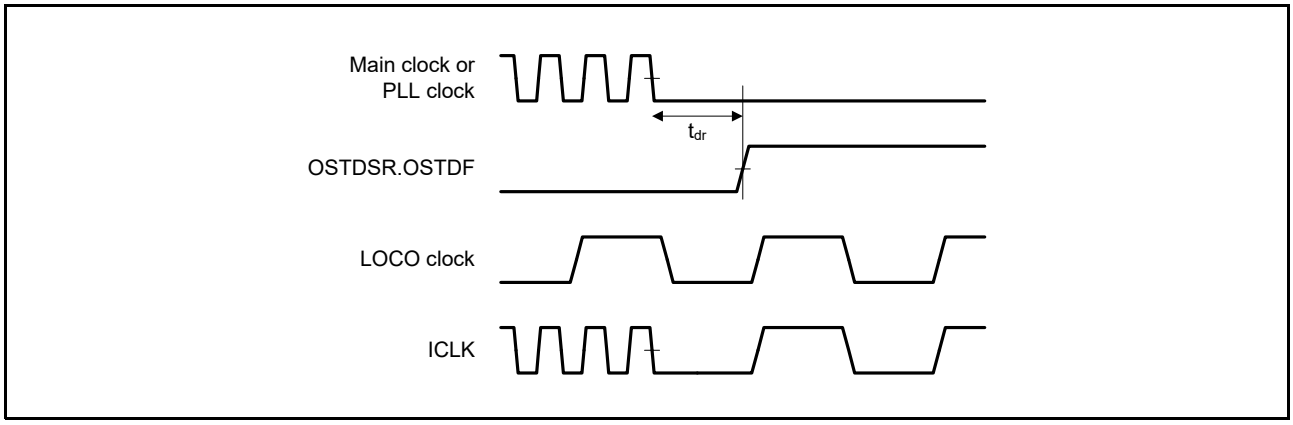


Figure 5.80 Oscillation Stop Detection Timing

Table 5.55 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.18	1.9	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.9	11	—	1.7	10	ms
	128 bytes	t_{DP128}	—	4.7	27	—	2.9	16	—	2.6	15	ms
	256 bytes	t_{DP256}	—	8.9	50	—	5.4	31	—	4.9	28	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	33	—	—	30	µs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	100000 *2	—	—	Times
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	132	—	—	120	µs
First suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	216	—	—	132	—	—	120	µs
	128 bytes	—	—	—	216	—	—	132	—	—	120	µs
	256 bytes	—	—	—	216	—	—	132	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Suspend delay time during erasing (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

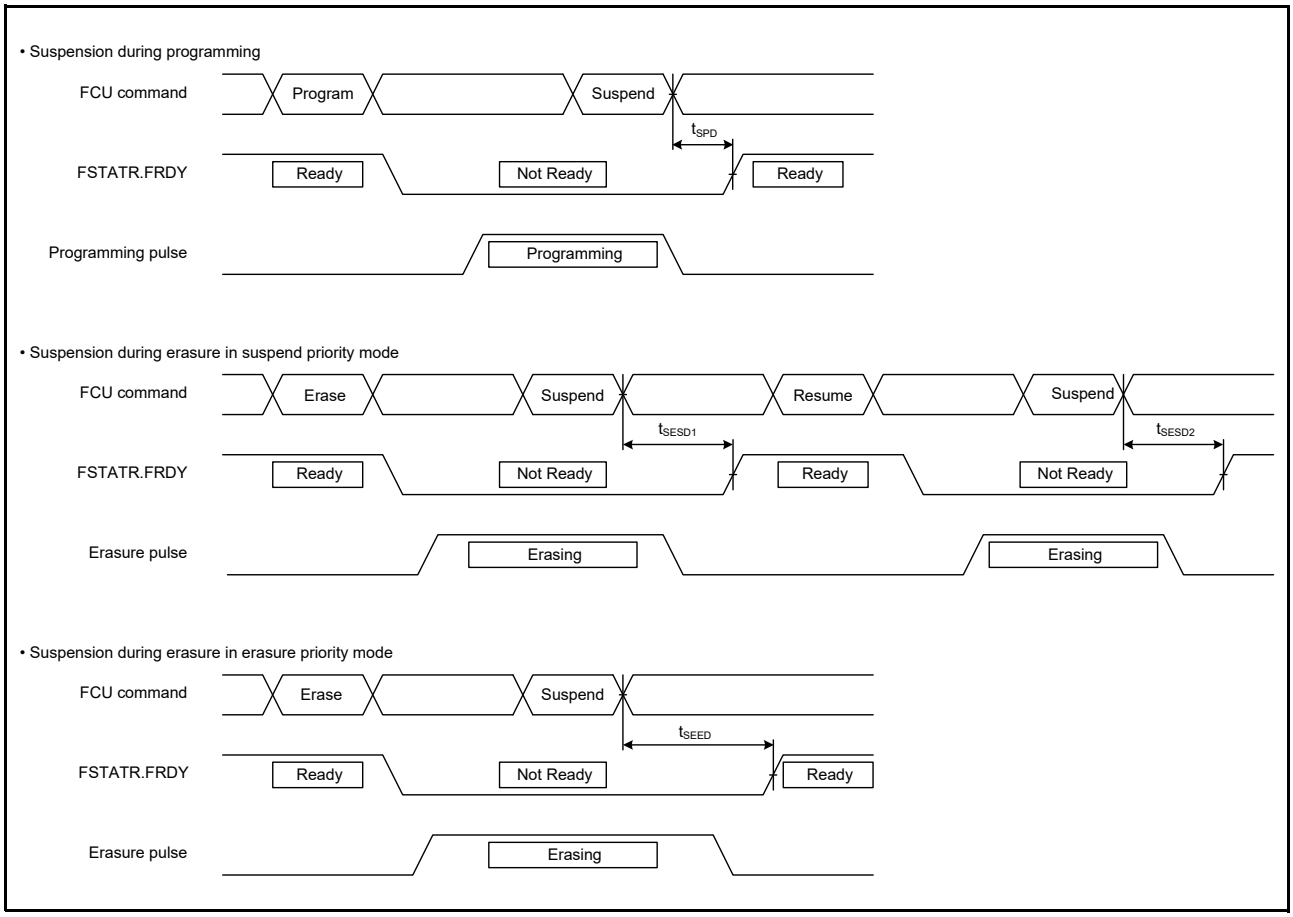


Figure 5.82 Flash Memory Programming/Erasure Suspension Timing

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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