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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5651cddfb-30

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.

Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, see Table 1.2, Code Flash Memory Capacity and Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 120 MHz 32-bit RX CPU (RXv2) - Minimum instruction execution time: One instruction per state (cycle of the system clock) - Address space: 4-Gbyte linear - Register set of the CPU - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers - Basic instructions: 75 - Floating-point instructions: 11 - DSP instructions: 23 - Addressing modes: 11 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: $32 \times 32 \rightarrow 64$ bits - On-chip divider: $32 / 32 \rightarrow 32$ bits - Barrel shifter: 32 bits
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	- Capacity: 512 Kbytes/768 Kbytes/1 Mbyte/1.5 Mbytes/2 Mbytes $50 \text{ MHz} \leq$ No-wait cycle access $100 \text{ MHz} \leq$ 1-wait cycle access $100 \text{ MHz} \geq$ 2-wait cycle access - Instructions hitting the ROM cache or operand = 120 MHz: No-wait access - On-board programming: Four types - Off-board programming (parallel programmer mode) - Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. - A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	- Capacity: 32 Kbytes - Programming/erasing: 100,000 times
	RAM	- Capacity: 256 Kbytes (Products with 1 Mbyte of code flash memory or less) - RAM: 256 Kbytes - Capacity: 640 Kbytes (Products with at least 1.5 Mbytes of code flash memory) - RAM: 256 Kbytes - Expansion RAM: 384 Kbytes 120 MHz, no-wait access
	Standby RAM	- Capacity: 8 Kbytes - Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565NEDDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NEDDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85

Table 1.3 List of Products (2/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N7ADFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NEDDLK	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLK	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDLK	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLK	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NEDDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R		
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15	
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14	
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13	
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12	
11	PD6	PG1	VCC	P61	RX65N Group, RX651 Group PTLG0177KA-A (177-Pin TFLGA) (Upper Perspective View)							P81	P82	PC6	VCC	11	
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10	
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9	
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8	
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7	
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_ USB	USB0_ DP	6	
5	P46	P47	P45	P44	NC								PJ2	P12	VCC_ USB	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4	
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3	
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2	
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R		

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

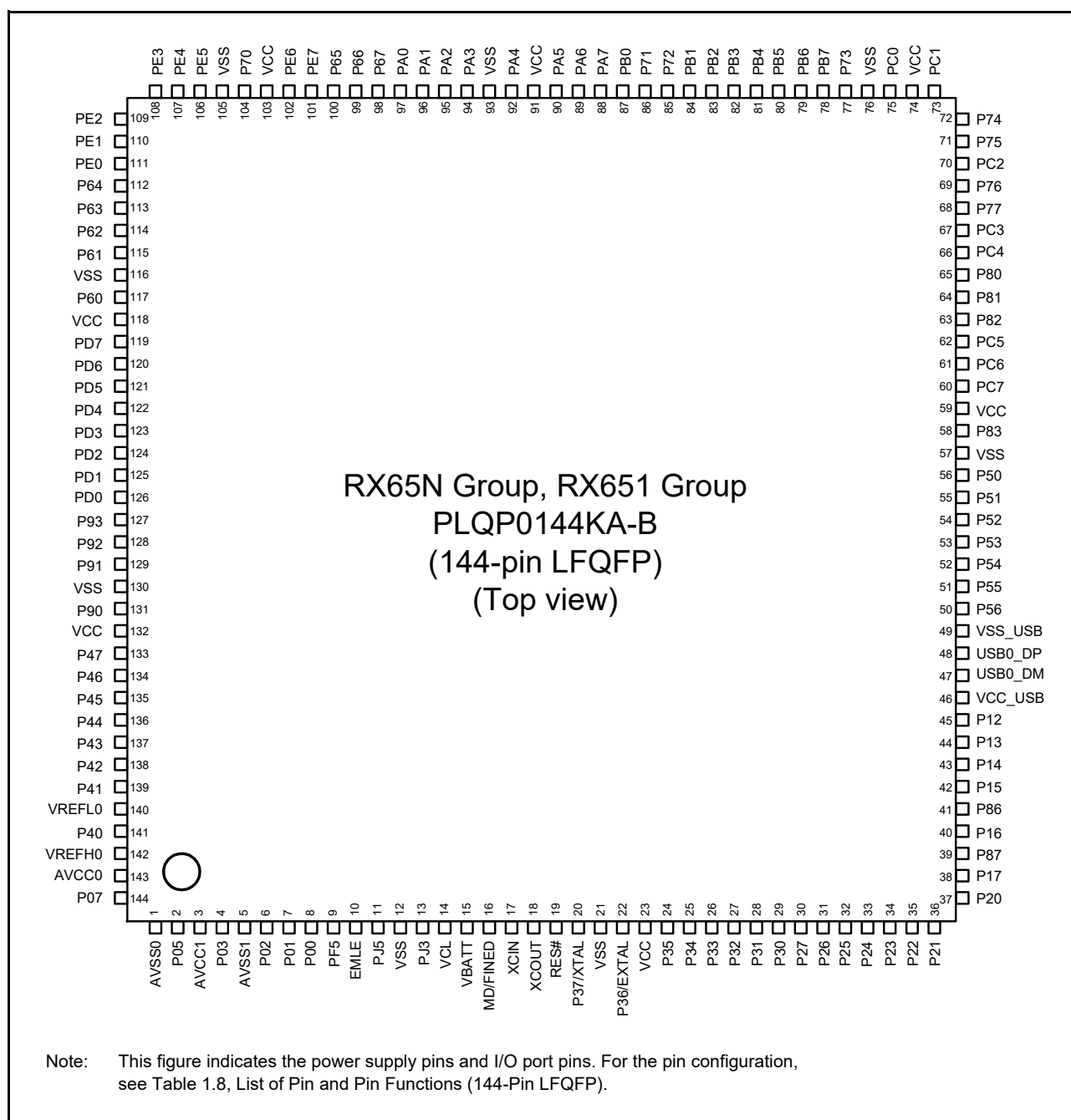
**Figure 1.7 Pin Assignment (144-Pin LQFP)**

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
L4		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0 #
L12		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
L13		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6	SDSI_D3-B	LCD_TC ON1-B		
L14		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCIO/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		LCD_TC ON3-B	IRQ4-DS	
L15		P72	A19/CS2#		ET0_MDC		LCD_DA TA23-A		
M1		P27	CS7#	MTIOC2B/ TMCIO/PO7	SCK1/RSPCKB- A				
M2		P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
M3		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
M4		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
M5		PJ2			TXD8/SMOSI8/ SSDA8/SSLC3-B		LCD_TC ON2-A		
M6		PJ1		MTIOC6A	RXD8/SMISO8/ SSCL8/SSLC2-B		LCD_TC ON3-A		
M7		P85		MTIOC6C/ TIOCC0			LCD_DA TA1-A		
M8		P55	D0[A0/D0]/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC- B/CRX1		LCD_DA TA5-A	IRQ10	
M9		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
M10		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A	MMC_D5-A	LCD_DA TA11-A		
M11		P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A	LCD_DA TA13-A		
M12		P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A	LCD_DA TA17-A		
M13		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (8/8)

Pin Number				Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC						
160		P92	D18/A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
161		P91	D17/A17		SCK7				AN115
162	VSS								
163		P90	D16/A16		TXD7/SMOSI7/ SSDA7				AN114
164	VCC								
165		P47						IRQ15- DS	AN007
166		P46						IRQ14- DS	AN006
167		P45						IRQ13- DS	AN005
168		P44						IRQ12- DS	AN004
169		P43						IRQ11- DS	AN003
170		P42						IRQ10- DS	AN002
171		P41						IRQ9-DS	AN001
172	VREFL0								
173		P40						IRQ8-DS	AN000
174	VREFH0								
175	AVCC0								
176		P07						IRQ15	ADTRG0 #

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

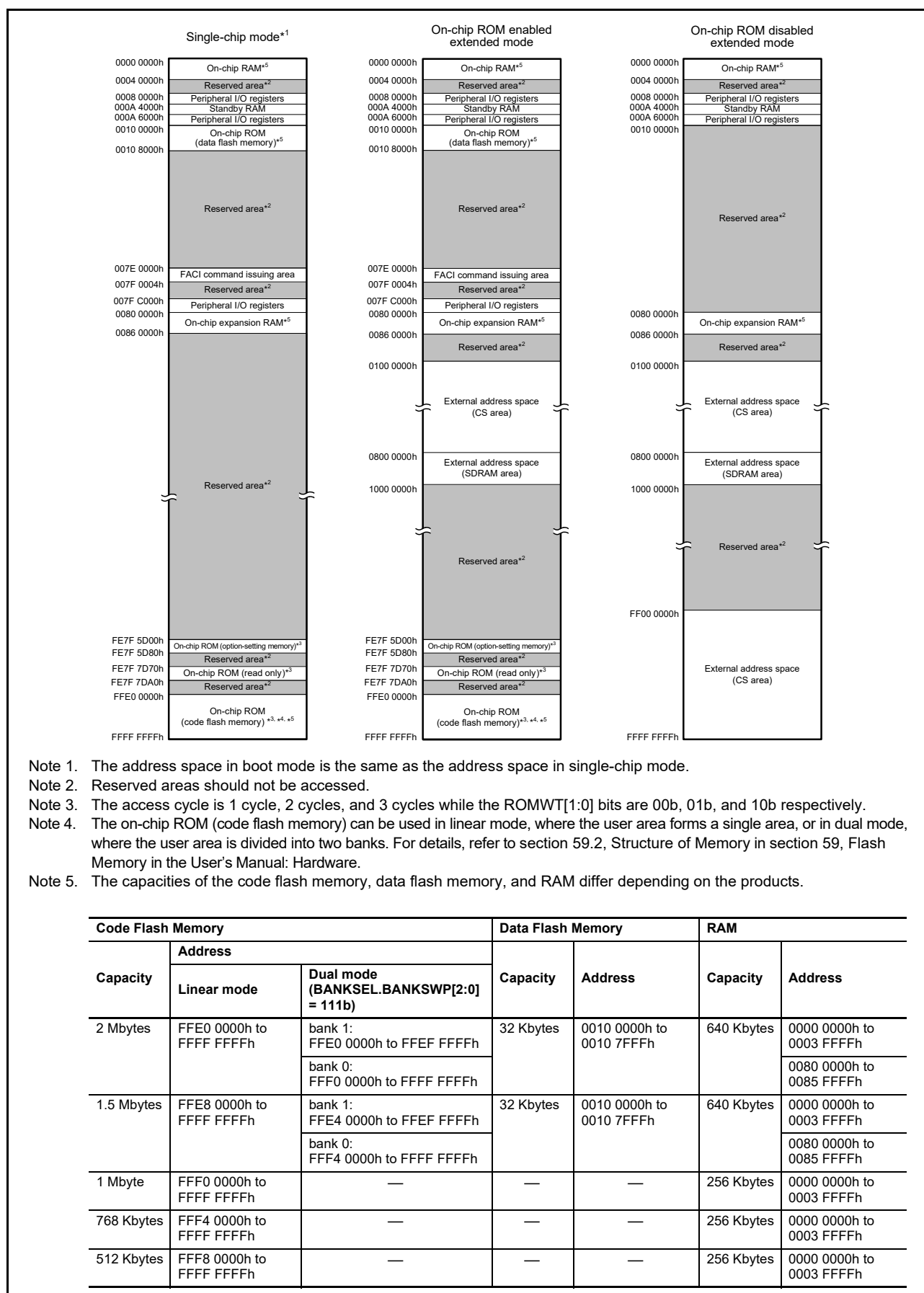


Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (10 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 779Dh	ICU	Software Configurable Interrupt B Source Select Register 157	SLIBR157	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Eh	ICU	Software Configurable Interrupt B Source Select Register 158	SLIBR158	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Fh	ICU	Software Configurable Interrupt B Source Select Register 159	SLIBR159	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A0h	ICU	Software Configurable Interrupt B Source Select Register 160	SLIBR160	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A1h	ICU	Software Configurable Interrupt B Source Select Register 161	SLIBR161	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A2h	ICU	Software Configurable Interrupt B Source Select Register 162	SLIBR162	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A3h	ICU	Software Configurable Interrupt B Source Select Register 163	SLIBR163	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A4h	ICU	Software Configurable Interrupt B Source Select Register 164	SLIBR164	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A5h	ICU	Software Configurable Interrupt B Source Select Register 165	SLIBR165	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A6h	ICU	Software Configurable Interrupt B Source Select Register 166	SLIBR166	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A7h	ICU	Software Configurable Interrupt B Source Select Register 167	SLIBR167	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A8h	ICU	Software Configurable Interrupt B Source Select Register 168	SLIBR168	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A9h	ICU	Software Configurable Interrupt B Source Select Register 169	SLIBR169	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AAh	ICU	Software Configurable Interrupt B Source Select Register 170	SLIBR170	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ABh	ICU	Software Configurable Interrupt B Source Select Register 171	SLIBR171	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ACh	ICU	Software Configurable Interrupt B Source Select Register 172	SLIBR172	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ADh	ICU	Software Configurable Interrupt B Source Select Register 173	SLIBR173	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AEh	ICU	Software Configurable Interrupt B Source Select Register 174	SLIBR174	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AFh	ICU	Software Configurable Interrupt B Source Select Register 175	SLIBR175	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B0h	ICU	Software Configurable Interrupt B Source Select Register 176	SLIBR176	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B1h	ICU	Software Configurable Interrupt B Source Select Register 177	SLIBR177	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B2h	ICU	Software Configurable Interrupt B Source Select Register 178	SLIBR178	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B3h	ICU	Software Configurable Interrupt B Source Select Register 179	SLIBR179	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B4h	ICU	Software Configurable Interrupt B Source Select Register 180	SLIBR180	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B5h	ICU	Software Configurable Interrupt B Source Select Register 181	SLIBR181	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B6h	ICU	Software Configurable Interrupt B Source Select Register 182	SLIBR182	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B7h	ICU	Software Configurable Interrupt B Source Select Register 183	SLIBR183	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B8h	ICU	Software Configurable Interrupt B Source Select Register 184	SLIBR184	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B9h	ICU	Software Configurable Interrupt B Source Select Register 185	SLIBR185	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BAh	ICU	Software Configurable Interrupt B Source Select Register 186	SLIBR186	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BBh	ICU	Software Configurable Interrupt B Source Select Register 187	SLIBR187	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (19 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9084h	S12AD	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 908Ch	S12AD	A/D Comparison Function Window A/B Status Monitoring Register	ADWINMON	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9090h	S12AD	A/D Comparison Function Control Register	ADCMPCR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9094h	S12AD	A/D Comparison Function Window A Channel Select Register 0	ADCMPSNR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9098h	S12AD	A/D Comparison Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 909Ch	S12AD	A/D Comparison Function Window A Lower Level Setting Register	ADCMPDR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 909Eh	S12AD	A/D Comparison Function Window A Upper Level Setting Register	ADCMPDR1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90A0h	S12AD	A/D Comparison Function Window A Channel Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90A6h	S12AD	A/D Comparison Function Window B Channel Select Register	ADCMPBNSR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90A8h	S12AD	A/D Comparison Function Window B Lower Level Setting Register	ADWINLLB	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90AAh	S12AD	A/D Comparison Function Window B Upper Level Setting Register	ADWINULB	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90ACh	S12AD	A/D Comparison Function Window B Channel Status Register	ADCMPBSR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90D4h	S12AD	A/D Channel Select Register C0	ADANSC0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90D9h	S12AD	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9100h	S12AD1	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9104h	S12AD1	A/D Channel Select Register A0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9106h	S12AD1	A/D Channel Select Register A1	ADANSA1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9108h	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 910Ah	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 910Ch	S12AD1	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 910Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa

Table 4.1 List of I/O Registers (Address Order) (23 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A006h	SMCI0	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A009h	SCI0	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A00Ah	SCI0	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A00Bh	SCI0	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A00Ch	SCI0	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i

Table 4.1 List of I/O Registers (Address Order) (35 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C010h	PORTG	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C026h	PORT6	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Fh	PORTF	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C030h	PORTG	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C040h	PORT0	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C041h	PORT1	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C042h	PORT2	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C043h	PORT3	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C044h	PORT4	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C045h	PORT5	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C046h	PORT6	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C047h	PORT7	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C048h	PORT8	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C049h	PORT9	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C04Ah	PORTA	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports

Table 4.1 List of I/O Registers (Address Order) (60 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 13D0h	GLCDC	Contrast Adjustment Register	CONTRAST	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13D4h	GLCDC	Panel Dither Control Register	PANELDTHA	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13E4h	GLCDC	Output Phase Control Register	CLKPHASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1404h	GLCDC	Reference Timing Setting Register	TCONTIM	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1408h	GLCDC	Vertical Timing Setting Register A1	TCONSTVA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 140Ch	GLCDC	Vertical Timing Setting Register A2	TCONSTVA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1410h	GLCDC	Vertical Timing Setting Register B1	TCONSTVB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1414h	GLCDC	Vertical Timing Setting Register B2	TCONSTVB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1418h	GLCDC	Horizontal Timing Setting Register A1	TCONSTHA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 141Ch	GLCDC	Horizontal Timing Setting Register A2	TCONSTHA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1420h	GLCDC	Horizontal Timing Setting Register B1	TCONSTHB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1424h	GLCDC	Horizontal Timing Setting Register B2	TCONSTHB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1428h	GLCDC	Data Enable Polarity Setting Register	TCONDE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1440h	GLCDC	Status Detection Control Register	DTCTEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1444h	GLCDC	Interrupt Request Enable Control Register	INTEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1448h	GLCDC	Detected Status Clear Register	STCLR	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 144Ch	GLCDC	Detected Status Monitor Register	STMON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1450h	GLCDC	Panel Clock Control Register	PANELCLK	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 3000h	DRW2D	Geometry Control Register	CONTROL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3000h	DRW2D	Status Register	STATUS	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3004h	DRW2D	Surface Control Register	CONTROL2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3004h	DRW2D	Hardware Version Register	HWVER	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3010h	DRW2D	Limiter 1 Start Value Register	L1START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3014h	DRW2D	Limiter 2 Start Value Register	L2START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3018h	DRW2D	Limiter 3 Start Value Register	L3START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 301Ch	DRW2D	Limiter 4 Start Value Register	L4START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3020h	DRW2D	Limiter 5 Start Value Register	L5START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3024h	DRW2D	Limiter 6 Start Value Register	L6START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3028h	DRW2D	Limiter 1 X-Axis Increment Register	L1XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 302Ch	DRW2D	Limiter 2 X-Axis Increment Register	L2XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3030h	DRW2D	Limiter 3 X-Axis Increment Register	L3XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3034h	DRW2D	Limiter 4 X-Axis Increment Register	L4XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3038h	DRW2D	Limiter 5 X-Axis Increment Register	L5XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 303Ch	DRW2D	Limiter 6 X-Axis Increment Register	L6XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3040h	DRW2D	Limiter 1 Y-Axis Increment Register	L1YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3044h	DRW2D	Limiter 2 Y-Axis Increment Register	L2YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3048h	DRW2D	Limiter 3 Y-Axis Increment Register	L3YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 304Ch	DRW2D	Limiter 4 Y-Axis Increment Register	L4YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3050h	DRW2D	Limiter 5 Y-Axis Increment Register	L5YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3054h	DRW2D	Limiter 6 Y-Axis Increment Register	L6YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3058h	DRW2D	Limiter 1 Band Width Parameter Register	L1BAND	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 305Ch	DRW2D	Limiter 2 Band Width Parameter Register	L2BAND	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3064h	DRW2D	Base Color Register	COLOR1	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3068h	DRW2D	Secondary Color Register	COLOR2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3074h	DRW2D	Pattern Register	PATTERN	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3078h	DRW2D	Bounding Box Dimension Register	SIZE	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 307Ch	DRW2D	Frame Buffer Pitch Register	PITCH	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3080h	DRW2D	Frame Buffer Base Address Register	ORIGIN	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3090h	DRW2D	U Limiter Start Value Register	LUST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3094h	DRW2D	U Limiter X-Axis Increment Register	LUXADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D

Table 4.1 List of I/O Registers (Address Order) (61 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 3098h	DRW2D	U Limiter Y-Axis Increment Register	LUYADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 309Ch	DRW2D	V Limiter Start Value Integer Part Register	LVSTI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A0h	DRW2D	V Limiter Start Value Fractional Part Register	LVSTF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A4h	DRW2D	V Limiter X-Axis Increment Integer Part Register	LVXADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A8h	DRW2D	V Limiter Y-Axis Increment Integer Part Register	LVYADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30ACh	DRW2D	V Limiter Increment Fractional Parts Register	LVYXADDF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B4h	DRW2D	Texels Per Texture Line Register	TEXPITCH	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B8h	DRW2D	Texture Mask Register	TEXMSK	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30BCh	DRW2D	Texture Base Address Register	TEXORG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C0h	DRW2D	Interrupt Control Register	IRQCTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C4h	DRW2D	Cache Control Register	CACHECTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C8h	DRW2D	Display List Start Address Register	DLISTST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30CCh	DRW2D	Performance Counter 1	PERFCNT1	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D0h	DRW2D	Performance Counter 2	PERFCNT2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D4h	DRW2D	Performance Counters Control Register	PERFTRG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30DCh	DRW2D	CLUT Start Address Register	TEXCLADDR	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E0h	DRW2D	CLUT Data Register	TEXCLDATA	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E4h	DRW2D	CLUT Offset Register	TEXCLOFST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E8h	DRW2D	Chroma Key Register	COLKEY	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
007F C040h	FLASH	Data Flash Memory Access Frequency Setting Register	EEPFCLK	8	8	2 FCLK		Flash
FE7F 7D7Ch	TEMPS	Temperature Sensor Calibration Data Register	TSCDR	32	32	1 to 3 ICLK		TEMPS
FE7F 7D90h	FLASH	Unique ID Register 0	UIDR0	32	32	1 to 3 ICLK		Flash
FE7F 7D94h	FLASH	Unique ID Register 1	UIDR1	32	32	1 to 3 ICLK		Flash
FE7F 7D98h	FLASH	Unique ID Register 2	UIDR2	32	32	1 to 3 ICLK		Flash
FE7F 7D9Ch	FLASH	Unique ID Register 3	UIDR3	32	32	1 to 3 ICLK		Flash

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 0008 81ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 0008 81EEh and 0008 81ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 0008 81EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 0008 81EFh and 0008 81EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 0008 81FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 0008 81FEh and 0008 81FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 0008 81FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 0008 81FFh and 0008 81FDh, respectively.

Note 5. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 6. The address must end with 0h, 4h, 8h, or Ch when access is made in 32-bit units. The address must end with 0h, 2h, 4h, 6h, 8h, Ah, Ch, or Eh when access is made in 16-bit units.

Note 7. When the register is accessed while the GLCDC is operating, a delay may be generated in accessing.

Table 5.12 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	32	—	264	kHz
	Peripheral module clock (PCLKA)			—	—	264	
	Peripheral module clock (PCLKB)			—	—	264	
	Peripheral module clock (PCLKC)* ¹			—	—	264	
	Peripheral module clock (PCLKD)* ¹			—	—	264	
	Flash-IF clock (FCLK)			32	—	264	
	External bus clock (BCLK)	Other than 100-pin package		—	—	264	
		100-pin package		—	—	264	
	BCLK pin output	Other than 100-pin package		—	—	264	
		100-pin package		—	—	264	
	SDRAM clock (SDCLK)	Other than 100-pin package		—	—	264	
	SDCLK pin output	Other than 100-pin package		—	—	264	

Note 1. The 12-bit A/D converter cannot be used.

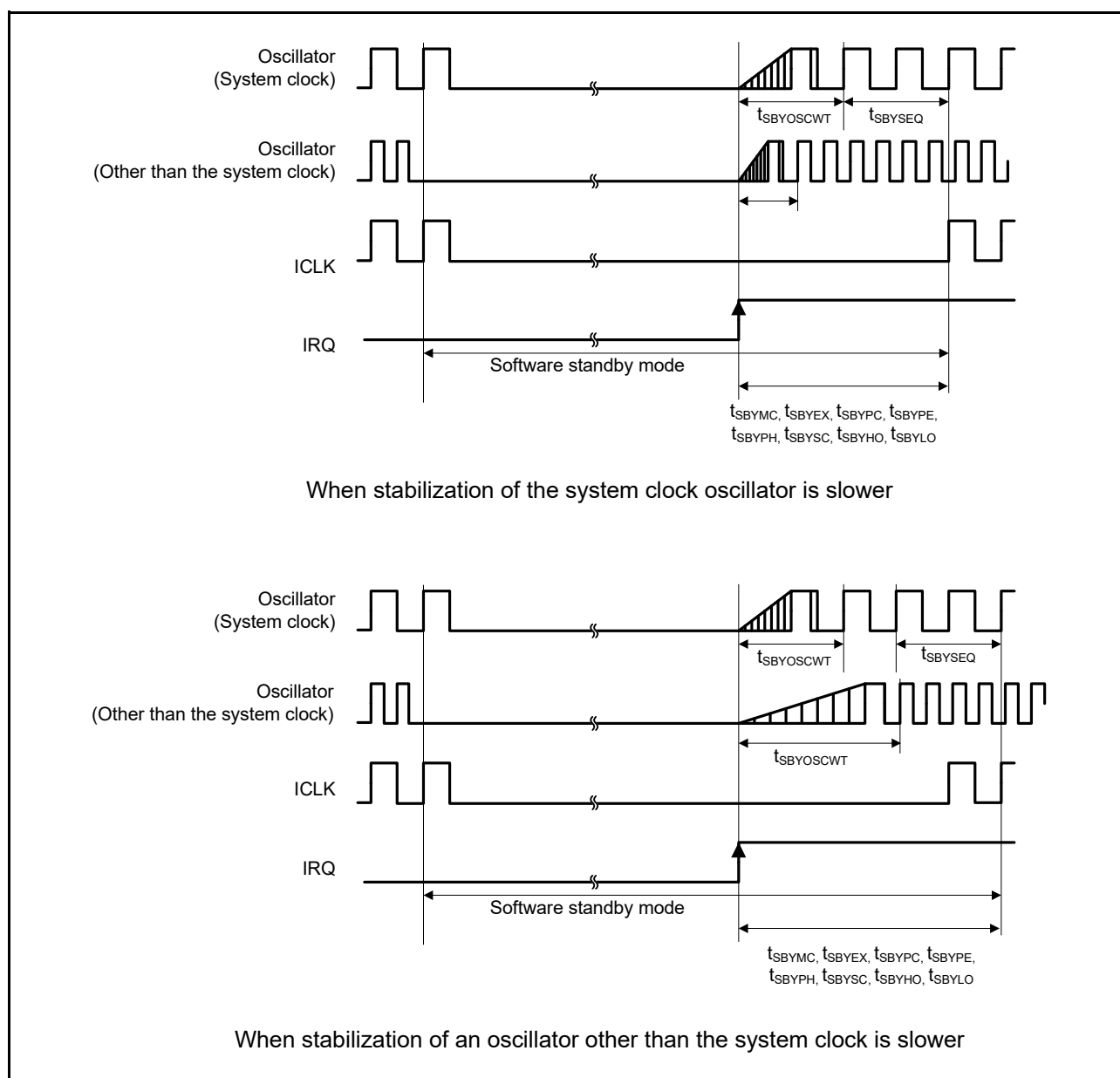


Figure 5.12 Software Standby Mode Cancellation Timing

5.3.5 Bus Timing

Table 5.24 Bus Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $ICLK = PCLKA = 8$ to 120 MHz, $PCLKB = BCLK = SDCLK = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

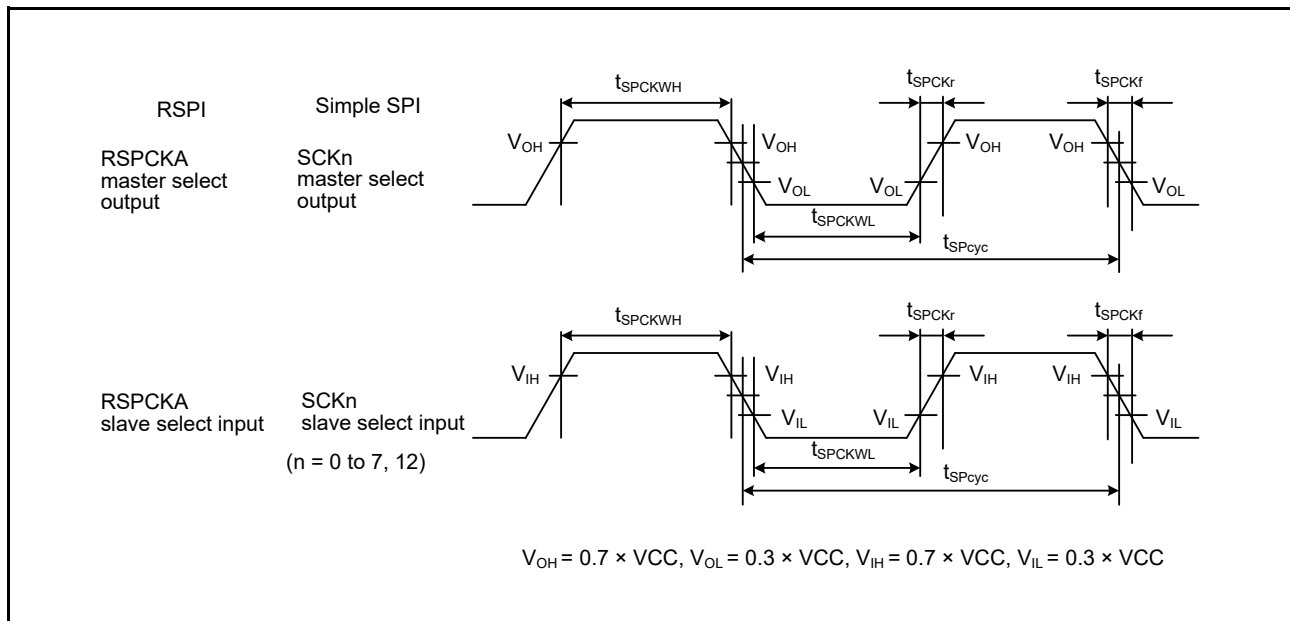
Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	12.5	ns	Figure 5.16 to Figure 5.21
Byte control delay time	t_{BCD}	—	12.5	ns	
CS# delay time	t_{CSD}	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	ns	
RD# delay time	t_{RSD}	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	12.5	ns	
Write data delay time	t_{WDD}	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	12.5	—	ns	Figure 5.22
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	12.5	ns	Figure 5.23
CS# delay time 2 (SDRAM)	t_{CSD2}	1	12.5	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	12.5	ns	
CKE delay time (SDRAM)	t_{CKED}	1	12.5	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	10	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	12.5	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	12.5	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	12.5	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	12.5	ns	

Table 5.36 Simple SPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPCyc}	4	65536	t_{PACyc}	Figure 5.44
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPCyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPCyc}	
	SCK clock rise/fall time	t_{SPCKr} , t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 5.45 to Figure 5.50
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPCyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPCyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	−10	—	ns	
	Data rise/fall time	t_{Dr} , t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr} , t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{PBCyc}	Figure 5.49, Figure 5.50
	Slave output release time	t_{REL}	—	5	t_{PBCyc}	

Note 1. t_{PACyc} : PCLKA cycle, t_{PBCyc} : PCLKB cycle

**Figure 5.44 RSPI Clock Timing and Simple SPI Clock Timing**

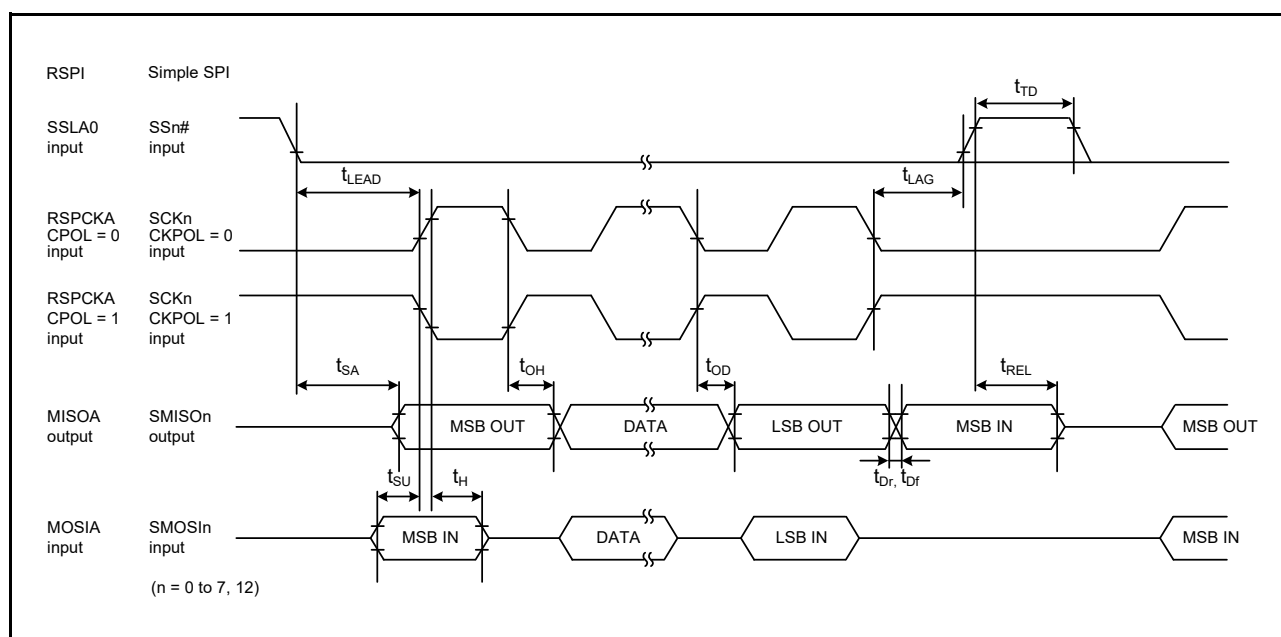


Figure 5.49 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

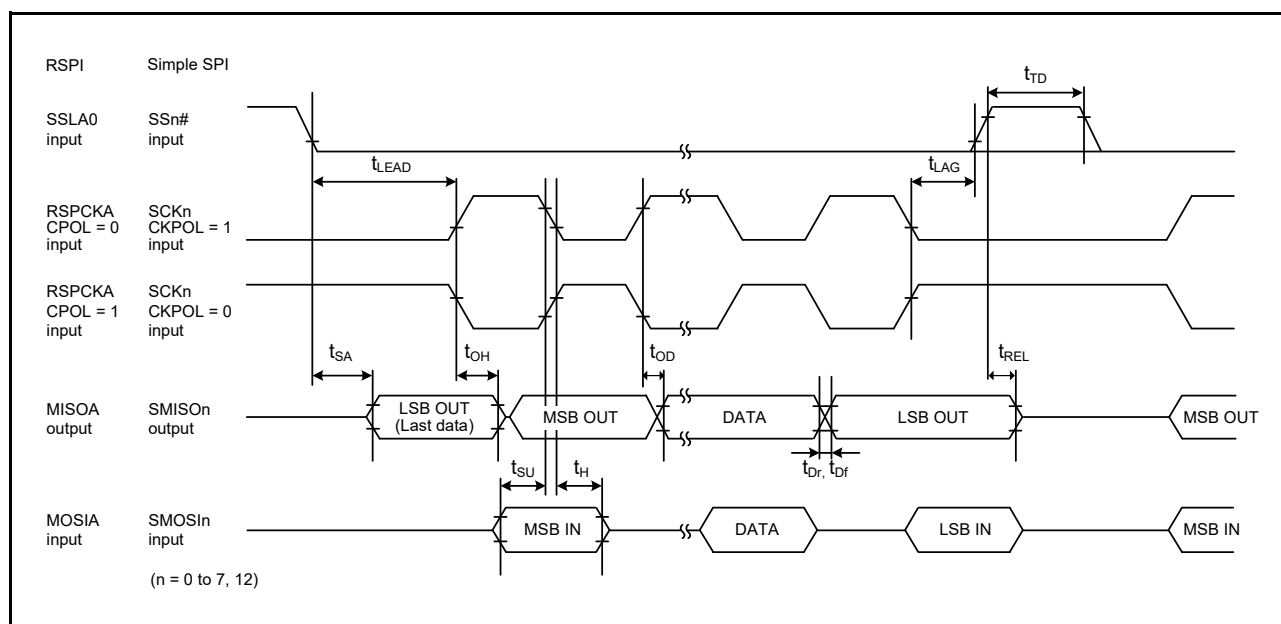
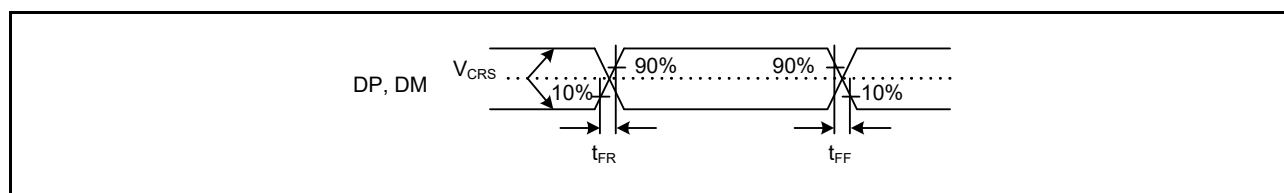
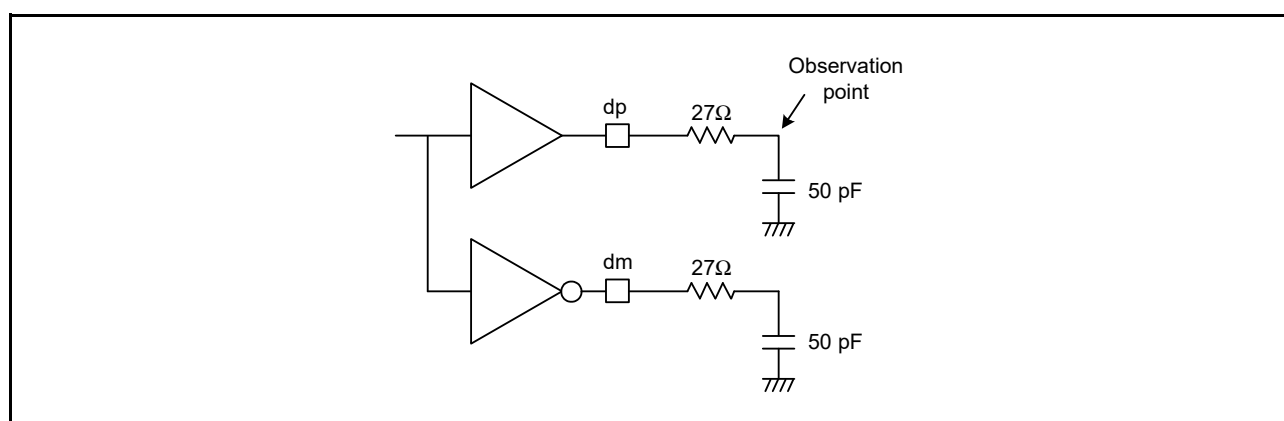


Figure 5.50 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

Table 5.45 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $3.0 \leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $U_{CLK} = 48$ MHz,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V
	Input low level voltage	V_{IL}	—	—	0.8	V
	Differential input sensitivity	V_{DI}	0.2	—	—	V
	Differential common mode range	V_{CM}	0.8	—	2.5	V
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V
	Output low level voltage	V_{OL}	0.0	—	0.3	V
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V
	Rise time	t_{FR}	4	—	20	ns
	Fall time	t_{FF}	4	—	20	ns
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	%
	Output resistance	Z_{DRV}	28	—	44	Ω
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	k Ω
			1.425	—	3.090	k Ω
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	k Ω

**Figure 5.74 DP and DM Output Timing (Full-Speed)****Figure 5.75 Test Circuit (Full-Speed)**