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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5651cddfp-30

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Safety	Clock frequency accuracy measurement circuit (CAC)	Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDG-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Encryption function	AESa*2	- Key lengths: 128, 192, and 256 bits - Support for CFB, OFB, and CMAC operating modes - Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles - Compliant with FIPS PUB 197
	True random number generator (RNG)*2	- Length of random numbers: 16 bits - Generation of random-number-generated interrupts after a number is generated - Random number generation time: 1.9 ms (typ)
	Trusted Secure IP (TSIP)*2	- Security algorithm - Common key encryption: AES (compliant with NIST FIPS PUB 197), 3DES, ARC4 - Non-common key encryption: RSA - Other features - TRNG (true-random number generator) - Hash value generation: SHA1, SHA224, SHA256, GHASH - Support of unique ID
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$, V _{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: -40 to +85°C G-version: -40 to +105°C
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-B) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-B)
On-chip debugging system		- E1 emulator (JTAG and FINE interfaces) - E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. The product part number differs according to whether or not the MCU includes the encryption function.

Note 3. The product part number differs according to whether or not the MCU includes an SDHI (SD host interface)/SDSI (SD slave interface) (products with 1 Mbyte of code flash memory or less).

Note 4. When the realtime clock is not used, initialize the registers in the time clock according to description in section 31.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.

Table 1.3 List of Products (3/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N4EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
RX65N (G version)	R5F565NEDGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NEDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565N9AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N9BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N9EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N9FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (6/8)

Pin Number				Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC						
109		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DA TA4-B	IRQ5-DS	
110		PA3	A3	MTIOC0D/ MTCLKD/ TIOC0D/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DA TA5-B	IRQ6-DS	
111	TRDATA3	PG7	D31						
112		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DA TA6-B		
113	TRDATA2	PG6	D30						
114		PA1	DQM3/A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DA TA7-B	IRQ11	
115	VCC								
116	TRCLK	PG5	D29						
117	VSS								
118		PA0	DQM2/ BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DA TA8-B		
119	TRSYNC	PG4	D28						
120		P67	DQM1/CS7#	MTIOC7C				IRQ15	
121	TRDATA1	PG3	D27						
122		P66	DQM0/CS6#	MTIOC7D					
123	TRDATA0	PG2	D26						
124		P65	CKE/CS5#						
125		PE7	D15[A15/ D15]/D7[A7/ D7]	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DA TA9-B	IRQ7	AN105
126		PE6	D14[A14/ D14]/D6[A6/ D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DA TA10-B	IRQ6	AN104
127	VCC								
128		P70	SDCLK						
129	VSS								
130		PE5	D13[A13/ D13]/D5[A5/ D5]	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DA TA11-B	IRQ5	AN103
131		PE4	D12[A12/ D12]/D4[A4/ D4]	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DA TA12-B		AN102
132		PE3	D11[A11/ D11]/D3[A3/ D3]	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#SS12#	MMC_D7-B	LCD_DA TA13-B		AN101
133		PE2	D10[A10/ D10]/D2[A2/ D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3- B	MMC_D6-B	LCD_DA TA14-B	IRQ7-DS	AN100

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface			
145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCI, RSPI, RIIC, CAN, USB)	(QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
L11		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A			
L12	TRDATA4	P73	CS3#	PO16	ET0_WOL				
L13	VSS								
M1		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C*1/ PIXD6			
M2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C*1/ PIXD3		IRQ7	ADTRG1 #
M3		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
M4		P12		TMC11	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
M5	VCC_USB								
M6	VSS_USB								
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
M8		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMC12/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A		IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A			
M10	TRDATA7	P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A			
M11		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
M12		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
M13	VCC								
N1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN	SDHI_CLK-C*1/ PIXD5		IRQ9	
N2		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID	SDHI_CMD-C*1/ PIXD4		IRQ8	
N3		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C*1/ PIXD2			
N4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
N5					USB0_DM				
N6					USB0_DP				

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (2/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
30	TCK	P27	CS7#	MTIOC2B/ TMC13/PO7	SCK1/RSPCKB- A				
31	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
32		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD*1/ HSYNC			ADTRG0 #
33		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP*1/ PIXCLK			
34		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C*1/ PIXD7			
35		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C*1/ PIXD6			
36		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN	SDHI_CLK-C*1/ PIXD5		IRQ9	
37		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID	SDHI_CMD-C*1/ PIXD4		IRQ8	
38		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C*1/ PIXD3		IRQ7	ADTRG1 #
39		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C*1/ PIXD2			
40		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOU	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
41		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
42		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMC12/ PO13	RXD1/SMOSI1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	
43		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
44		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1 #
45		P12		TMC1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
46	VCC_USB								
47					USB0_DM				
48					USB0_DP				

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (2/5)

Pin Number				Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC						
26		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B				
27		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN			IRQ9	
28		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID			IRQ8	
29		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS			IRQ7	ADTRG1 #
30		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOU	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
31		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS			IRQ5	
32		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
33		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1 #
34		P12		TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
35	VCC_USB								
36					USB0_DM				
37					USB0_DP				
38	VSS_USB								
39		P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ CRX1			IRQ10	
40		P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
41		P53*2	BCLK						
42		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
43		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (7 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 3852h	BSC	CS5 Control Register	CS5CR	16	16	1, 2 BCLK		Buses
0008 385Ah	BSC	CS5 Recovery Cycle Register	CS5REC	16	16	1, 2 BCLK		Buses
0008 3862h	BSC	CS6 Control Register	CS6CR	16	16	1, 2 BCLK		Buses
0008 386Ah	BSC	CS6 Recovery Cycle Register	CS6REC	16	16	1, 2 BCLK		Buses
0008 3872h	BSC	CS7 Control Register	CS7CR	16	16	1, 2 BCLK		Buses
0008 387Ah	BSC	CS7 Recovery Cycle Register	CS7REC	16	16	1, 2 BCLK		Buses
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK		Buses
0008 3C00h	BSC	SDC Control Register	SDCCR	8	8	1, 2 BCLK		Buses
0008 3C01h	BSC	SDC Mode Register	SDCMOD	8	8	1, 2 BCLK		Buses
0008 3C02h	BSC	SDRAM Access Mode Register	SDAMOD	8	8	1, 2 BCLK		Buses
0008 3C10h	BSC	SDRAM Self-Refresh Control Register	SDSELF	8	8	1, 2 BCLK		Buses
0008 3C14h	BSC	SDRAM Refresh Control Register	SDRFCR	16	16	1, 2 BCLK		Buses
0008 3C16h	BSC	SDRAM Auto-Refresh Control Register	SDRFEN	8	8	1, 2 BCLK		Buses
0008 3C20h	BSC	SDRAM Initialization Sequence Control Register	SDICR	8	8	1, 2 BCLK		Buses
0008 3C24h	BSC	SDRAM Initialization Register	SDIR	16	16	1, 2 BCLK		Buses
0008 3C40h	BSC	SDRAM Address Register	SDADR	8	8	1, 2 BCLK		Buses
0008 3C44h	BSC	SDRAM Timing Register	SDTR	32	32	1, 2 BCLK		Buses
0008 3C48h	BSC	SDRAM Mode Register	SDMOD	16	16	1, 2 BCLK		Buses
0008 3C50h	BSC	SDRAM Status Register	SDSR	8	8	1, 2 BCLK		Buses
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK		MPU
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK		MPU
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK		MPU
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK		MPU
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK		MPU
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK		MPU
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK		MPU
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK		MPU
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK		MPU
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK		MPU
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK		MPU
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK		MPU
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK		MPU
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK		MPU
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK		MPU
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK		MPU
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK		MPU
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK		MPU
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK		MPU
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK		MPU
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK		MPU
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK		MPU
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK		MPU
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK		MPU
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK		MPU
0008 7010h to 0008 70FFh	ICU	Interrupt Request Registers 016 to 255	IR016 to 255	8	8	2 ICLK		ICUB
0008 711Ah to 0008 71FFh	ICU	DTC Transfer Request Enable Registers 026 to 255	DTCER026 to DTCER255	8	8	2 ICLK		ICUB
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Registers 02 to 1F	IER02 to IER1F	8	8	2 ICLK		ICUB

Table 4.1 List of I/O Registers (Address Order) (8 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK		ICUB
0008 72E1h	ICU	Software Interrupt 2 Generation Register	SWINT2R	8	8	2 ICLK		ICUB
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK		ICUB
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Registers 000 to 255	IPR000 to IPR255	8	8	2 ICLK		ICUB
0008 7400h	ICU	DMAC Trigger Select Register 0	DMRSR0	8	8	2 ICLK		ICUB
0008 7404h	ICU	DMAC Trigger Select Register 1	DMRSR1	8	8	2 ICLK		ICUB
0008 7408h	ICU	DMAC Trigger Select Register 2	DMRSR2	8	8	2 ICLK		ICUB
0008 740Ch	ICU	DMAC Trigger Select Register 3	DMRSR3	8	8	2 ICLK		ICUB
0008 7410h	ICU	DMAC Trigger Select Register 4	DMRSR4	8	8	2 ICLK		ICUB
0008 7414h	ICU	DMAC Trigger Select Register 5	DMRSR5	8	8	2 ICLK		ICUB
0008 7418h	ICU	DMAC Trigger Select Register 6	DMRSR6	8	8	2 ICLK		ICUB
0008 741Ch	ICU	DMAC Trigger Select Register 7	DMRSR7	8	8	2 ICLK		ICUB
0008 7500h to 0008 750Fh	ICU	IRQ Control Registers 0 to 15	IRQCR0 to 15	8	8	2 ICLK		ICUB
0008 7520h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUB
0008 7521h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK		ICUB
0008 7528h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK		ICUB
0008 752Ah	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK		ICUB
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK		ICUB
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK		ICUB
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK		ICUB
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK		ICUB
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK		ICUB
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK		ICUB
0008 7600h	ICU	Group BE0 Interrupt Request Register	GRPBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7630h	ICU	Group BL0 Interrupt Request Register	GRPBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7634h	ICU	Group BL1 Interrupt Request Register	GRPBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7638h	ICU	Group BL2 Interrupt Request Register	GRPBL2	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7640h	ICU	Group BE0 Interrupt Request Enable Register	GENBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7670h	ICU	Group BL0 Interrupt Request Enable Register	GENBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7674h	ICU	Group BL1 Interrupt Request Enable Register	GENBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7678h	ICU	Group BL2 Interrupt Request Enable Register	GENBL2	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7680h	ICU	Group BE0 Interrupt Clear Register	GCRBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7700h	ICU	Software Configurable Interrupt B Request Register 0	PIBR0	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7701h	ICU	Software Configurable Interrupt B Request Register 1	PIBR1	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7702h	ICU	Software Configurable Interrupt B Request Register 2	PIBR2	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7703h	ICU	Software Configurable Interrupt B Request Register 3	PIBR3	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7704h	ICU	Software Configurable Interrupt B Request Register 4	PIBR4	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7705h	ICU	Software Configurable Interrupt B Request Register 5	PIBR5	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7706h	ICU	Software Configurable Interrupt B Request Register 6	PIBR6	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7707h	ICU	Software Configurable Interrupt B Request Register 7	PIBR7	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7708h	ICU	Software Configurable Interrupt B Request Register 8	PIBR8	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (18 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8528h	MMCIF	Response Register 1	CERESP1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 852Ch	MMCIF	Response Register 0	CERESP0	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8530h	MMCIF	Automatically Issued CMD12 Response Register	CERESPCM D12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8534h	MMCIF	Data Register	CEDATA	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 853Ch	MMCIF	Boot Operation Setting Register	CEBOOT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8540h	MMCIF	Interrupt status Flag Register	CEINT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8544h	MMCIF	Interrupt request Enable Register	CEINTEN	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8548h	MMCIF	Status Register 1	CEHOSTSTS 1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 854Ch	MMCIF	Status Register 2	CEHOSTSTS 2	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8570h	MMCIF	MMC Detection and Port Control Register	CEDETECT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8574h	MMCIF	Special Mode Setting Register	CEADDMODE	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 857Ch	MMCIF	Version Register	CEVERSION	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9063h	S12AD	A/D Conversion Time Setting Protection Release Register	ADSAMPR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9066h	S12AD	A/D Sample-and-Hold Circuit Control Register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 906Eh	S12AD	A/D Conversion Time Setting Register	ADSAM	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 907Ch	S12AD	A/D Sample-and-Hold Operating Mode Select Register	ADSHMSR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa

Table 4.1 List of I/O Registers (Address Order) (50 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0078h	EDMAC 0	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 007Ch	EDMAC 0	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00C8h	EDMAC 0	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00CCh	EDMAC 0	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00D4h	EDMAC 0	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00D8h	EDMAC 0	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0100h	ETHER C0	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0108h	ETHER C0	Receive Frame Maximum Length Register	RFLR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0110h	ETHER C0	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0118h	ETHER C0	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0120h	ETHER C0	PHY Interface Register	PIR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0128h	ETHER C0	PHY Status Register	PSR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0140h	ETHER C0	Random Number Generation Counter Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0150h	ETHER C0	Interpacket Gap Register	IPGR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0154h	ETHER C0	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0158h	ETHER C0	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0160h	ETHER C0	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0164h	ETHER C0	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0168h	ETHER C0	PAUSE Frame Retransmit Counter	TPAUSECR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 016Ch	ETHER C0	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01C0h	ETHER C0	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01C8h	ETHER C0	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01D0h	ETHER C0	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01D4h	ETHER C0	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01D8h	ETHER C0	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01DCh	ETHER C0	Carrier Not Detect Counter Register	CNDCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01E4h	ETHER C0	CRC Error Frame Receive Counter Register	CEFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01E8h	ETHER C0	Frame Receive Error Counter Register	FRECR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01ECh	ETHER C0	Too-Short Frame Receive Counter Register	TSFRRCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01F0h	ETHER C0	Too-Long Frame Receive Counter Register	TLFRRCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01F4h	ETHER C0	Received Alignment Error Frame Counter Register	RFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C

Table 4.1 List of I/O Registers (Address Order) (52 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1290h	MTU0	Noise Filter Control Register 0	NFCR0	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1291h	MTU1	Noise Filter Control Register 1	NFCR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1292h	MTU2	Noise Filter Control Register 2	NFCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1293h	MTU3	Noise Filter Control Register 3	NFCR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1294h	MTU4	Noise Filter Control Register 4	NFCR4	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1298h	MTU8	Noise Filter Control Register 8	NFCR8	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1299h	MTU0	Noise Filter Control Register C	NFCRC	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1300h	MTU0	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1308h	MTU0	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1320h	MTU0	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1328h	MTU0	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1380h	MTU1	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1388h	MTU1	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1391h	MTU1	Timer Mode Register 3	TMDR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1394h	MTU1	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A0h	MTU1	Timer Longword Counter	TCNTLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A4h	MTU1	Timer Longword General Register	TGRALW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A8h	MTU1	Timer Longword General Register	TGRBLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1400h	MTU2	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less)Conditions: $V_{CC} = AVCC0 = AVCC1 = VCC_USB = 2.7$ to 3.6 V, 2.7 V $\leq VREFH0 \leq AVCC0$, $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item			Symbol	D version		G version		Unit	Test Conditions		
				Typ.	Max.	Typ.	Max.				
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	40	—	45	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz	
		Normal	Peripheral function clock signal supplied*4		22	—	22	—			
			Peripheral function clock signal stopped*4		12	—	12	—			
		Core Mark	Peripheral function clock signal stopped*4		15	—	15	—			
		Sleep mode: The clock signal to peripheral modules is supplied*4			16	24	16	28			
		All-module-clock-stop mode (reference value)			8	15	8	19			
		Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4			1.1	—	1.1	—			
		Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4			1.1	—	1.1	—			
		Software standby mode			1.6	6.4	1.6	9.8			
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)		15.5	61	15.5	85	μA	V _{BATT} = 2.0 V, V _{CC} = 0 V V _{BATT} = 3.3 V, V _{CC} = 0 V V _{BATT} = 2.0 V, V _{CC} = 0 V V _{BATT} = 3.3 V, V _{CC} = 0 V		
		Power not supplied to standby RAM and USB resume detecting unit (USB0 only)	Power-on reset circuit and low-power consumption function disabled*5	11.5	38	11.5	48				
			Power-on reset circuit and low-power consumption function enabled*6	4.9	29	4.9	39				
		Increased by RTC operation	When a low C _L crystal is in use	1	—	1	—				
			When a standard C _L crystal is in use	2	—	2	—				
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		0.9	—	0.9			—	
					1.6	—	1.6			—	
			When a crystal oscillator for standard clock loads is in use		1.7	—	1.7			—	
				3.3	—	3.3	—				
		Inrush current on returning from deep software standby mode	Inrush current*7	I _{RUSH}	—	70	—			70	mA
			Energy of inrush current*7	E _{RUSH}	—	1.0	—			1.0	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripheral modules is stopped in this state.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)

[D version]

 I_{CC} Max. = $0.31 \times f + 6.5$ (max. operation in high-speed operating mode) I_{CC} Typ. = $0.16 \times f + 2.8$ (ICLK 1 MHz max) (normal operation in high-speed operating mode) I_{CC} Typ. = $0.4 \times f + 1.1$ (low-speed operating mode 1) I_{CC} Max. = $0.15 \times f + 6.5$ (sleep mode)

[G version]

 I_{CC} Max. = $0.33 \times f + 9$ (max. operation in high-speed operating mode) I_{CC} Typ. = $0.16 \times f + 2.8$ (ICLK 1 MHz max) (normal operation in high-speed operating mode) I_{CC} Typ. = $0.4 \times f + 1.1$ (low-speed operating mode 1) I_{CC} Max. = $0.21 \times f + 9$ (sleep mode)

Note 4. Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D.

The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).

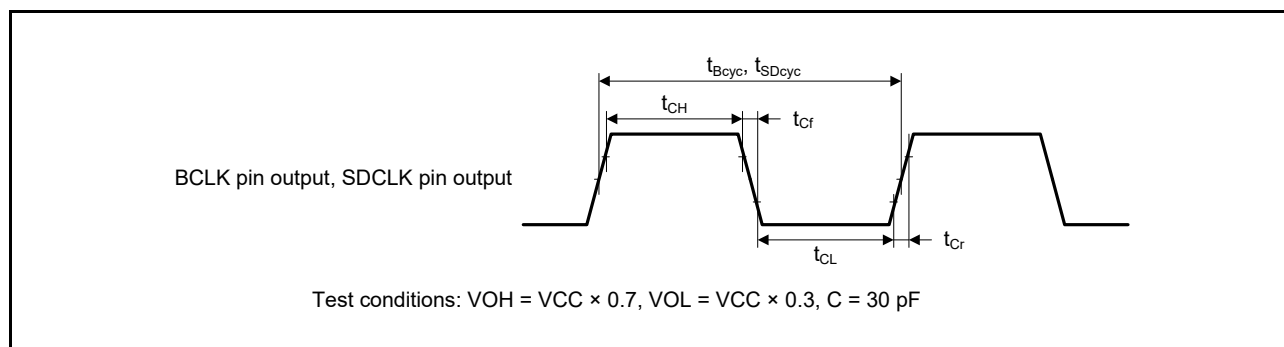
Note 5. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.

5.3.2 Clock Timing

Table 5.14 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	Figure 5.3
	100-pin package		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	

**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

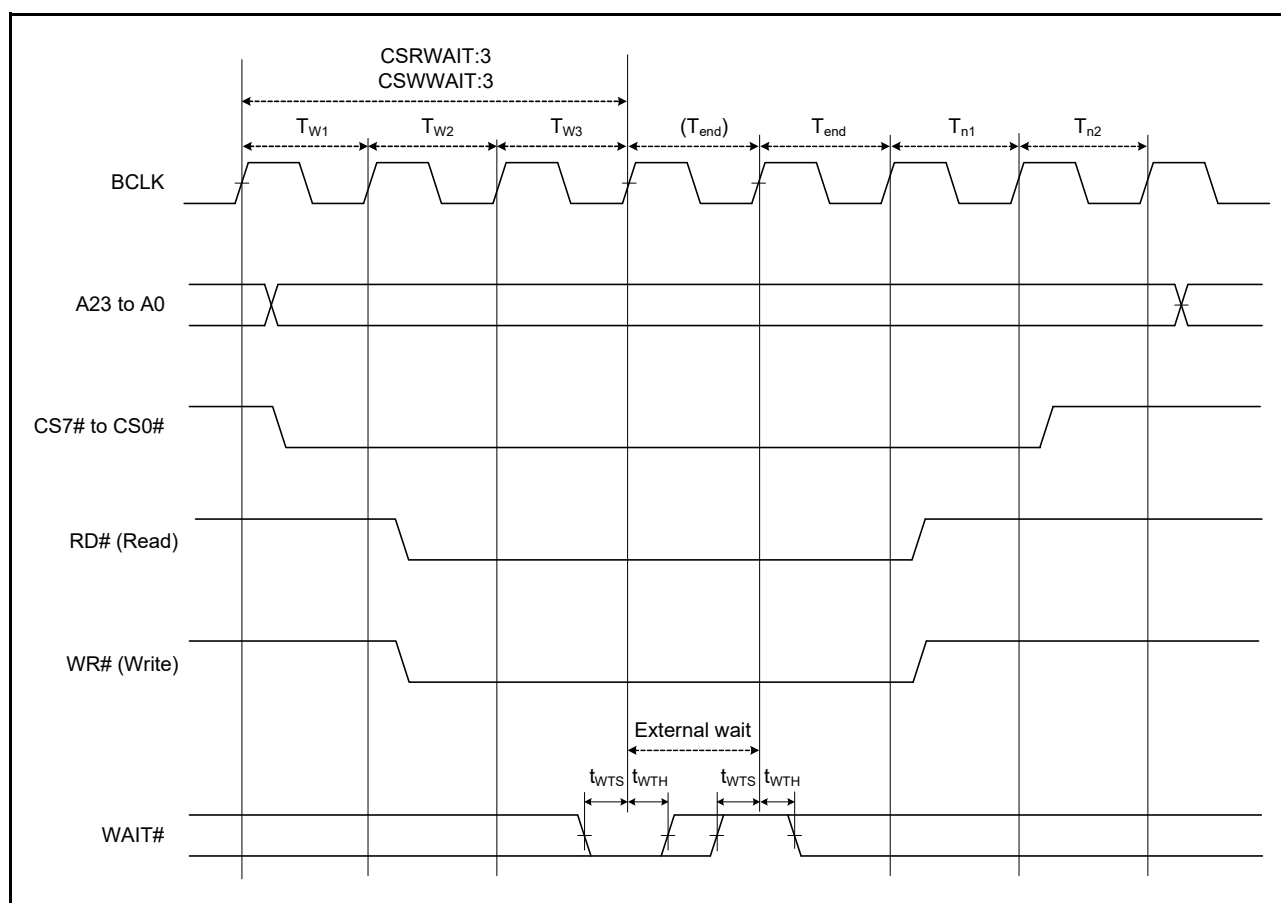


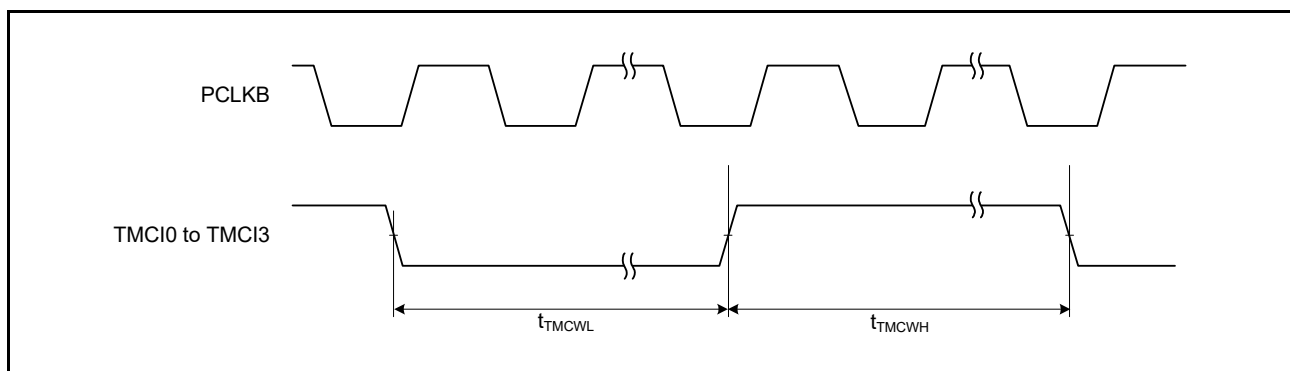
Figure 5.22 External Bus Timing/External Wait Control

Table 5.28 TMR Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH} , t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 5.36
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.36 TMR Clock Input Timing****Table 5.29 CMTW Timing**

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PBcyc}	Figure 5.37
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc} : PCLKB cycle

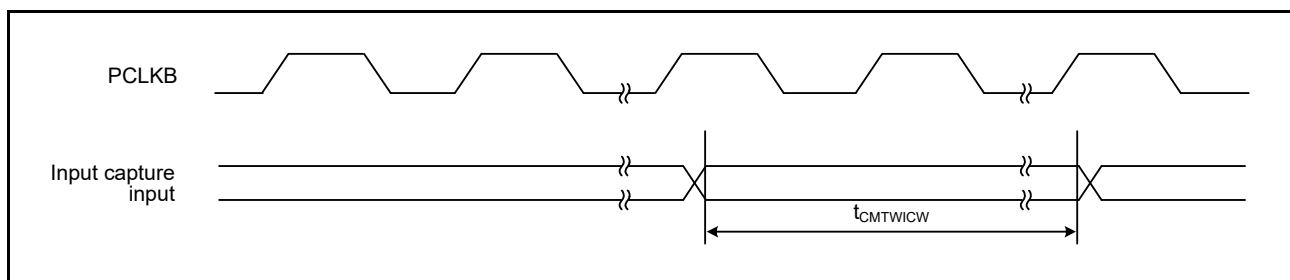
**Figure 5.37 CMTW Input Capture Input Timing**

Table 5.38 RIIC Timing (1)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.54
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 \times (\text{External pull-up voltage}/5.5V)$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 \times (\text{External pull-up voltage}/5.5V)$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

5.4 USB Characteristics

Table 5.44 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $3.0 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $UCLK = 48$ MHz,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

	Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	DP – DM
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	$I_{OH} = -200 \mu A$
	Output low level voltage	V_{OL}	0.0	—	0.3	V	$I_{OL} = 2$ mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 5.72
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR} / t_{LF}
Pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	k Ω	

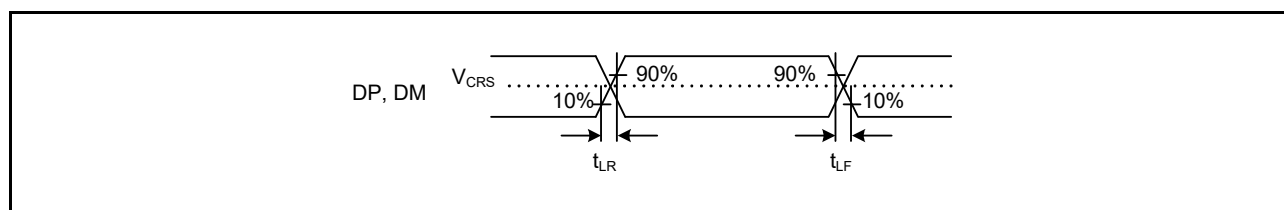
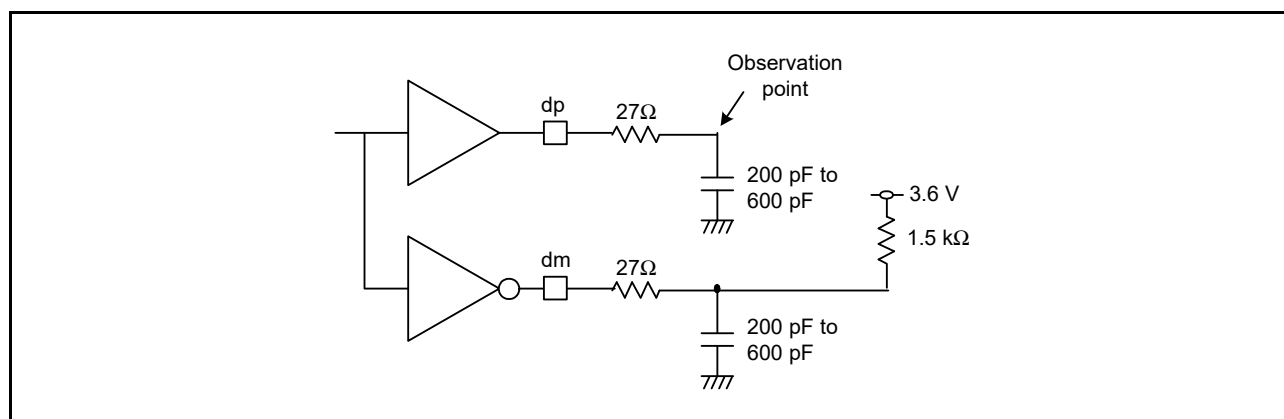
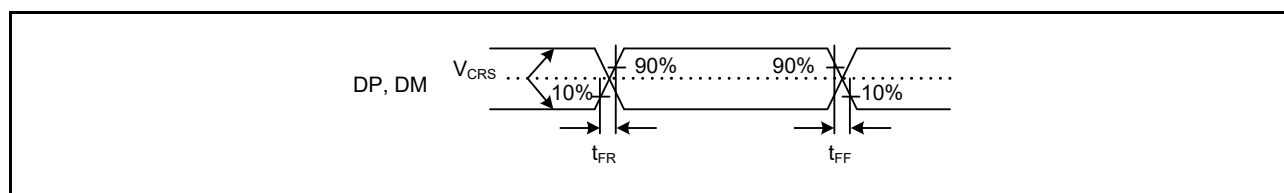
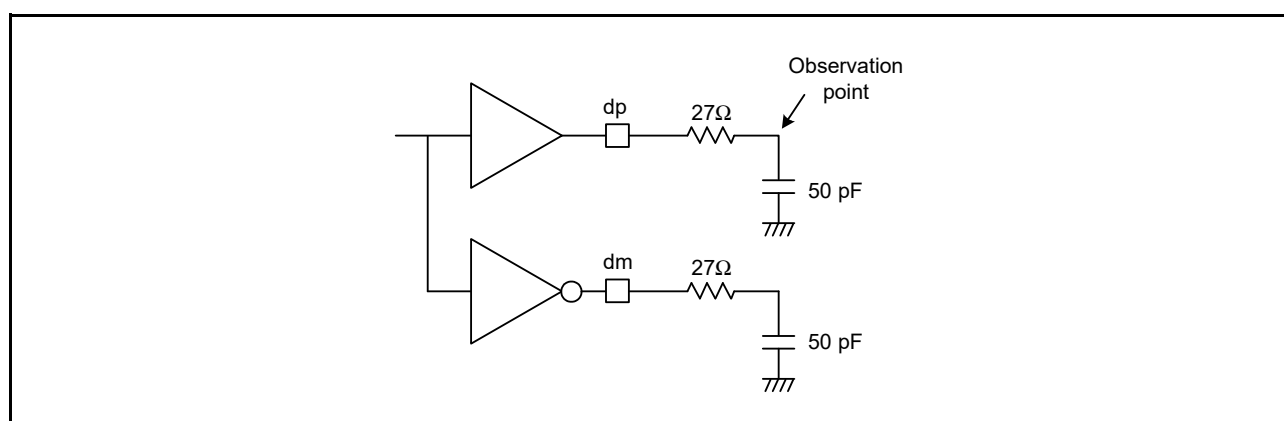
**Figure 5.72 DP and DM Output Timing (Low Speed)****Figure 5.73 Test Circuit (Low Speed)**

Table 5.45 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $3.0 \leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $U_{CLK} = 48$ MHz,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V
	Input low level voltage	V_{IL}	—	—	0.8	V
	Differential input sensitivity	V_{DI}	0.2	—	—	V
	Differential common mode range	V_{CM}	0.8	—	2.5	V
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V
	Output low level voltage	V_{OL}	0.0	—	0.3	V
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V
	Rise time	t_{FR}	4	—	20	ns
	Fall time	t_{FF}	4	—	20	ns
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	%
	Output resistance	Z_{DRV}	28	—	44	Ω
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	k Ω
			1.425	—	3.090	k Ω
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	k Ω

**Figure 5.74 DP and DM Output Timing (Full-Speed)****Figure 5.75 Test Circuit (Full-Speed)**

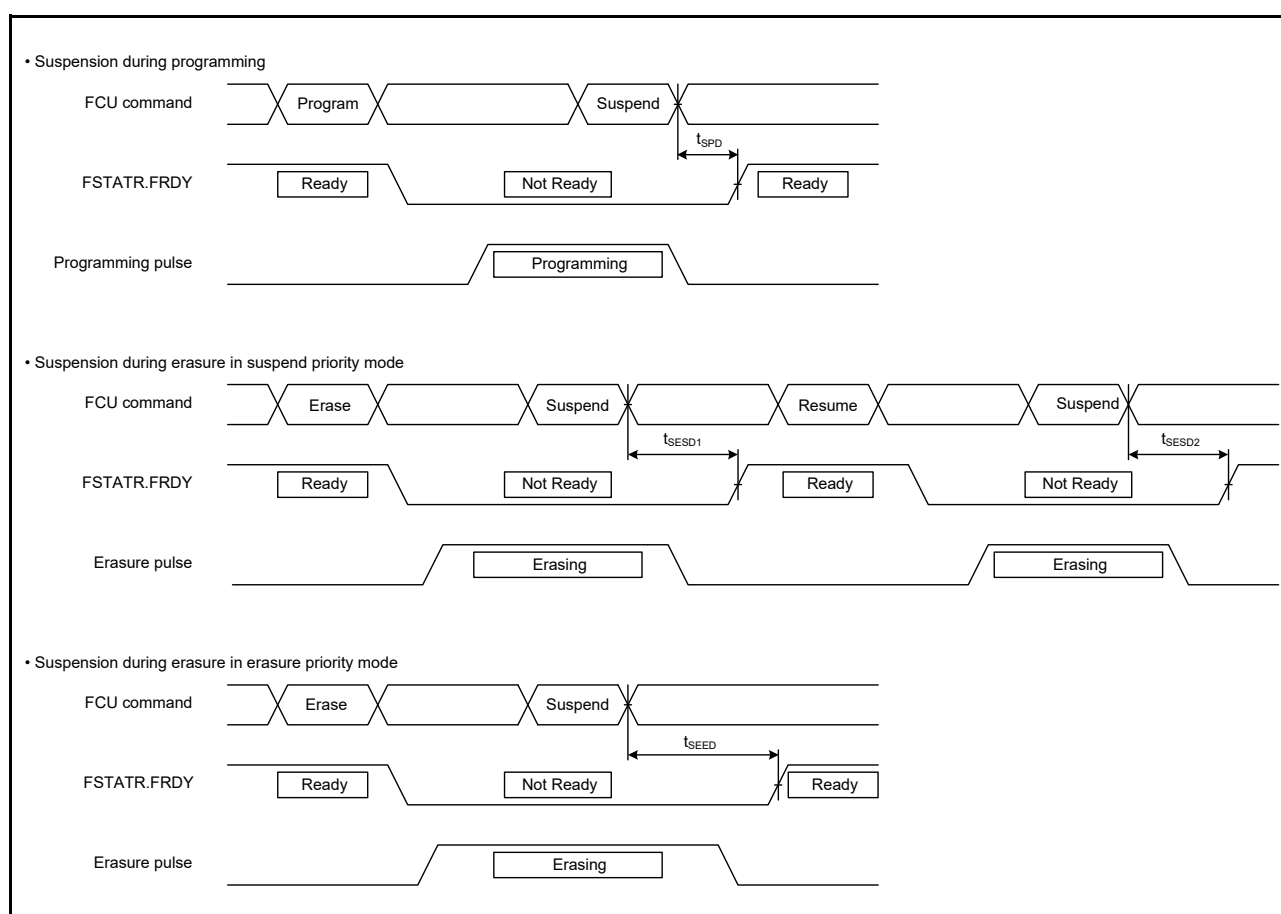


Figure 5.82 Flash Memory Programming/Erasure Suspension Timing