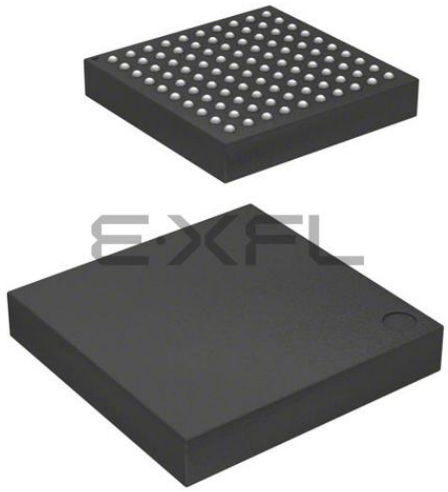
Renesas Electronics America Inc - R5F5651CDDLJ#20 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5651cddlj-20

Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (2/2)

Functions	Products	Products with 1 Mbyte of code flash memory or less		Products with at least 1.5 Mbytes of code flash memory		
	Package	145 Pins, 144 Pins	100 Pins	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
12-bit A/D converter		AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels)	AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels)	AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels)		AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels)
12-bit D/A converter		Ch. 0 and 1	Ch. 1	Ch. 0 and 1		Ch. 1
Temperature sensor		Available				
CRC calculator		Available				
Data operation circuit		Available				
Clock frequency accuracy measurement circuit		Available				
Encryption	AES	Available*1		Incorporated in the Trusted Secure IP		
	RNG	Available*1		Incorporated in the Trusted Secure IP		
	Trusted Secure IP	Not available		Available		
Event link controller		Available				

Note 1. Regarding the public release of this module, an exchange of non-disclosure agreement is necessary. For details, contact your Renesas sales agency.

Table 1.4 Pin Functions (5/8)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK0	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.
	RMII0_CRS_DV	Input	Indicate that there are carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode
	RMII0_RX_ER	Input	Indicate an error has occurred during reception of data in RMII mode.
	ET0_CRS	Input	Carrier detection/data reception enable pins
	ET0_RX_DV	Input	Indicate that there are valid receive data on ET0_ERXD3 to ET0_ERXD0.
	ET0_EXOUT	Output	General-purpose external output pins
	ET0_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable pins. Function as signals indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0.
	ET0_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY-LSI of an error during transmission.
	ET0_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timings from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER.
	ET0_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timings to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER.
	ET0_COL	Input	Input collision detection signals.
	ET0_WOL	Output	Receive Magic packets.
	ET0_MDC	Output	Output reference clock signals for information transfer via ET0_MDIO.
	ET0_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.
USB 2.0 host/function module	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB0_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA/ USB0_OVRCURB	Input	USB overcurrent pins
	USB0_VBUS	Input	USB cable connection/disconnection detection input pins
CAN module	CRX0, CRX1, CRX1-DS	Input	Input pins
	CTX0, CTX1	Output	Output pins

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
A1	AVSS0								
A2	AVCC0								
A3	VREFL0								
A4		P42						IRQ10-DS	AN002
A5		P46						IRQ14-DS	AN006
A6	VCC								
A7	VSS								
A8		P94	D20/A20						
A9	VCC								
A10	TRSYNC1	P97	D23/A23						
A11		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106
A12		P60	CS0#						
A13		P63	CAS#/ D2[A2/D2]/ CS3#						
A14		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B		ANEX1
A15		PE2	D10[A10/ D10]/D2[A2/ D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100
B1		P05						IRQ13	DA1
B2		P07						IRQ15	ADTRG0#
B3		P40						IRQ8-DS	AN000
B4		P41						IRQ9-DS	AN001
B5		P47						IRQ15-DS	AN007
B6		P91	D17/A17		SCK7				AN115
B7		P92	D18/A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B	IRQ1	AN109
B9	TRDATA5	P96	D22/A22						
B10		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
B11	TRDATA7	PG1	D25						
B12	VSS								
B13		P64	WE#/D3[A3/ D3]/CS4#						
B14		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B		ANEX0

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
D14		PE7	D15[A15/D15]/D7[A7/D7]	MTIOC6A/TOC1	MISOB-B	SDHI_WP/MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105
D15		P65	CKE/CS5#						
E1		PJ5		POE8#	CTS2#/RTS2#/SS2#				
E2	EMLE								
E3		PF5						IRQ4	
E4	VSS								
E5 *1	NC								
E12		PE6	D14[A14/D14]/D6[A6/D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/MMC_CD-B	LCD_DATA10-B	IRQ6	AN104
E13	TRDATA0	PG2	D26						
E14	TRDATA1	PG3	D27						
E15		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	VBATT								
F2	VCL								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#				
F4	BSCANP								
F12		P66	DQM0/CS6#	MTIOC7D					
F13	TRSYNC	PG4	D28						
F14		PA0	DQM2/BC0#/A0	MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF	ET0_TX_EN/RMII0_TXD_EN/SSLA1-B		LCD_DATA8-B		
F15	VSS								
G1	XCIN								
G2	XCOUT								
G3	MD/FINED								
G4	TRST#	PF4							
G12	TRCLK	PG5	D29						
G13	TRDATA2	PG6	D30						
G14		PA1	DQM3/A1	MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17	ET0_WOL/SCK5/SSLA2-B		LCD_DATA7-B	IRQ11	
G15	VCC								
H1	XTAL	P37							
H2	VSS								
H3	RES#								
H4	UPSEL	P35						NMI	
H12		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B		LCD_DATA4-B	IRQ5-DS	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (4/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
H12		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DATA0-B*1	IRQ12	
H13		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B*1		
J1	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
J2		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0	PCKO		IRQ3-DS	
J3		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC		IRQ2-DS	
J4	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
J10		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6	SDSI_D3-B	LCD_TCON1-B*1		
J11		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B*1		
J12		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2-B	LCD_TCON2-B*1		
J13		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		LCD_TCON3-B*1	IRQ4-DS	
K1	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A				
K2	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
K3	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
K4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	
K5	TRDATA2	P54	ALE/ D1[A1/D1]*1/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
K6		P53*2	BCLK						

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (3/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
49	VSS_USB								
50		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7*1				
51	TRDATA3	P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7*1/ SMOSI7*1/ SSDA7*1/CRX1			IRQ10	
52	TRDATA2	P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
53		P53*2	BCLK						
54		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
55		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
56		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
57	VSS								
58	TRCLK	P83	EDACK1	MTIOC4C	ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10#				
59	VCC								
60	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A	MMC_D7-A		IRQ14	
61		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A		IRQ13	
62		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A	MMC_D5-A			
63	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10	MMC_D4-A			
64	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A			
65	TRDATA0	P80	EDREQ0	MTIOC3B/ PO26	ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10#	QIO2-A/SDHI_WP/ MMC_D2-A			
66		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A	QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A			
67		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5	QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A			
68	TRDATA7	P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A			

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (5/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
87		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DATA0-B*1	IRQ12	
88		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B*1		
89		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B*1		
90		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B*1		
91	VCC								
92		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DATA4-B*1	IRQ5-DS	
93	VSS								
94		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DATA5-B*1	IRQ6-DS	
95		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DATA6-B*1		
96		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DATA7-B*1	IRQ11	
97		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DATA8-B*1		
98		P67	DQM1/CS7#	MTIOC7C				IRQ15	
99		P66	DQM0/CS6#	MTIOC7D					
100		P65	CKE/CS5#						
101		PE7	D15[A15/ D15]/D7[A7/ D7]*1	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DATA9-B*1	IRQ7	AN105
102		PE6	D14[A14/ D14]/D6[A6/ D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DATA10-B*1	IRQ6	AN104
103	VCC								
104		P70	SDCLK						
105	VSS								
106		PE5	D13[A13/ D13]/D5[A5/ D5]*1	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DATA11-B*1	IRQ5	AN103
107		PE4	D12[A12/ D12]/D4[A4/ D4]*1	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DATA12-B*1		AN102
108		PE3	D11[A11/ D11]/D3[A3/ D3]*1	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#/SS12#	MMC_D7-B	LCD_DATA13-B*1		AN101
109		PE2	D10[A10/ D10]/D2[A2/ D2]*1	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B*1	IRQ7-DS	AN100

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK		Operating Modes
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK		Operating Modes
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK		Low Power Consumption
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK		Low Power Consumption
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK		Low Power Consumption
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK		Low Power Consumption
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK		Clock Generation Circuit
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK		Clock Generation Circuit
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK		Clock Generation Circuit
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK		Clock Generation Circuit
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK		Clock Generation Circuit
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK		Clock Generation Circuit
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK		Clock Generation Circuit

Table 4.1 List of I/O Registers (Address Order) (34 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIh
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B321h	SCI12	Control Register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B322h	SCI12	Control Register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B323h	SCI12	Control Register 2	CR2	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B324h	SCI12	Control Register 3	CR3	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B325h	SCI12	Port Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B327h	SCI12	Status Register	STR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports

Table 4.1 List of I/O Registers (Address Order) (58 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 0400h to 000E 07FCh	GLCDC	Graphic 1 Color Look-up Table 1[0 to 255]	GR1CLUT1[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 0800h to 000E 0BFCh	GLCDC	Graphic 2 Color Look-up Table 0[0 to 255]	GR2CLUT0[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 0C00h to 000E 0FFCh	GLCDC	Graphic 2 Color Look-up Table 1[0 to 255]	GR2CLUT1[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 1000h	GLCDC	Background Generating Block Operation Control Register	BGEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1004h	GLCDC	Free-Running Period Register	BGPERI	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1008h	GLCDC	Synchronization Position Register	BGSYNC	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 100Ch	GLCDC	Vertical Size Register	BGVSIZE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1010h	GLCDC	Horizontal Size Register	BGHSIZE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1014h	GLCDC	Background Color Register	BGCOLOR	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1018h	GLCDC	Background Generating Block Status Monitor Register	BGMON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1100h	GLCDC	Graphic 1 Register Update Control Register	GR1VEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1104h	GLCDC	Graphic 1 Frame Buffer Read Control Register	GR1FLMRD	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 110Ch	GLCDC	Graphic 1 Frame Buffer Control Register 2	GR1FLM2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1110h	GLCDC	Graphic 1 Frame Buffer Control Register 3	GR1FLM3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1118h	GLCDC	Graphic 1 Frame Buffer Control Register 5	GR1FLM5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 111Ch	GLCDC	Graphic 1 Frame Buffer Control Register 6	GR1FLM6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1120h	GLCDC	Graphic 1 Alpha Blending Control Register 1	GR1AB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1124h	GLCDC	Graphic 1 Alpha Blending Control Register 2	GR1AB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1128h	GLCDC	Graphic 1 Alpha Blending Control Register 3	GR1AB3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 112Ch	GLCDC	Graphic 1 Alpha Blending Control Register 4	GR1AB4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1130h	GLCDC	Graphic 1 Alpha Blending Control Register 5	GR1AB5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1134h	GLCDC	Graphic 1 Alpha Blending Control Register 6	GR1AB6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1138h	GLCDC	Graphic 1 Alpha Blending Control Register 7	GR1AB7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 113Ch	GLCDC	Graphic 1 Alpha Blending Control Register 8	GR1AB8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1140h	GLCDC	Graphic 1 Alpha Blending Control Register 9	GR1AB9	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 114Ch	GLCDC	Graphic 1 Background Color Control Register	GR1BASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1150h	GLCDC	Graphic 1 CLUT/Interrupt Control Register	GR1CLUTINT	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1154h	GLCDC	Graphic 1 Status Monitor Register	GR1MON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1200h	GLCDC	Graphic 2 Register Update Control Register	GR2VEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1204h	GLCDC	Graphic 2 Frame Buffer Read Control Register	GR2FLMRD	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 120Ch	GLCDC	Graphic 2 Frame Buffer Control Register 2	GR2FLM2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1210h	GLCDC	Graphic 2 Frame Buffer Control Register 3	GR2FLM3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1218h	GLCDC	Graphic 2 Frame Buffer Control Register 5	GR2FLM5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 121Ch	GLCDC	Graphic 2 Frame Buffer Control Register 6	GR2FLM6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1220h	GLCDC	Graphic 2 Alpha Blending Control Register 1	GR2AB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1224h	GLCDC	Graphic 2 Alpha Blending Control Register 2	GR2AB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1228h	GLCDC	Graphic 2 Alpha Blending Control Register 3	GR2AB3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 122Ch	GLCDC	Graphic 2 Alpha Blending Control Register 4	GR2AB4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1230h	GLCDC	Graphic 2 Alpha Blending Control Register 5	GR2AB5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1234h	GLCDC	Graphic 2 Alpha Blending Control Register 6	GR2AB6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1238h	GLCDC	Graphic 2 Alpha Blending Control Register 7	GR2AB7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 123Ch	GLCDC	Graphic 2 Alpha Blending Control Register 8	GR2AB8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1240h	GLCDC	Graphic 2 Alpha Blending Control Register 9	GR2AB9	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 124Ch	GLCDC	Graphic 2 Background Color Control Register	GR2BASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1250h	GLCDC	Graphic 2 CLUT/Interrupt Control Register	GR2CLUTINT	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1254h	GLCDC	Graphic 2 Status Monitor Register	GR2MON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC

Table 5.4 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Input pull-up MOS current	Other than P35	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μA	V_{in} = VCC
Input capacitance	All input pins (except for ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	Ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM		—	—	16		

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

Table 5.12 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	32	—	264	kHz
	Peripheral module clock (PCLKA)			—	—	264	
	Peripheral module clock (PCLKB)			—	—	264	
	Peripheral module clock (PCLKC)*1			—	—	264	
	Peripheral module clock (PCLKD)*1			—	—	264	
	Flash-IF clock (FCLK)			32	—	264	
	External bus clock (BCLK)	Other than 100-pin package		—	—	264	
		100-pin package		—	—	264	
	BCLK pin output	Other than 100-pin package		—	—	264	
		100-pin package		—	—	264	
	SDRAM clock (SDCLK)	Other than 100-pin package		—	—	264	
	SDCLK pin output	Other than 100-pin package		—	—	264	

Note 1. The 12-bit A/D converter cannot be used.

Table 5.17 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.63	4.16	3.78	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 5.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	9.26	8.33	7.57	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 5.7

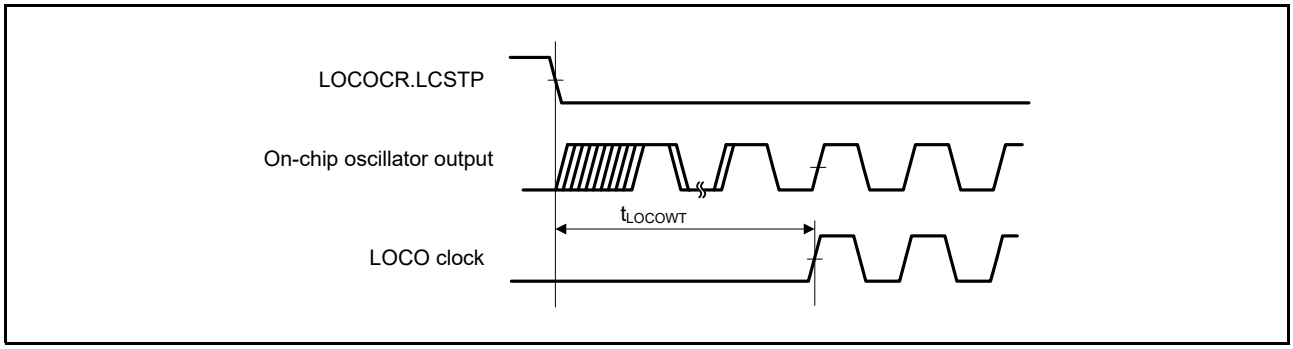


Figure 5.6 LOCO Clock Oscillation Start Timing

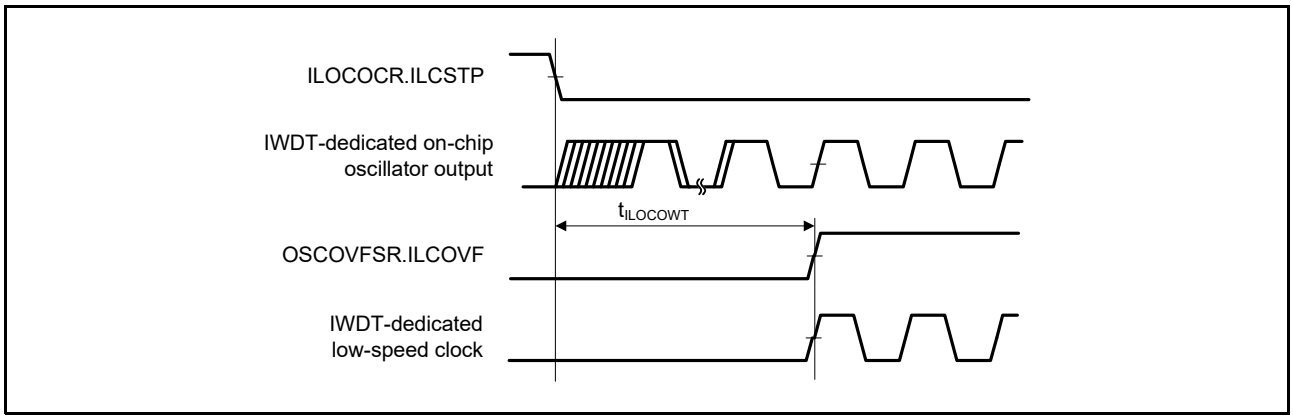


Figure 5.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 5.18 HOCO Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	–20°C ≤ T_a ≤ 85°C
		17.56	18	18.44	MHz	
		19.52	20	20.48	MHz	
		15.52	16	16.48	MHz	–40°C ≤ T_a < –20°C
		17.46	18	18.54	MHz	
		19.4	20	20.6	MHz	
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	µs	Figure 5.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	µs	Figure 5.9

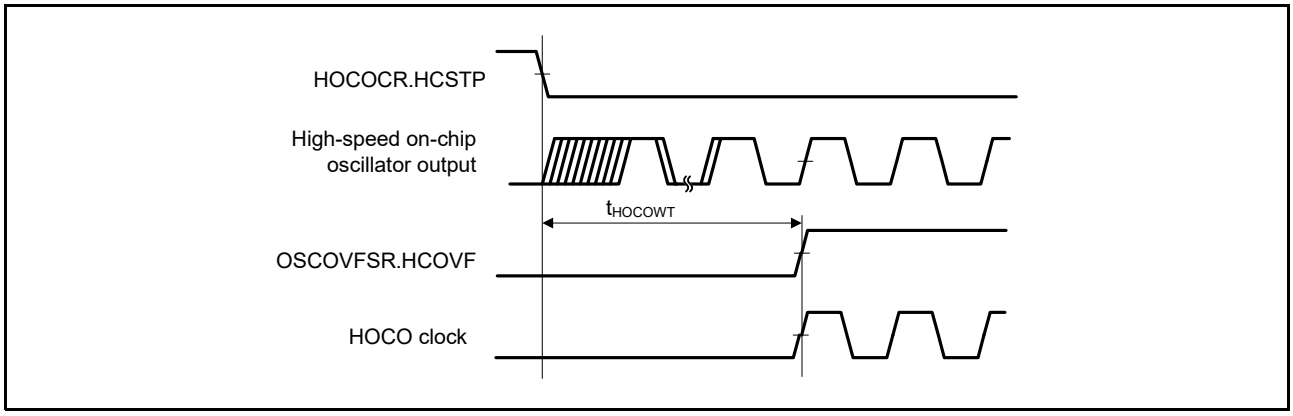


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

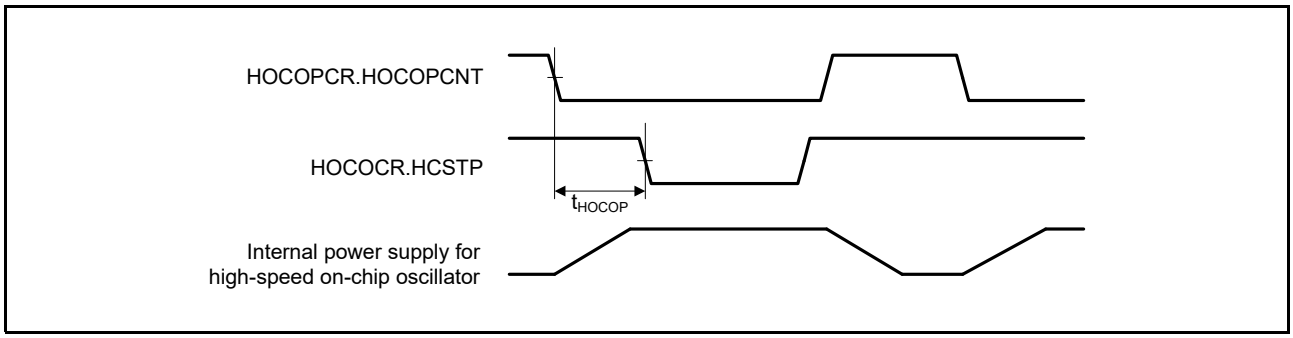


Figure 5.9 High-Speed On-Chip Oscillator Power Supply Control Timing

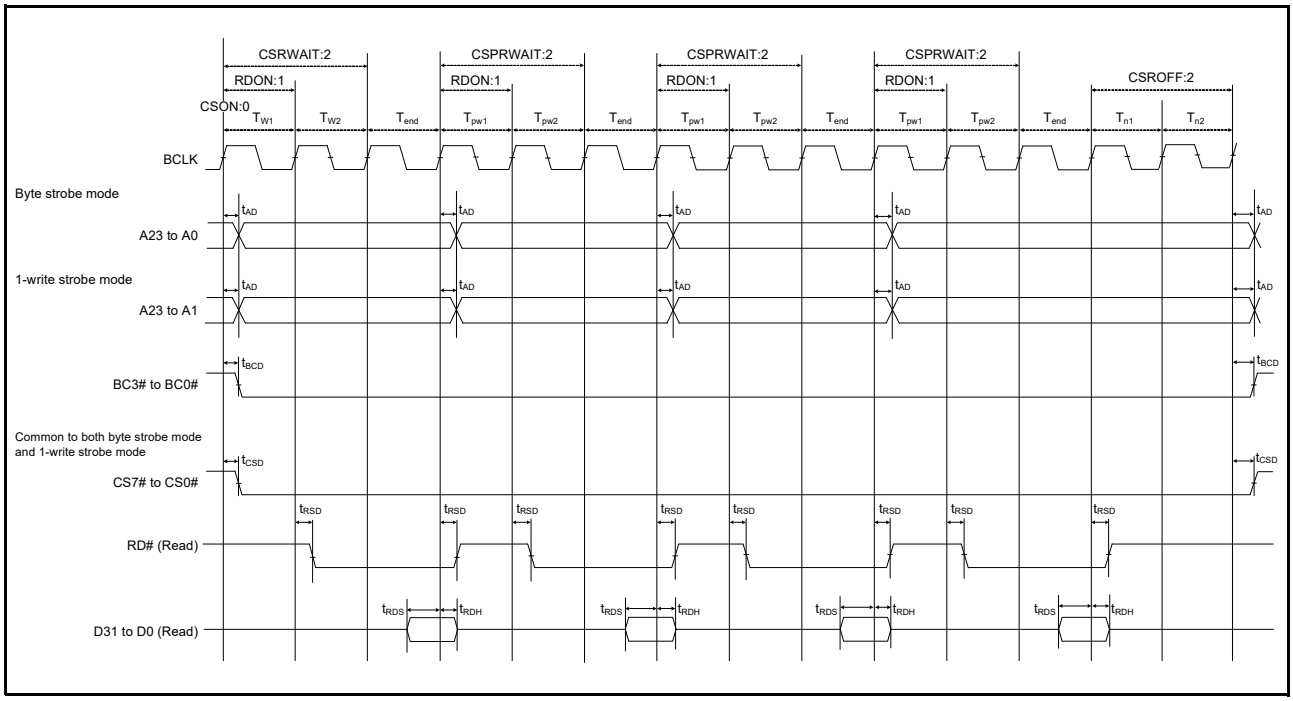


Figure 5.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

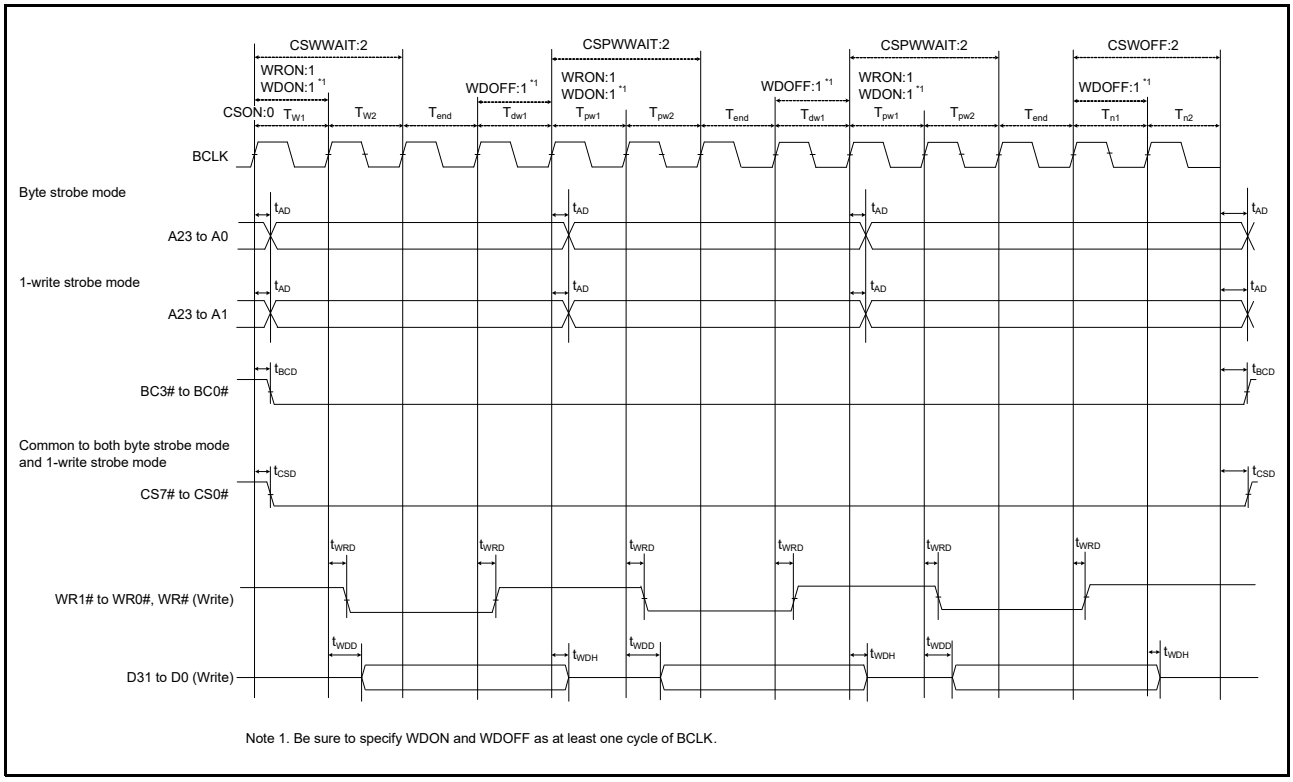


Figure 5.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

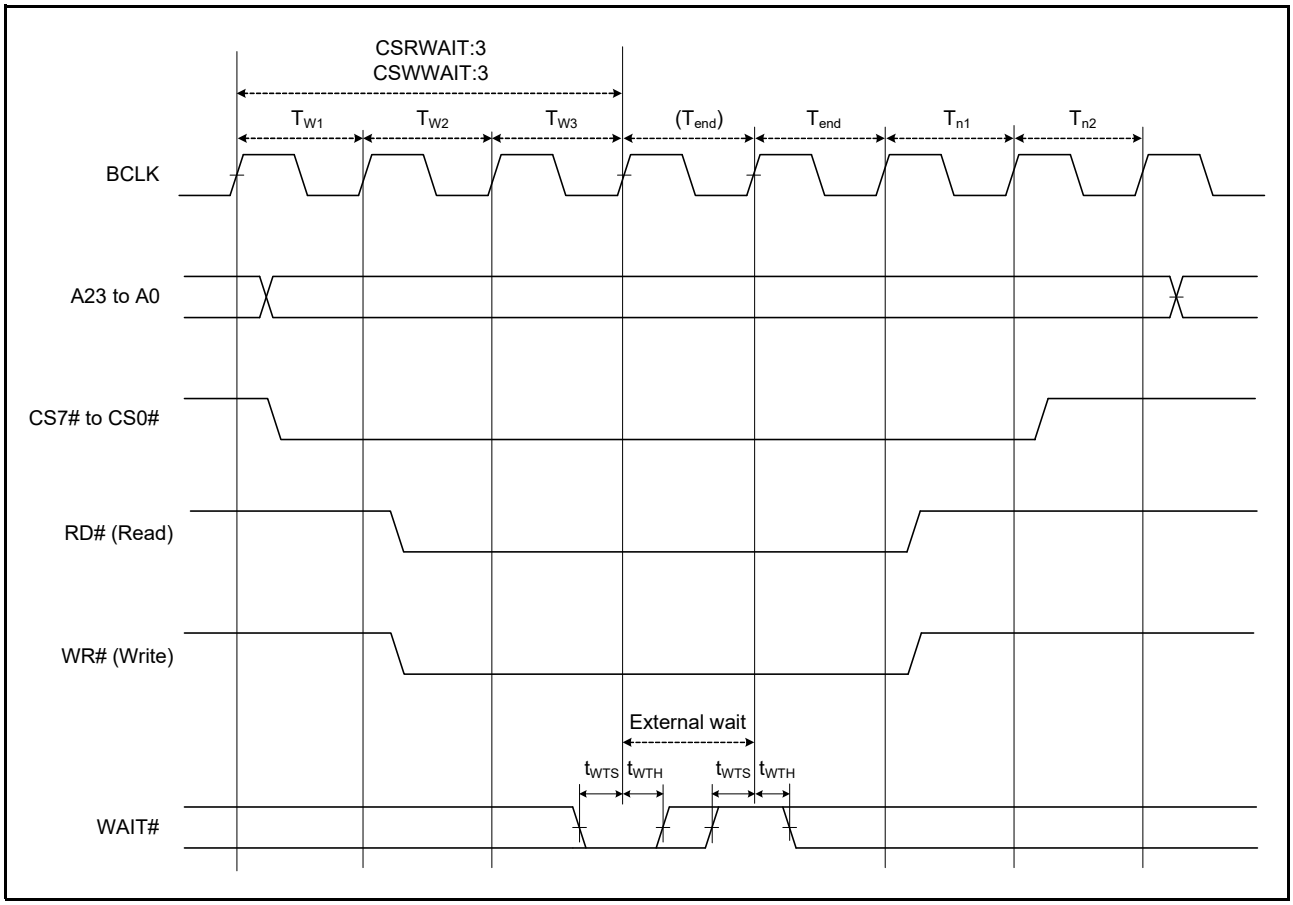


Figure 5.22 External Bus Timing/External Wait Control

Table 5.27 TPU Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PBcyc}	Figure 5.34
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PBcyc}	Figure 5.35
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

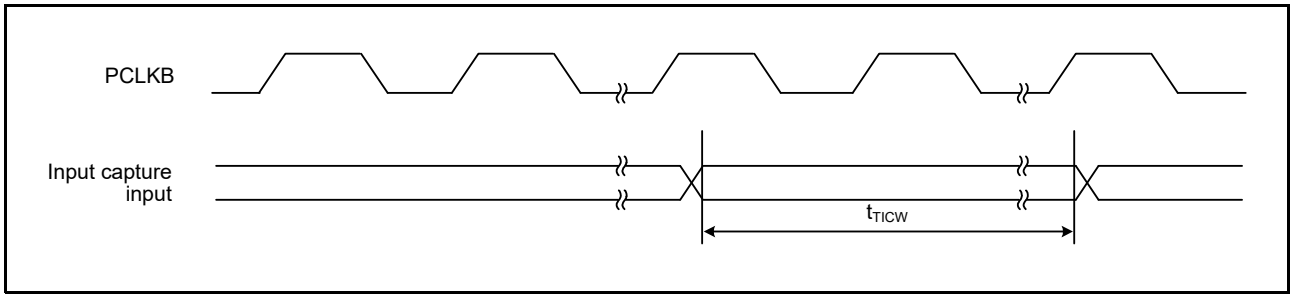


Figure 5.34 TPU Input Capture Input Timing

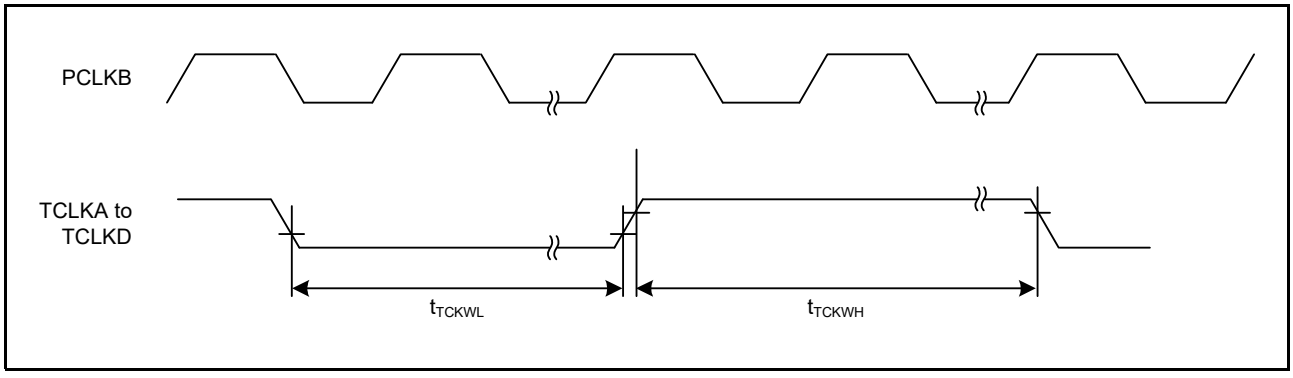


Figure 5.35 TPU Clock Input Timing

Table 5.40 MMC Host Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions*2
MMCIF	MMC_CLK clock cycle	t_{MMCPP}	2 × t_{PBcyc}	—	ns	Figure 5.55
	MMC_CLK clock high level width	t_{MMCWH}	6.5	—	ns	
	MMC_CLK clock low level width	t_{MMCWL}	6.5	—	ns	
	MMC_CLK clock rising time	t_{MMCLH}	—	3	ns	
	MMC_CLK clock falling time	t_{MMCHL}	—	3	ns	
	MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode)	$t_{MMCODLY}$	–6.6	6.6	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data setup	t_{MMCISU}	8	—	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data hold	t_{MMCIH}	2.5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the MMC interface, the AC portion of the electrical characteristics is measured for each group.

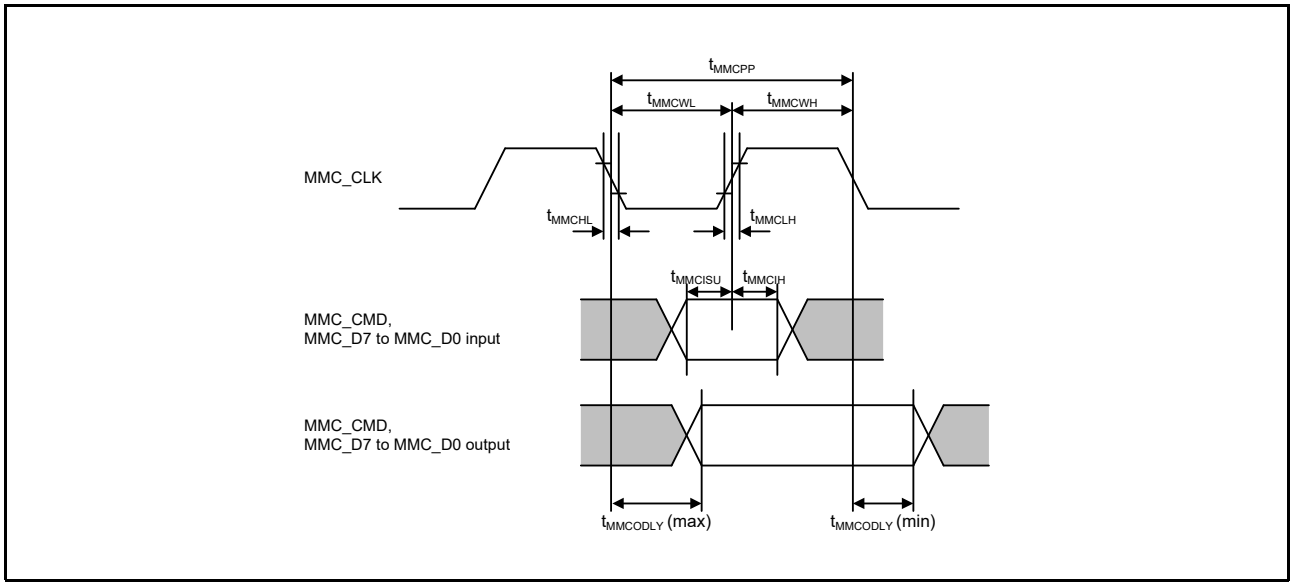
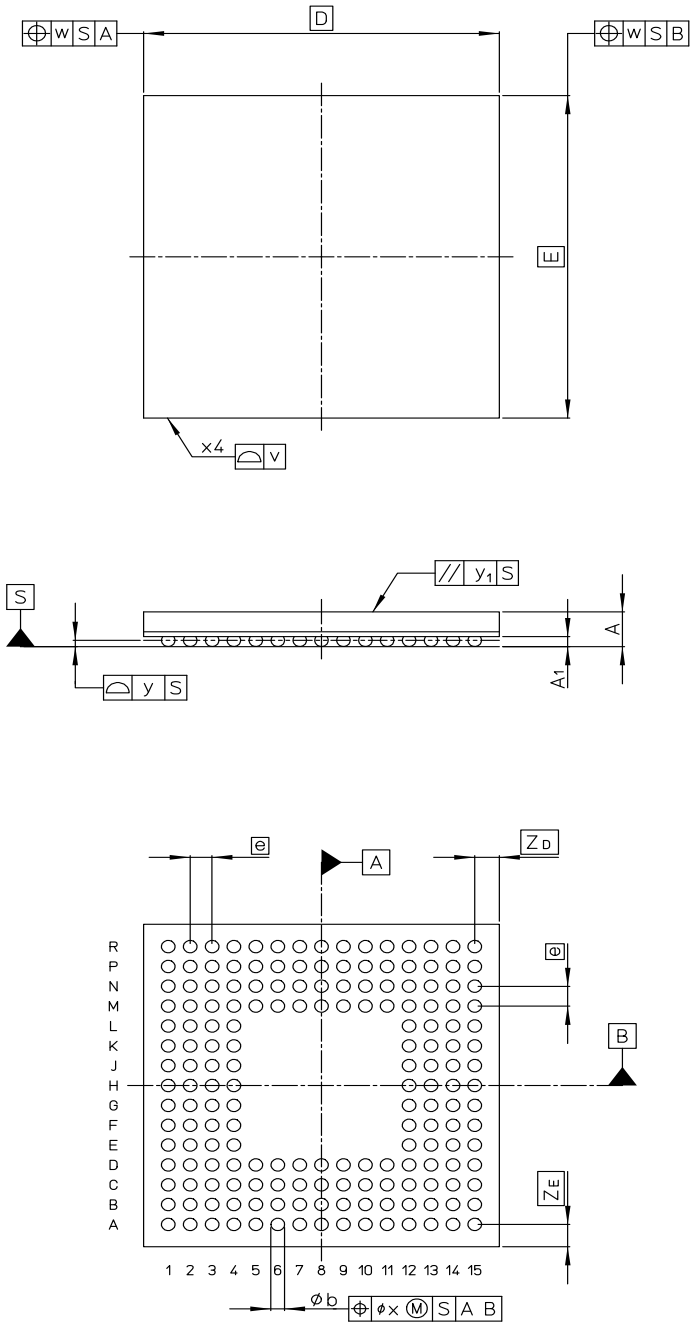


Figure 5.55 MMC Interface

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.2
SD	—	—	—
SE	—	—	—
ZD	—	0.90	—
ZE	—	0.90	—

Figure B 176-Pin LFBGA (PLBG0176GA-A)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.