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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5651eddfp-30

Table 1.1 Outline of Specifications (8/9)

Classification	Module/Function	Description
12-bit A/D converter (S12ADFa)		• 12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels) • 12-bit resolution (switchable between 8, 10, and 12 bits) • Conversion time 0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control (only for 3 group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU3, TMR, TPU) trigger, external trigger • Event linking by the ELC
12-bit D/A converter (R12DA)		• 2 channels • 12-bit resolution • Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output) • Buffered output or unbuffered output can be selected. • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ± 1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available

Table 1.1 Outline of Specifications (9/9)

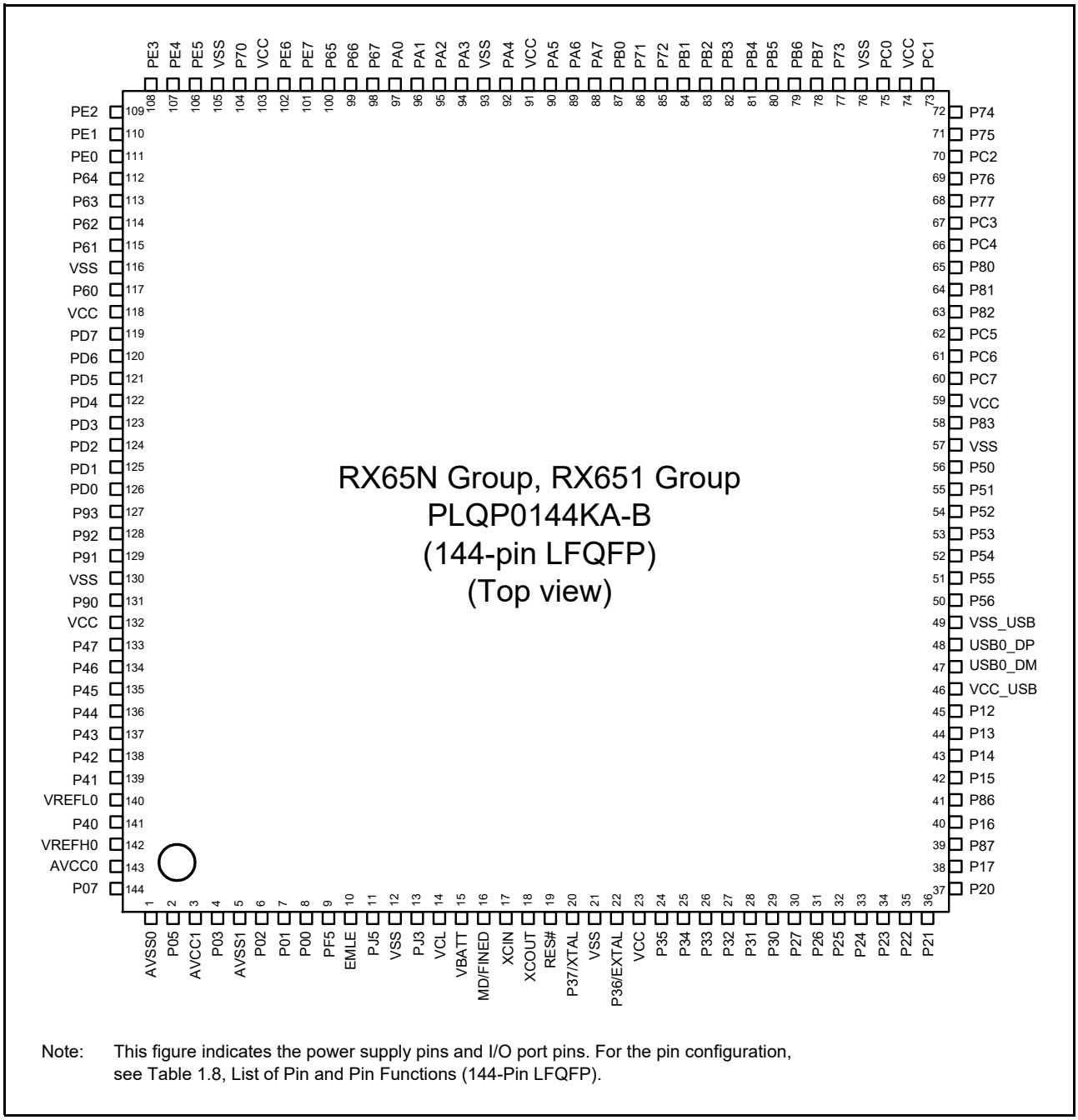
Classification	Module/Function	Description
Safety	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	• The function to compare, add, or subtract 16-bit data
Encryption function	AESa*2	• Key lengths: 128, 192, and 256 bits • Support for CFB, OFB, and CMAC operating modes • Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles • Compliant with FIPS PUB 197
	True random number generator (RNG)*2	• Length of random numbers: 16 bits • Generation of random-number-generated interrupts after a number is generated • Random number generation time: 1.9 ms (typ)
	Trusted Secure IP (TSIP)*2	• Security algorithm Common key encryption: AES (compliant with NIST FIPS PUB 197), 3DES, ARC4 Non-common key encryption: RSA • Other features TRNG (true-random number generator) Hash value generation: SHA1, SHA224, SHA256, GHASH Support of unique ID
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, V_{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-B) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-B)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. The product part number differs according to whether or not the MCU includes the encryption function.
Note 3. The product part number differs according to whether or not the MCU includes an SDHI (SD host interface)/SDSI (SD slave interface) (products with 1 Mbyte of code flash memory or less).
Note 4. When the realtime clock is not used, initialize the registers in the time clock according to description in section 31.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.

Table 1.2 Code Flash Memory Capacity and Comparison of Functions for Different Packages (2/2)

Functions	Products	Products with 1 Mbyte of code flash memory or less		Products with at least 1.5 Mbytes of code flash memory		
	Package	145 Pins, 144 Pins	100 Pins	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
12-bit A/D converter		AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels)	AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels)	AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels)		AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels)
12-bit D/A converter		Ch. 0 and 1	Ch. 1	Ch. 0 and 1		Ch. 1
Temperature sensor		Available				
CRC calculator		Available				
Data operation circuit		Available				
Clock frequency accuracy measurement circuit		Available				
Encryption	AES	Available*1		Incorporated in the Trusted Secure IP		
	RNG	Available*1		Incorporated in the Trusted Secure IP		
	Trusted Secure IP	Not available		Available		
Event link controller		Available				

Note 1. Regarding the public release of this module, an exchange of non-disclosure agreement is necessary. For details, contact your Renesas sales agency.



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.7 Pin Assignment (144-Pin LFQFP)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (7/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
P3		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C/PIXD2			
P4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		LCD_CLK-A	IRQ4	
P5	VSS_USB								
P6	VCC_USB								
P7		P57			RXD7/SMISO7/ SSCL7/SSLC0-B		LCD_DATA3-A		
P8		P10	ALE	MTIC5W/ TMRI3				IRQ0	
P9		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
P10		P83	EDACK1	MTIOC4C	ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10#		LCD_DATA8-A		
P11		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A	LCD_DATA10-A	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A	QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A	LCD_DATA15-A		
P13		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A	LCD_DATA19-A		
P14		P75	CS5#	PO20	ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11#	SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A	LCD_DATA20-A		
P15	VCC								
R1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN	SDHI_CLK-C/ PIXD5		IRQ9	
R2		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID	SDHI_CMD-C/ PIXD4		IRQ8	
R3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB			IRQ6	ADTRG0#
R4		P13	WR2#/BC2#	MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		LCD_TCON0-A	IRQ3	ADTRG1#
R5					USB0_DM				
R6					USB0_DP				
R7		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7/RSPCKC-B		LCD_DATA4-A		
R8		P11		MTIC5V/TMCI3	SCK2		LCD_DATA7-A	IRQ1	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (7/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
N7	TRDATA3	P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7*1/ SMOSI7*1/ SSDA7*1/CRX1			IRQ10	
N8	VSS								
N9	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A	MMC_D7-A		IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10	MMC_D4-A			
N11		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5	QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A			
N12	TRSYNC1	P75	CS5#	PO20	ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11#	SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A			
N13	TRDATA5	P74	A20/CS4#	PO19	ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11#				

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
45	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A			IRQ14	
46		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A			IRQ13	
47		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A				
48		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A				
49		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5				
50		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A				
51		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
52		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
53		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
54		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
55		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CLK-B*1		
56		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B*1		
57		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK6	SDSI_D3-B	LCD_TCON1-B*1		
58		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6#	SDSI_D2-B	LCD_TCON2-B*1		
59		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6		LCD_TCON3-B*1	IRQ4-DS	

Table 4.1 List of I/O Registers (Address Order) (13 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 79F1h	ICU	Software Configurable Interrupt A Source Select Register 241	SLIAR241	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F2h	ICU	Software Configurable Interrupt A Source Select Register 242	SLIAR242	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F3h	ICU	Software Configurable Interrupt A Source Select Register 243	SLIAR243	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F4h	ICU	Software Configurable Interrupt A Source Select Register 244	SLIAR244	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F5h	ICU	Software Configurable Interrupt A Source Select Register 245	SLIAR245	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F6h	ICU	Software Configurable Interrupt A Source Select Register 246	SLIAR246	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F7h	ICU	Software Configurable Interrupt A Source Select Register 247	SLIAR247	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F8h	ICU	Software Configurable Interrupt A Source Select Register 248	SLIAR248	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F9h	ICU	Software Configurable Interrupt A Source Select Register 249	SLIAR249	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FAh	ICU	Software Configurable Interrupt A Source Select Register 250	SLIAR250	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FBh	ICU	Software Configurable Interrupt A Source Select Register 251	SLIAR251	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FCh	ICU	Software Configurable Interrupt A Source Select Register 252	SLIAR252	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FDh	ICU	Software Configurable Interrupt A Source Select Register 253	SLIAR253	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FEh	ICU	Software Configurable Interrupt A Source Select Register 254	SLIAR254	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FFh	ICU	Software Configurable Interrupt A Source Select Register 255	SLIAR255	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7A00h	ICU	Software Configurable Interrupt Source Select Register Write Protect Register	SLIPRCR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 7A01h	ICU	EXDMAC Trigger Select Register	SELEXDR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK	IWDTa

Table 4.1 List of I/O Registers (Address Order) (27 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A08Ah	SCI4	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Bh	SCI4	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Ch	SCI4	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A091h	SCI4	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A090h	SCI4	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A092h	SCI4	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A9h	SCI5	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0AAh	SCI5	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0ABh	SCI5	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (28 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0ACh	SCI5	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0C9h	SCI6	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CAh	SCI6	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CBh	SCI6	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CCh	SCI6	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (29 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E0h	SCI7	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E1h	SCI7	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E2h	SCI7	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E3h	SCI7	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E4h	SCI7	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E5h	SCI7	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E6h	SMCI7	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E7h	SCI7	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E8h	SCI7	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E9h	SCI7	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EAh	SCI7	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EBh	SCI7	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0ECh	SCI7	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EDh	SCI7	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EEh	SCI7	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EFh	SCI7	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (55 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 0044h	SCI10	Serial Status Register	SSR/ SSRFIFO	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0045h	SCI10	Receive Data Register	RDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0046h	SMCI10	Smart Card Mode Register	SCMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0047h	SCI10	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0048h	SCI10	Noise Filter Setting Register	SNFR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0049h	SCI10	I2C Mode Register 1	SIMR1	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Ah	SCI10	I2C Mode Register 2	SIMR2	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Bh	SCI10	I2C Mode Register 3	SIMR3	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Ch	SCI10	I2C Status Register	SISR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Dh	SCI10	SPI Mode Register	SPMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Eh	SCI10	Transmit Data Register H	TDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Fh	SCI10	Transmit Data Register L	TDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Eh	SCI10	Transmit Data Register HL	TDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 004Eh	SCI10	Transmit FIFO Data Register	FTDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Fh	SCI10	Transmit FIFO Data Register	FTDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 004Eh	SCI10	Transmit FIFO Data Register	FTDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0050h	SCI10	Receive Data Register H	RDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0051h	SCI10	Receive Data Register L	RDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0050h	SCI10	Receive Data Register HL	RDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0050h	SCI10	Receive FIFO Data Register	FRDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0051h	SCI10	Receive FIFO Data Register	FRDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0050h	SCI10	Receive FIFO Data Register	FRDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0052h	SCI10	Modulation Duty Register	MDDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0053h	SCI10	Data Comparison Control Register	DCCR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0054h	SCI10	FIFO Control Register	FCR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0055h	SCI10	FIFO Control Register	FCR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0054h	SCI10	FIFO Control Register	FCR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0056h	SCI10	FIFO Data Count Register	FDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0057h	SCI10	FIFO Data Count Register	FDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0056h	SCI10	FIFO Data Count Register	FDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0058h	SCI10	Line Status Register	LSR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0059h	SCI10	Line Status Register	LSR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0058h	SCI10	Line Status Register	LSR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 005Ah	SCI10	Comparison Data Register	CDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 005Bh	SCI10	Comparison Data Register	CDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 005Ah	SCI10	Comparison Data Register	CDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 005Ch	SCI10	Serial Port Register	SPTR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0060h	SCI11	Serial Mode Register	SMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0061h	SCI11	Bit Rate Register	BRR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0062h	SCI11	Serial Control Register	SCR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0063h	SCI11	Transmit Data Register	TDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0064h	SCI11	Serial Status Register	SSR/ SSRFIFO	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0065h	SCI11	Receive Data Register	RDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0066h	SMCI11	Smart Card Mode Register	SCMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0067h	SCI11	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0068h	SCI11	Noise Filter Setting Register	SNFR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0069h	SCI11	I2C Mode Register 1	SIMR1	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Ah	SCI11	I2C Mode Register 2	SIMR2	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Bh	SCI11	I2C Mode Register 3	SIMR3	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi

Table 4.1 List of I/O Registers (Address Order) (56 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 006Ch	SCI11	I²C Status Register	SISR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Dh	SCI11	SPI Mode Register	SPMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Eh	SCI11	Transmit Data Register H	TDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Fh	SCI11	Transmit Data Register L	TDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Eh	SCI11	Transmit Data Register HL	TDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 006Eh	SCI11	Transmit FIFO Data Register	FTDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Fh	SCI11	Transmit FIFO Data Register	FTDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 006Eh	SCI11	Transmit FIFO Data Register	FTDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0070h	SCI11	Receive Data Register H	RDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0071h	SCI11	Receive Data Register L	RDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0070h	SCI11	Receive Data Register HL	RDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0070h	SCI11	Receive FIFO Data Register	FRDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0071h	SCI11	Receive FIFO Data Register	FRDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0070h	SCI11	Receive FIFO Data Register	FRDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0072h	SCI11	Modulation Duty Register	MDDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0073h	SCI11	Data Comparison Control Register	DCCR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0074h	SCI11	FIFO Control Register	FCR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0075h	SCI11	FIFO Control Register	FCR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0074h	SCI11	FIFO Control Register	FCR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0076h	SCI11	FIFO Data Count Register	FDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0077h	SCI11	FIFO Data Count Register	FDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0076h	SCI11	FIFO Data Count Register	FDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 0078h	SCI11	Line Status Register	LSR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0079h	SCI11	Line Status Register	LSR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0078h	SCI11	Line Status Register	LSR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 007Ah	SCI11	Comparison Data Register	CDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 007Bh	SCI11	Comparison Data Register	CDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 007Ah	SCI11	Comparison Data Register	CDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCIi
000D 007Ch	SCI11	Serial Port Register	SPTR	8	8	3, 4 PCLKA	1, 2 ICLK	SCIi
000D 0100h	RSPI0	RSPI Control Register	SPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0101h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0102h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0103h	RSPI0	RSPI Status Register	SPSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0104h	RSPI0	RSPI Data Register	SPDR	32	8, 16, 32	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0108h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0109h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0110h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0112h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0114h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0116h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0118h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 011Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 011Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc

Table 4.1 List of I/O Registers (Address Order) (61 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 3098h	DRW2D	U Limiter Y-Axis Increment Register	LUYADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 309Ch	DRW2D	V Limiter Start Value Integer Part Register	LVSTI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A0h	DRW2D	V Limiter Start Value Fractional Part Register	LVSTF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A4h	DRW2D	V Limiter X-Axis Increment Integer Part Register	LVXADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A8h	DRW2D	V Limiter Y-Axis Increment Integer Part Register	LVYADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30ACh	DRW2D	V Limiter Increment Fractional Parts Register	LVYXADDF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B4h	DRW2D	Texels Per Texture Line Register	TEXPITCH	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B8h	DRW2D	Texture Mask Register	TEXMSK	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30BCh	DRW2D	Texture Base Address Register	TEXORG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C0h	DRW2D	Interrupt Control Register	IRQCTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C4h	DRW2D	Cache Control Register	CACHECTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C8h	DRW2D	Display List Start Address Register	DLISTST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30CCh	DRW2D	Performance Counter 1	PERFCNT1	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D0h	DRW2D	Performance Counter 2	PERFCNT2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D4h	DRW2D	Performance Counters Control Register	PERFTRG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30DCh	DRW2D	CLUT Start Address Register	TEXCLADDR	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E0h	DRW2D	CLUT Data Register	TEXCLDATA	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E4h	DRW2D	CLUT Offset Register	TEXCLOFST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E8h	DRW2D	Chroma Key Register	COLKEY	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
007F C040h	FLASH	Data Flash Memory Access Frequency Setting Register	EEPFCLK	8	8	2 FCLK		Flash
FE7F 7D7Ch	TEMPS	Temperature Sensor Calibration Data Register	TSCDR	32	32	1 to 3 ICLK		TEMPS
FE7F 7D90h	FLASH	Unique ID Register 0	UIDR0	32	32	1 to 3 ICLK		Flash
FE7F 7D94h	FLASH	Unique ID Register 1	UIDR1	32	32	1 to 3 ICLK		Flash
FE7F 7D98h	FLASH	Unique ID Register 2	UIDR2	32	32	1 to 3 ICLK		Flash
FE7F 7D9Ch	FLASH	Unique ID Register 3	UIDR3	32	32	1 to 3 ICLK		Flash

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 0008 81ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 0008 81EEh and 0008 81ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 0008 81EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 0008 81EFh and 0008 81EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 0008 81FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 0008 81FEh and 0008 81FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 0008 81FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 0008 81FFh and 0008 81FDh, respectively.

Note 5. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 6. The address must end with 0h, 4h, 8h, or Ch when access is made in 32-bit units. The address must end with 0h, 2h, 4h, 6h, 8h, Ah, Ch, or Eh when access is made in 16-bit units.

Note 7. When the register is accessed while the GLCDC is operating, a delay may be generated in accessing.

Table 5.17 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.63	4.16	3.78	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 5.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	9.26	8.33	7.57	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 5.7

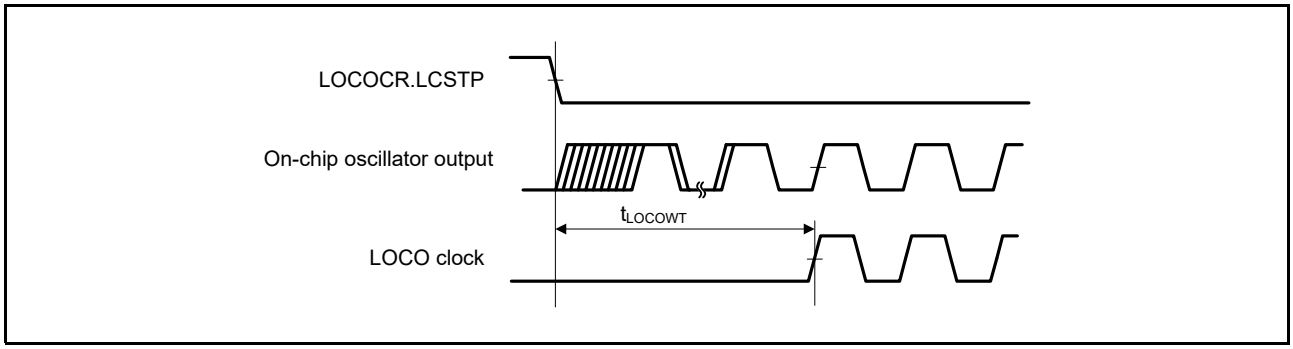


Figure 5.6 LOCO Clock Oscillation Start Timing

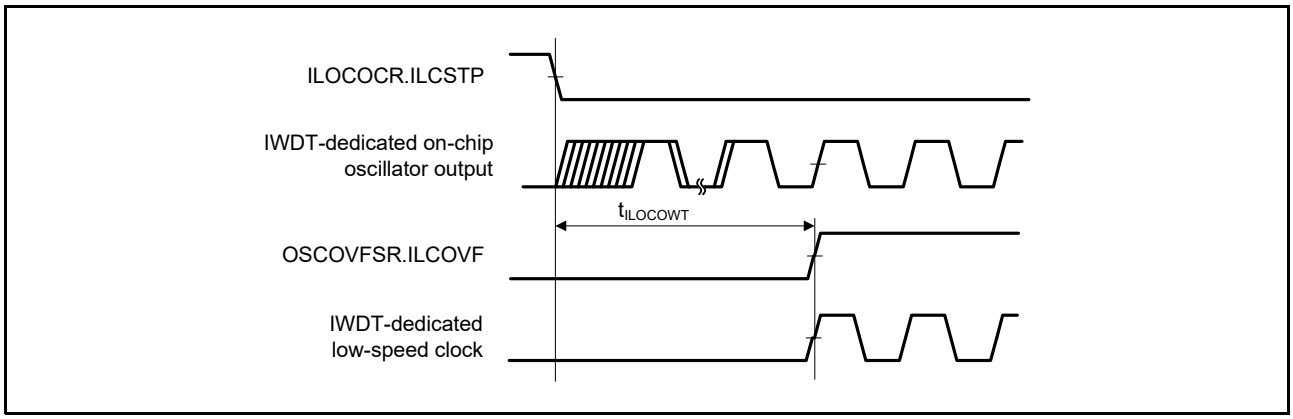
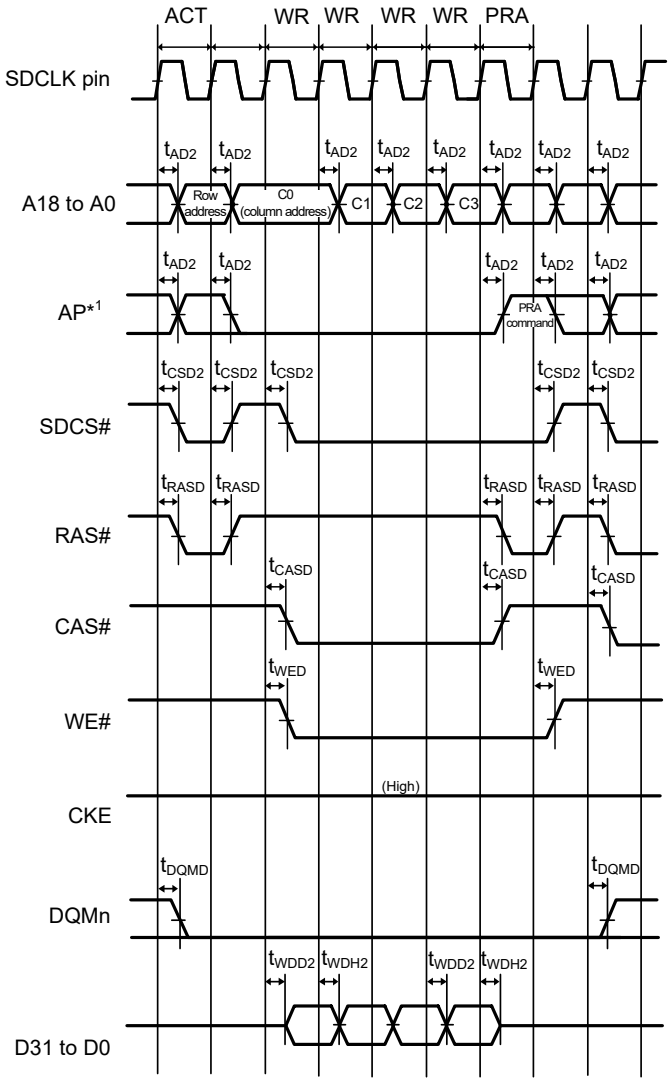


Figure 5.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Write Bus Timing

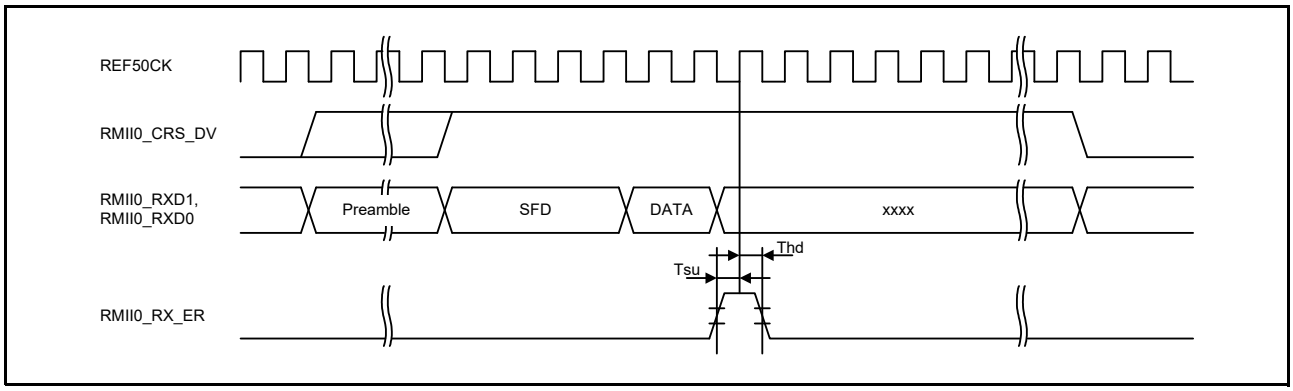


Figure 5.59 RMII Reception Timing (Error Occurrence)

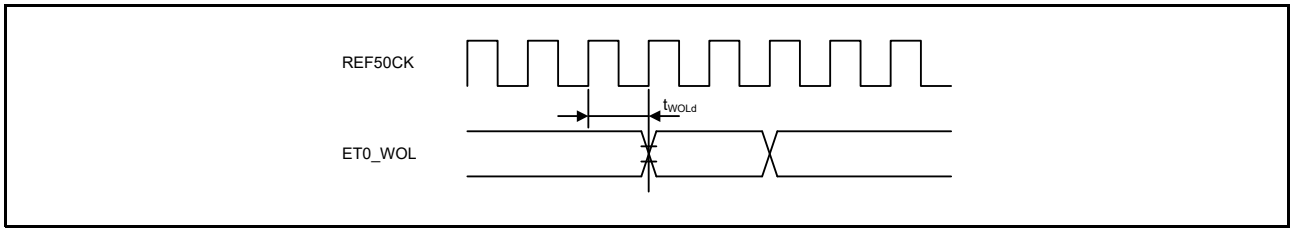


Figure 5.60 WOL Output Timing (RMII)

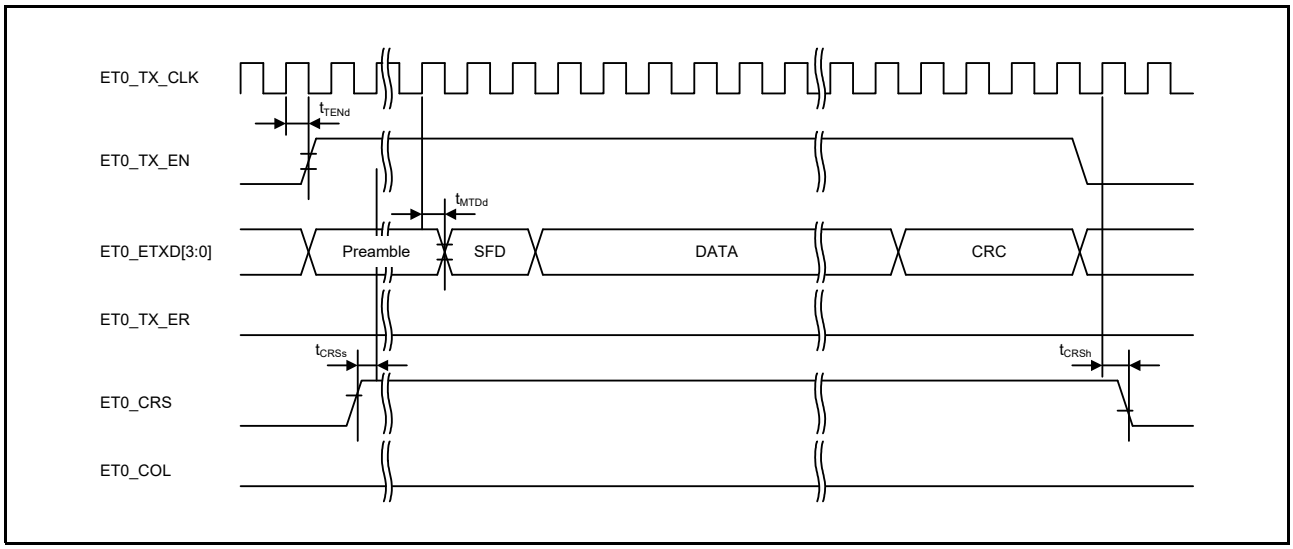


Figure 5.61 MII Transmission Timing (Normal Operation)

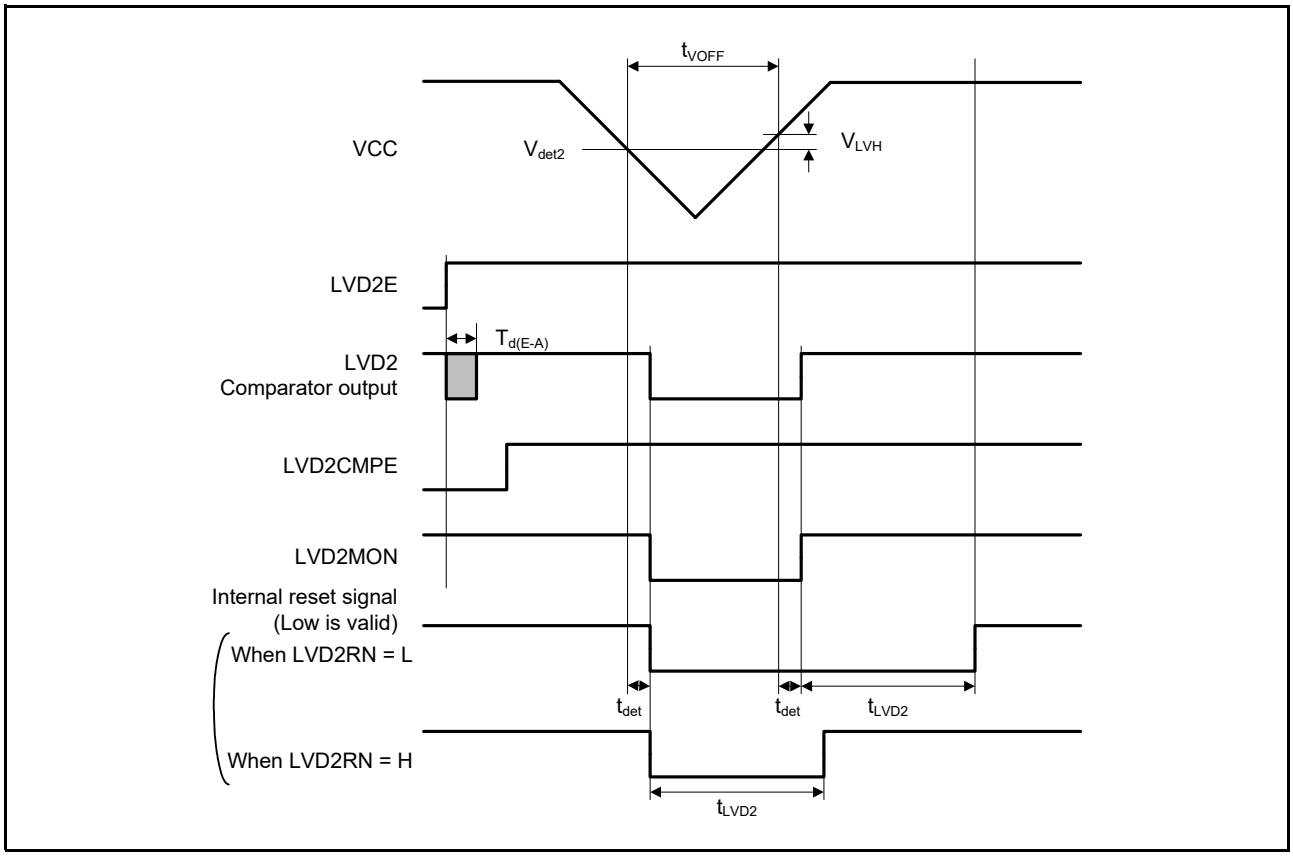


Figure 5.79 Voltage Detection Circuit Timing (V_{det2})

5.9 Oscillation Stop Detection Timing

Table 5.52 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.80

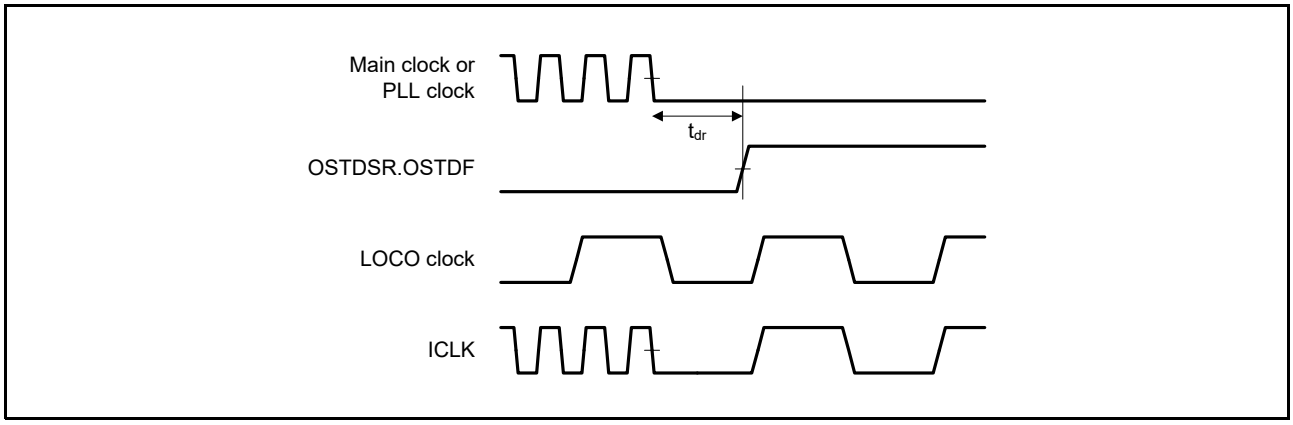
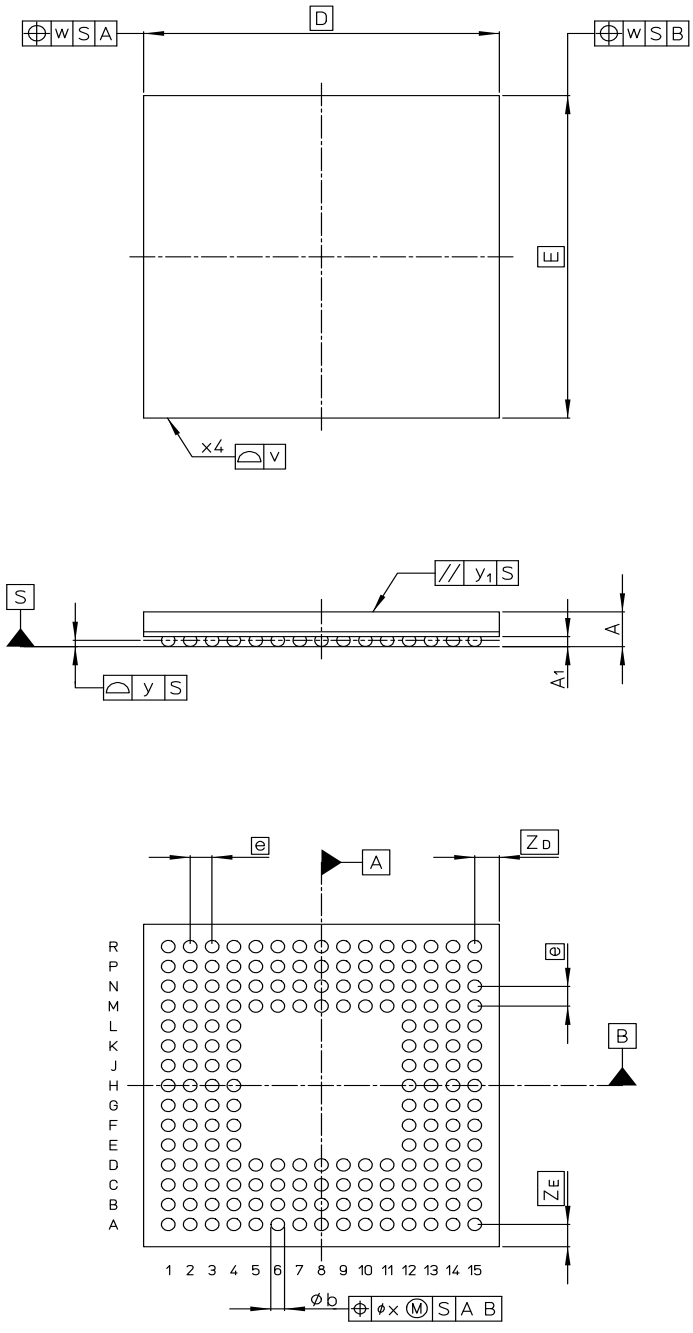


Figure 5.80 Oscillation Stop Detection Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.2
SD	—	—	—
SE	—	—	—
ZD	—	0.90	—
ZE	—	0.90	—

Figure B 176-Pin LFBGA (PLBG0176GA-A)