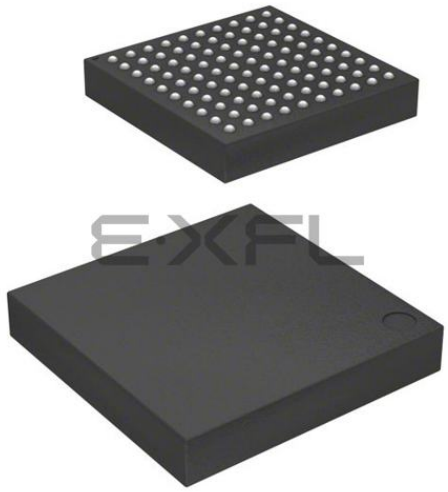
Renesas Electronics America Inc - R5F565N4ADLJ#20 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n4adlj-20

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Timers	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)*4	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
Communication function	Ethernet controller (ETHERC)	• Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a “wake-on-LAN” signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards
	DMA controller for Ethernet controller (EDMACa)	• Alleviation of CPU load by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 FS host/ function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus power are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
A1	AVSS0								
A2	AVCC0								
A3	VREFL0								
A4		P42						IRQ10-DS	AN002
A5		P46						IRQ14-DS	AN006
A6	VCC								
A7	VSS								
A8		P94	D20/A20						
A9	VCC								
A10	TRSYNC1	P97	D23/A23						
A11		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106
A12		P60	CS0#						
A13		P63	CAS#/ D2[A2/D2]/ CS3#						
A14		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B		ANEX1
A15		PE2	D10[A10/ D10]/D2[A2/ D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100
B1		P05						IRQ13	DA1
B2		P07						IRQ15	ADTRG0#
B3		P40						IRQ8-DS	AN000
B4		P41						IRQ9-DS	AN001
B5		P47						IRQ15-DS	AN007
B6		P91	D17/A17		SCK7				AN115
B7		P92	D18/A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B	IRQ1	AN109
B9	TRDATA5	P96	D22/A22						
B10		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
B11	TRDATA7	PG1	D25						
B12	VSS								
B13		P64	WE#/D3[A3/ D3]/CS4#						
B14		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B		ANEX0

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
B15		PE3	D11[A11/D11]/D3[A3/D3]	MTIOC4B/PO26/TOC3/POE8#	ET0_ERXD3/CTS12#/RTS12#/SS12#	MMC_D7-B	LCD_DATA13-B		AN101
C1	AVSS1								
C2	AVCC1								
C3	VREFH0								
C4		P43						IRQ11-DS	AN003
C5		P45						IRQ13-DS	AN005
C6		P90	D16/A16		TXD7/SMOSI7/SSDA7				AN114
C7		PD0	D0[A0/D0]	POE4#			LCD_EXTCLK-B	IRQ0	AN108
C8		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2-B/MMC_D2-B	LCD_DATA22-B	IRQ2	AN110
C9		PD3	D3[A3/D3]	MTIOC8D/TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DATA21-B	IRQ3	AN111
C10	TRDATA6	PG0	D24						
C11	VCC								
C12		P62	RAS#/D1[A1/D1]/CS2#						
C13		PE4	D12[A12/D12]/D4[A4/D4]	MTIOC4D/MTIOC1A/PO28	ET0_ERXD2/SSLB0-B		LCD_DATA12-B		AN102
C14	VSS								
C15		P70	SDCLK						
D1		P01		TMCI0	RXD6/SMISO6/SSCL6			IRQ9	AN119
D2		P02		TMCI1	SCK6			IRQ10	AN120
D3		P03						IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6			IRQ8	AN118
D5		P44						IRQ12-DS	AN004
D6		P93	D19/A19	POE0#	CTS7#/RTS7#/SS7#				AN117
D7	TRDATA4	P95	D21/A21						
D8	VSS								
D9		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/POE10#	SSLC1-A	QSPCLK-B/SDHI_CLK-B/MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3-A	QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B	LCD_DATA17-B	IRQ7	AN107
D11		P61	SDCS#/D0[A0/D0]/CS1#						
D12		PE5	D13[A13/D13]/D5[A5/D5]	MTIOC4C/MTIOC2B	ET0_RX_CLK/REF50CK0/RSPCKB-B		LCD_DATA11-B	IRQ5	AN103
D13	VCC								

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
D14		PE7	D15[A15/D15]/D7[A7/D7]	MTIOC6A/TOC1	MISOB-B	SDHI_WP/MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105
D15		P65	CKE/CS5#						
E1		PJ5		POE8#	CTS2#/RTS2#/SS2#				
E2	EMLE								
E3		PF5						IRQ4	
E4	VSS								
E5 *1	NC								
E12		PE6	D14[A14/D14]/D6[A6/D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/MMC_CD-B	LCD_DATA10-B	IRQ6	AN104
E13	TRDATA0	PG2	D26						
E14	TRDATA1	PG3	D27						
E15		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	VBATT								
F2	VCL								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#				
F4	BSCANP								
F12		P66	DQM0/CS6#	MTIOC7D					
F13	TRSYNC	PG4	D28						
F14		PA0	DQM2/BC0#/A0	MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF	ET0_TX_EN/RMII0_TXD_EN/SSLA1-B		LCD_DATA8-B		
F15	VSS								
G1	XCIN								
G2	XCOUT								
G3	MD/FINED								
G4	TRST#	PF4							
G12	TRCLK	PG5	D29						
G13	TRDATA2	PG6	D30						
G14		PA1	DQM3/A1	MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17	ET0_WOL/SCK5/SSLA2-B		LCD_DATA7-B	IRQ11	
G15	VCC								
H1	XTAL	P37							
H2	VSS								
H3	RES#								
H4	UPSEL	P35						NMI	
H12		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B		LCD_DATA4-B	IRQ5-DS	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (1/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
A1	AVSS0								
A2		P07						IRQ15	ADTRG0#
A3		P40						IRQ8-DS	AN000
A4		P42						IRQ10-DS	AN002
A5		P45						IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7				AN114
A7		P92	A18	POE4#	RXD7/SMISO7/SSCL7				AN116
A8		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2-B/MMC_D2-B	LCD_DATA22-B*1	IRQ2	AN110
A9		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/POE4#	SSLC2-A	QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B	LCD_DATA18-B*1	IRQ6	AN106
A10	VSS								
A11		P62	RAS#/D1[A1/D1]*1/CS2#						
A12		PE1	D9[A9/D9]/D1[A1/D1]*1	MTIOC4C/MTIOC3B/PO18	TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B*1		ANEX1
A13		PE3	D11[A11/D11]/D3[A3/D3]*1	MTIOC4B/PO26/TOC3/POE8#	ET0_ERXD3/CTS12#/RTS12#/SS12#	MMC_D7-B	LCD_DATA13-B*1		AN101
B1	AVCC1								
B2	AVCC0								
B3		P05						IRQ13	DA1
B4	VREFL0								
B5		P43						IRQ11-DS	AN003
B6		P47						IRQ15-DS	AN007
B7		P91	A17		SCK7				AN115
B8		PD0	D0[A0/D0]	POE4#			LCD_EXTCLK-B*1	IRQ0	AN108
B9		PD4	D4[A4/D4]	MTIOC8B/POE11#	SSLC0-A	QSSL-B/SDHI_CMD-B/MMC_CMD-B	LCD_DATA20-B*1	IRQ4	AN112
B10	VCC								
B11		P61	SDCS#/D0[A0/D0]*1/CS1#						
B12		PE2	D10[A10/D10]/D2[A2/D2]*1	MTIOC4A/PO23/TIC3	RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B*1	IRQ7-DS	AN100

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
B13		PE4	D12[A12/D12]/D4[A4/D4]*1	MTIOC4D/MTIOC1A/PO28	ET0_ERXD2/SSLB0-B		LCD_DATA12-B*1		AN102
C1	AVSS1								
C2		P02		TMCI1	SCK6			IRQ10	AN120
C3	VREFH0								
C4		P41						IRQ9-DS	AN001
C5		P46						IRQ14-DS	AN006
C6	VSS								
C7		PD1	D1[A1/D1]	MTIOC4B/POE0#	MOSIC-A/CTX0		LCD_DATA23-B*1	IRQ1	AN109
C8		PD3	D3[A3/D3]	MTIOC8D/TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DATA21-B*1	IRQ3	AN111
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3-A	QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B	LCD_DATA17-B*1	IRQ7	AN107
C10		P63	CAS#/D2[A2/D2]*1/CS3#						
C11		PE0	D8[A8/D8]/D0[A0/D0]*1	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B*1		ANEX0
C12		P70	SDCLK						
C13	VSS								
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6			IRQ8	AN118
D2		PF5						IRQ4	
D3		P03						IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6			IRQ9	AN119
D5	VCC								
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#				AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/POE10#	SSLC1-A	QSPCLK-B/SDHI_CLK-B/MMC_CLK-B	LCD_DATA19-B*1	IRQ5	AN113
D8		P60	CS0#						
D9		P64	WE#/D3[A3/D3]*1/CS4#						
D10		PE7	D15[A15/D15]/D7[A7/D7]*1	MTIOC6A/TOC1	MISOB-B	SDHI_WP/MMC_RES#-B	LCD_DATA9-B*1	IRQ7	AN105
D11	VCC								
D12		PE5	D13[A13/D13]/D5[A5/D5]*1	MTIOC4C/MTIOC2B	ET0_RX_CLK/REF50CK0/RSPCKB-B		LCD_DATA11-B*1	IRQ5	AN103
D13		PE6	D14[A14/D14]/D6[A6/D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/MMC_CD-B	LCD_DATA10-B*1	IRQ6	AN104
E1	VSS								
E2	VCL								
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#				

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
69	TRDATA6	P76	CS6#	PO22	ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11	QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A			
70		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A			
71	TRSYNC1	P75	CS5#	PO20	ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11#	SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A			
72	TRDATA5	P74	A20/CS4#	PO19	ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11#				
73		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
74	VCC								
75		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
76	VSS								
77	TRDATA4	P73	CS3#	PO16	ET0_WOL				
78		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
79		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
80		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CLK-B*1		
81		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B*1		
82		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6	SDSI_D3-B	LCD_TCON1-B*1		
83		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2-B	LCD_TCON2-B*1		
84		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		LCD_TCON3-B*1	IRQ4-DS	
85		P72	A19/CS2#		ET0_MDC				
86		P71	A18/CS1#		ET0_MDIO				

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/5)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
H1	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
H2		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3				ADTRG0#
H3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB			IRQ6	ADTRG0#
H4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS			IRQ5	
H5		P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ CRX1			IRQ10	
H6		P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
H7	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A			IRQ14	
H8		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A			IRQ13	
H9		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
H10		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
J1		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN				
J2		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN			IRQ9	
J3		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS			IRQ7	ADTRG1#
J4		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1#
J5	VSS_USB								

Table 4.1 List of I/O Registers (Address Order) (3 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 1248h	RAM	Expansion RAM Error Address Capture Register	EXRAMECAD	32	32	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK		Buses
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK		Buses
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK		DMACAa
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 201Fh	DMAC0	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 205Fh	DMAC1	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 209Fh	DMAC2	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa

Table 4.1 List of I/O Registers (Address Order) (6 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 2862h	EXDMAC1	EXDMA Peripheral Request Flag Register	EDMPRF	8	8	1, 2 BCLK		EXDMACa
0008 2A00h	EXDMAC	EXDMAC Module Start Register	EDMAST	8	8	1, 2 BCLK		EXDMACa
0008 2BE0h	EXDMAC	Cluster Buffer Register 0	CLSBR0	32	32	1, 2 BCLK		EXDMACa
0008 2BE4h	EXDMAC	Cluster Buffer Register 1	CLSBR1	32	32	1, 2 BCLK		EXDMACa
0008 2BE8h	EXDMAC	Cluster Buffer Register 2	CLSBR2	32	32	1, 2 BCLK		EXDMACa
0008 2BECh	EXDMAC	Cluster Buffer Register 3	CLSBR3	32	32	1, 2 BCLK		EXDMACa
0008 2BF0h	EXDMAC	Cluster Buffer Register 4	CLSBR4	32	32	1, 2 BCLK		EXDMACa
0008 2BF4h	EXDMAC	Cluster Buffer Register 5	CLSBR5	32	32	1, 2 BCLK		EXDMACa
0008 2BF8h	EXDMAC	Cluster Buffer Register 6	CLSBR6	32	32	1, 2 BCLK		EXDMACa
0008 2BFCh	EXDMAC	Cluster Buffer Register 7	CLSBR7	32	32	1, 2 BCLK		EXDMACa
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1, 2 BCLK		Buses
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1, 2 BCLK		Buses
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1, 2 BCLK		Buses
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1, 2 BCLK		Buses
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1, 2 BCLK		Buses
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1, 2 BCLK		Buses
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK		Buses
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK		Buses
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK		Buses
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK		Buses
0008 3042h	BSC	CS4 Mode Register	CS4MOD	16	16	1, 2 BCLK		Buses
0008 3044h	BSC	CS4 Wait Control Register 1	CS4WCR1	32	32	1, 2 BCLK		Buses
0008 3048h	BSC	CS4 Wait Control Register 2	CS4WCR2	32	32	1, 2 BCLK		Buses
0008 3052h	BSC	CS5 Mode Register	CS5MOD	16	16	1, 2 BCLK		Buses
0008 3054h	BSC	CS5 Wait Control Register 1	CS5WCR1	32	32	1, 2 BCLK		Buses
0008 3058h	BSC	CS5 Wait Control Register 2	CS5WCR2	32	32	1, 2 BCLK		Buses
0008 3062h	BSC	CS6 Mode Register	CS6MOD	16	16	1, 2 BCLK		Buses
0008 3064h	BSC	CS6 Wait Control Register 1	CS6WCR1	32	32	1, 2 BCLK		Buses
0008 3068h	BSC	CS6 Wait Control Register 2	CS6WCR2	32	32	1, 2 BCLK		Buses
0008 3072h	BSC	CS7 Mode Register	CS7MOD	16	16	1, 2 BCLK		Buses
0008 3074h	BSC	CS7 Wait Control Register 1	CS7WCR1	32	32	1, 2 BCLK		Buses
0008 3078h	BSC	CS7 Wait Control Register 2	CS7WCR2	32	32	1, 2 BCLK		Buses
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK		Buses
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK		Buses
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK		Buses
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK		Buses
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK		Buses
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK		Buses
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK		Buses
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK		Buses
0008 3842h	BSC	CS4 Control Register	CS4CR	16	16	1, 2 BCLK		Buses
0008 384Ah	BSC	CS4 Recovery Cycle Register	CS4REC	16	16	1, 2 BCLK		Buses

Table 4.1 List of I/O Registers (Address Order) (8 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK		ICUB
0008 72E1h	ICU	Software Interrupt 2 Generation Register	SWINT2R	8	8	2 ICLK		ICUB
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK		ICUB
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Registers 000 to 255	IPR000 to IPR255	8	8	2 ICLK		ICUB
0008 7400h	ICU	DMAC Trigger Select Register 0	DMRSR0	8	8	2 ICLK		ICUB
0008 7404h	ICU	DMAC Trigger Select Register 1	DMRSR1	8	8	2 ICLK		ICUB
0008 7408h	ICU	DMAC Trigger Select Register 2	DMRSR2	8	8	2 ICLK		ICUB
0008 740Ch	ICU	DMAC Trigger Select Register 3	DMRSR3	8	8	2 ICLK		ICUB
0008 7410h	ICU	DMAC Trigger Select Register 4	DMRSR4	8	8	2 ICLK		ICUB
0008 7414h	ICU	DMAC Trigger Select Register 5	DMRSR5	8	8	2 ICLK		ICUB
0008 7418h	ICU	DMAC Trigger Select Register 6	DMRSR6	8	8	2 ICLK		ICUB
0008 741Ch	ICU	DMAC Trigger Select Register 7	DMRSR7	8	8	2 ICLK		ICUB
0008 7500h to 0008 750Fh	ICU	IRQ Control Registers 0 to 15	IRQCR0 to 15	8	8	2 ICLK		ICUB
0008 7520h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUB
0008 7521h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK		ICUB
0008 7528h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK		ICUB
0008 752Ah	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK		ICUB
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK		ICUB
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK		ICUB
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK		ICUB
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK		ICUB
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK		ICUB
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK		ICUB
0008 7600h	ICU	Group BE0 Interrupt Request Register	GRPBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7630h	ICU	Group BL0 Interrupt Request Register	GRPBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7634h	ICU	Group BL1 Interrupt Request Register	GRPBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7638h	ICU	Group BL2 Interrupt Request Register	GRPBL2	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7640h	ICU	Group BE0 Interrupt Request Enable Register	GENBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7670h	ICU	Group BL0 Interrupt Request Enable Register	GENBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7674h	ICU	Group BL1 Interrupt Request Enable Register	GENBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7678h	ICU	Group BL2 Interrupt Request Enable Register	GENBL2	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7680h	ICU	Group BE0 Interrupt Clear Register	GCRBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7700h	ICU	Software Configurable Interrupt B Request Register 0	PIBR0	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7701h	ICU	Software Configurable Interrupt B Request Register 1	PIBR1	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7702h	ICU	Software Configurable Interrupt B Request Register 2	PIBR2	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7703h	ICU	Software Configurable Interrupt B Request Register 3	PIBR3	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7704h	ICU	Software Configurable Interrupt B Request Register 4	PIBR4	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7705h	ICU	Software Configurable Interrupt B Request Register 5	PIBR5	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7706h	ICU	Software Configurable Interrupt B Request Register 6	PIBR6	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7707h	ICU	Software Configurable Interrupt B Request Register 7	PIBR7	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7708h	ICU	Software Configurable Interrupt B Request Register 8	PIBR8	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (46 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 4204h	CMTW0	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4208h	CMTW0	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4210h	CMTW0	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4214h	CMTW0	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4218h	CMTW0	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 421Ch	CMTW0	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4220h	CMTW0	Output Compare Register 0	CMWOCR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4224h	CMTW0	Output Compare Register 1	CMWOCR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4280h	CMTW1	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4284h	CMTW1	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4288h	CMTW1	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4290h	CMTW1	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4294h	CMTW1	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4298h	CMTW1	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 429Ch	CMTW1	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 42A0h	CMTW1	Output Compare Register 0	CMWOCR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 42A4h	CMTW1	Output Compare Register 1	CMWOCR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 5000h	SDSI	FN1 Access Control Register	FN1ACCR	32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI
0009 5004h	SDSI	Interrupt Enable Control Register 1	INTENCR1	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 5005h	SDSI	Interrupt Status Register 1	INTSR1	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 5006h	SDSI	SD Command Control Register	SDCMDCR	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 5007h	SDSI	SD Command Access Address 0 Register	SDCADD0R	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 5008h	SDSI	SD Command Access Address 1 Register	SDCADD1R	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 5009h	SDSI	SD Command Access Address 2 Register	SDCADD2R	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 500Ah	SDSI	SDSI Control Register 1	SDSICR1	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 500Bh	SDSI	DMA Control Register 1	DMACR1	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 500Ch	SDSI	Block Counter	BLKCNT	16	16	8, 9 PCLKB	2 to 5 ICLK	SDSI
0009 500Eh	SDSI	Byte Counter	BYTCNT	16	16	8, 9 PCLKB	2 to 5 ICLK	SDSI
0009 5010h	SDSI	DMA Transfer Address Register	DMATRADDR	32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI
0009 5100h	SDSI	SDSI Control Register 2	SDSICR2	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5104h	SDSI	SDSI Control Register 3	SDSICR3	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5108h	SDSI	Interrupt Enable Control Register 2	INTENCR2	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 510Ch	SDSI	Interrupt Status Register 2	INTSR2	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5110h	SDSI	DMA Control Register 2	DMACR2	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5200h to 0009 526Bh	SDSI	CIS Data Register 0 to 26	CISDATAR0 to 26	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5270h	SDSI	FBR Setting Register 1	FBR1	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5274h	SDSI	FBR Setting Register 2	FBR2	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5278h	SDSI	FBR Setting Register 3	FBR3	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 527Ch	SDSI	FBR Setting Register 4	FBR4	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5280h	SDSI	FBR Setting Register 5	FBR5	32	32	2, 3 PCLKB	2 ICLK	SDSI
0009 5800h to 0009 58FFh	SDSI	FN1 Data Register 10 to 163	FN1DATAR10 to 163	8, 32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI
0009 5900h to 0009 59FFh	SDSI	FN1 Data Register 20 to 263	FN1DATAR20 to 263	8, 32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI
0009 5A00h to 0009 5AFFh	SDSI	FN1 Data Register 30 to 363	FN1DATAR30 to 363	8, 32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI
0009 5B00h	SDSI	FN1 Interrupt Vector Register	FN1INTVECR	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 5B01h	SDSI	FN1 Interrupt Clear Register	FN1INTCLRR	8	8	7, 8 PCLKB	2 to 5 ICLK	SDSI
0009 5C00h to 0009 5FFFh	SDSI	FN1 Data Register 50 to 5255	FN1DATAR50 to 5255	8, 32	32	7, 8 PCLKB	2 to 5 ICLK	SDSI

Table 4.1 List of I/O Registers (Address Order) (47 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 004Eh	USB0	Device State Change Register	DVCHGR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb

Table 4.1 List of I/O Registers (Address Order) (50 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0078h	EDMAC 0	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 007Ch	EDMAC 0	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00C8h	EDMAC 0	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00CCh	EDMAC 0	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00D4h	EDMAC 0	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 00D8h	EDMAC 0	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0100h	ETHER C0	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0108h	ETHER C0	Receive Frame Maximum Length Register	RFLR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0110h	ETHER C0	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0118h	ETHER C0	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0120h	ETHER C0	PHY Interface Register	PIR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0128h	ETHER C0	PHY Status Register	PSR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0140h	ETHER C0	Random Number Generation Counter Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0150h	ETHER C0	Interpacket Gap Register	IPGR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0154h	ETHER C0	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0158h	ETHER C0	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0160h	ETHER C0	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0164h	ETHER C0	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 0168h	ETHER C0	PAUSE Frame Retransmit Counter	TPAUSECR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 016Ch	ETHER C0	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01C0h	ETHER C0	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01C8h	ETHER C0	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01D0h	ETHER C0	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01D4h	ETHER C0	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01D8h	ETHER C0	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01DCh	ETHER C0	Carrier Not Detect Counter Register	CNDCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01E4h	ETHER C0	CRC Error Frame Receive Counter Register	CEFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01E8h	ETHER C0	Frame Receive Error Counter Register	FRECR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01ECh	ETHER C0	Too-Short Frame Receive Counter Register	TSFRCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01F0h	ETHER C0	Too-Long Frame Receive Counter Register	TLFRCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 01F4h	ETHER C0	Received Alignment Error Frame Counter Register	RFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C

Table 4.1 List of I/O Registers (Address Order) (51 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 01F8h	ETHERC0	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 1200h	MTU3	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ch	MTU3	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1231h	MTU	Timer Interrupt Skipping Counter 1A	TITCNT1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ch	MTU	Timer Interrupt Skipping Counter 2A	TITCNT2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (58 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 0400h to 000E 07FCh	GLCDC	Graphic 1 Color Look-up Table 1[0 to 255]	GR1CLUT1[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 0800h to 000E 0BFCh	GLCDC	Graphic 2 Color Look-up Table 0[0 to 255]	GR2CLUT0[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 0C00h to 000E 0FFCh	GLCDC	Graphic 2 Color Look-up Table 1[0 to 255]	GR2CLUT1[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC
000E 1000h	GLCDC	Background Generating Block Operation Control Register	BGEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1004h	GLCDC	Free-Running Period Register	BGPERI	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1008h	GLCDC	Synchronization Position Register	BGSYNC	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 100Ch	GLCDC	Vertical Size Register	BGVSIZE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1010h	GLCDC	Horizontal Size Register	BGHSIZE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1014h	GLCDC	Background Color Register	BGCOLOR	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1018h	GLCDC	Background Generating Block Status Monitor Register	BGMON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1100h	GLCDC	Graphic 1 Register Update Control Register	GR1VEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1104h	GLCDC	Graphic 1 Frame Buffer Read Control Register	GR1FLMRD	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 110Ch	GLCDC	Graphic 1 Frame Buffer Control Register 2	GR1FLM2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1110h	GLCDC	Graphic 1 Frame Buffer Control Register 3	GR1FLM3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1118h	GLCDC	Graphic 1 Frame Buffer Control Register 5	GR1FLM5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 111Ch	GLCDC	Graphic 1 Frame Buffer Control Register 6	GR1FLM6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1120h	GLCDC	Graphic 1 Alpha Blending Control Register 1	GR1AB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1124h	GLCDC	Graphic 1 Alpha Blending Control Register 2	GR1AB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1128h	GLCDC	Graphic 1 Alpha Blending Control Register 3	GR1AB3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 112Ch	GLCDC	Graphic 1 Alpha Blending Control Register 4	GR1AB4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1130h	GLCDC	Graphic 1 Alpha Blending Control Register 5	GR1AB5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1134h	GLCDC	Graphic 1 Alpha Blending Control Register 6	GR1AB6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1138h	GLCDC	Graphic 1 Alpha Blending Control Register 7	GR1AB7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 113Ch	GLCDC	Graphic 1 Alpha Blending Control Register 8	GR1AB8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1140h	GLCDC	Graphic 1 Alpha Blending Control Register 9	GR1AB9	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 114Ch	GLCDC	Graphic 1 Background Color Control Register	GR1BASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1150h	GLCDC	Graphic 1 CLUT/Interrupt Control Register	GR1CLUTINT	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1154h	GLCDC	Graphic 1 Status Monitor Register	GR1MON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1200h	GLCDC	Graphic 2 Register Update Control Register	GR2VEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1204h	GLCDC	Graphic 2 Frame Buffer Read Control Register	GR2FLMRD	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 120Ch	GLCDC	Graphic 2 Frame Buffer Control Register 2	GR2FLM2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1210h	GLCDC	Graphic 2 Frame Buffer Control Register 3	GR2FLM3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1218h	GLCDC	Graphic 2 Frame Buffer Control Register 5	GR2FLM5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 121Ch	GLCDC	Graphic 2 Frame Buffer Control Register 6	GR2FLM6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1220h	GLCDC	Graphic 2 Alpha Blending Control Register 1	GR2AB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1224h	GLCDC	Graphic 2 Alpha Blending Control Register 2	GR2AB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1228h	GLCDC	Graphic 2 Alpha Blending Control Register 3	GR2AB3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 122Ch	GLCDC	Graphic 2 Alpha Blending Control Register 4	GR2AB4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1230h	GLCDC	Graphic 2 Alpha Blending Control Register 5	GR2AB5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1234h	GLCDC	Graphic 2 Alpha Blending Control Register 6	GR2AB6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1238h	GLCDC	Graphic 2 Alpha Blending Control Register 7	GR2AB7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 123Ch	GLCDC	Graphic 2 Alpha Blending Control Register 8	GR2AB8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1240h	GLCDC	Graphic 2 Alpha Blending Control Register 9	GR2AB9	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 124Ch	GLCDC	Graphic 2 Background Color Control Register	GR2BASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1250h	GLCDC	Graphic 2 CLUT/Interrupt Control Register	GR2CLUTINT	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1254h	GLCDC	Graphic 2 Status Monitor Register	GR2MON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC

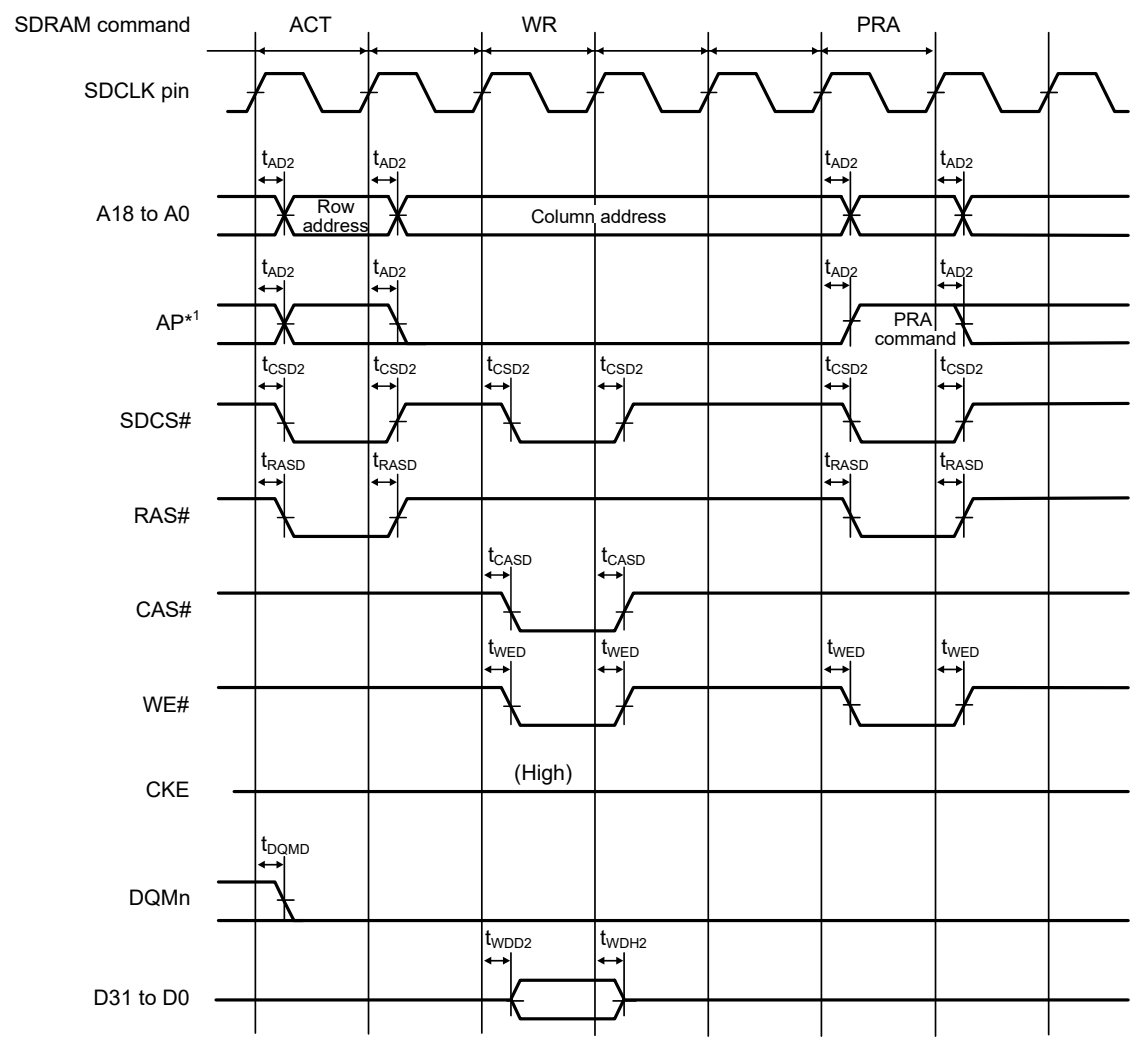
5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.21 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time after cancellation of software standby mode*1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bit × 32) + 76} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{MAIN}	µs	Figure 5.12
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			{(MSTS[7:0] bit × 32) + 138} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Sub-clock oscillator operating		t_{SBYSC}			{(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10 / f_{FCLK}	100 + 4 / f_{ICLK} + 2n / f_{SUE}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	100 + 7 / f_{ICLK} + 2n / f_{HOCO}		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	100 + 7 / f_{ICLK} + 2n / f_{LOCO}		

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when f_{ICLK}:f_{FCLK} = 1:1, 2:1, or 4:1.



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.24 SDRAM Space Single Write Bus Timing

Table 5.37 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions*2
QSPI	QSPCLK clock cycle	t_{QScyc}	2	4080	t_{PBcyc}	Figure 5.51
	Data input setup time*3	t_{Su}	6.5	—	ns	Figure 5.52, Figure 5.53
	Data input hold time	t_{IH}	5	—	ns	
	SS setup time	t_{LEAD}	1.5	8.5	t_{QScyc}	
	SS hold time	t_{LAG}	1	8	t_{QScyc}	
	Data output delay time	t_{OD}	—	10.0	ns	
	Data output hold time	t_{OH}	–5	—	ns	
	Successive transmission delay time	t_{TD}	1	8	t_{QScyc}	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the QSPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. For version G products (+85 < Ta ≤ +105°C), the high-drive ability control register of the QSPCLK pin measures this data input setup time with the high-speed interface high-drive output selected.

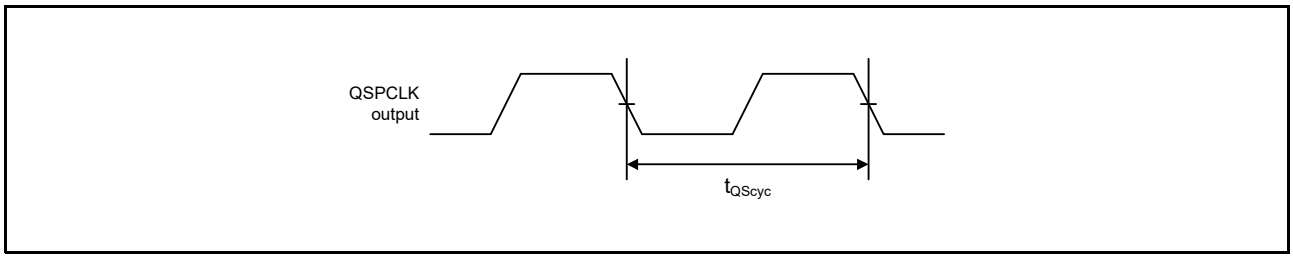


Figure 5.51 QSPI Clock Timing

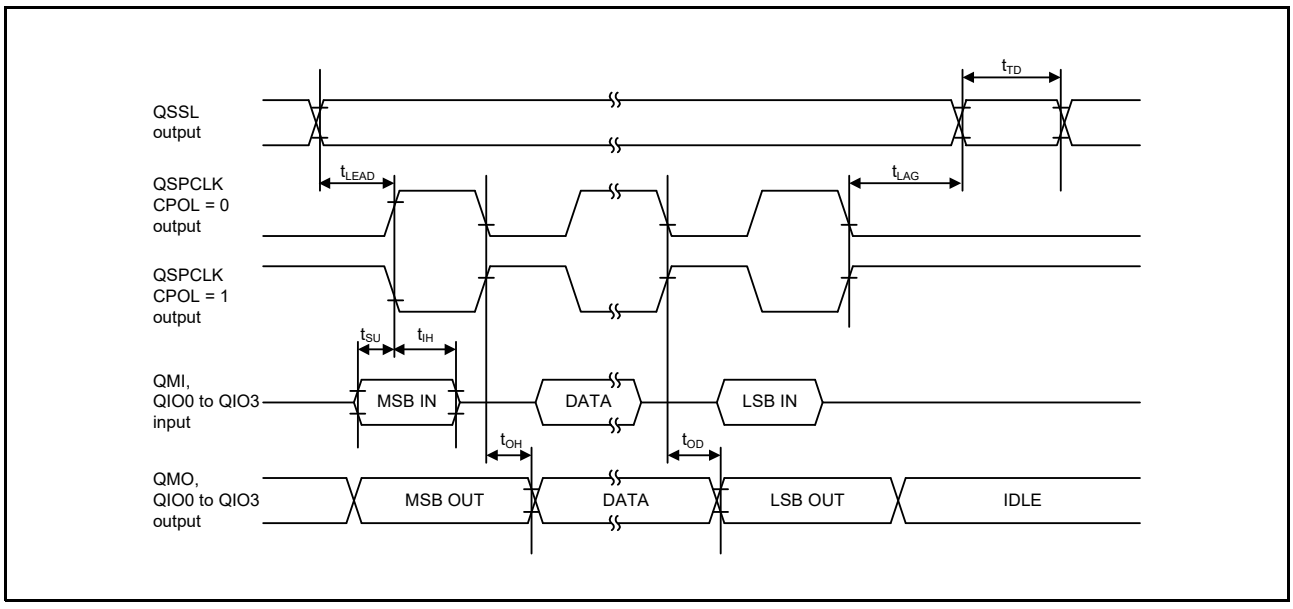


Figure 5.52 Transmit/Receive Timing (CPHA = 0)

Table 5.42 PDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	—	ns	Figure 5.66
	PIXCLK input high pulse width	t_{PIXH}	10	—	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	—	ns	
	PIXCLK rising time	t_{PIXr}	—	5	ns	
	PIXCLK falling time	t_{PIXf}	—	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	—	ns	Figure 5.67
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO rising time	t_{PCKr}	—	5	ns	
	PCKO falling time	t_{PCKf}	—	5	ns	
	VSYNC/HSYNC input setup time	t_{SYNCS}	10	—	ns	Figure 5.68
	VSYNC/HSYNC input hold time	t_{SYNCH}	5	—	ns	
	PIXD input setup time	t_{PIXDS}	10	—	ns	
	PIXD input hold time	t_{PIXDH}	5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

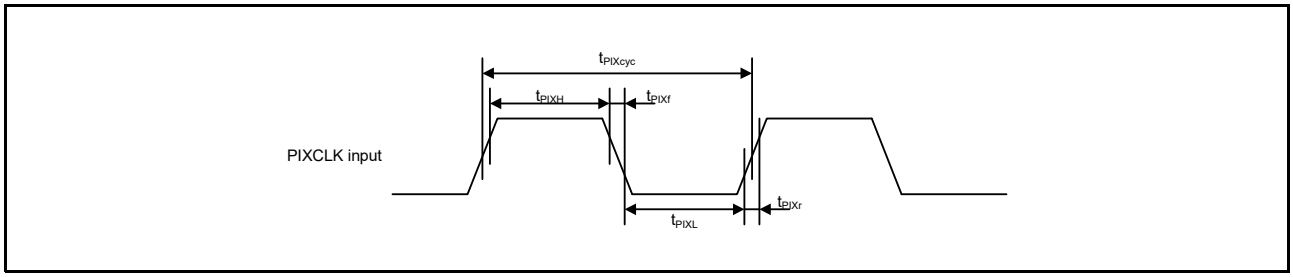


Figure 5.66 PDC Input Clock Timing

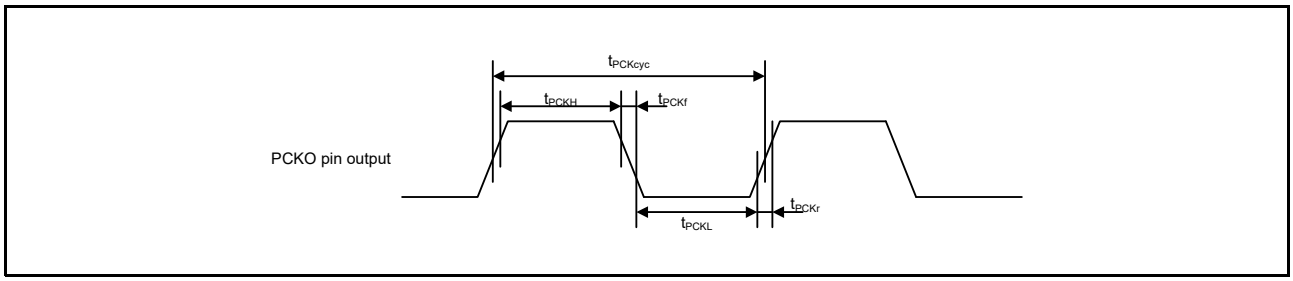


Figure 5.67 PDC Output Clock Timing