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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n4bdfp-30

Table 1.1 Outline of Specifications (6/9)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIg, SCIlh, SCLi)	13 channels (SCIg: 10 channels + SCIlh: 1 channel + SCLi: 2 channels) - SCIg, SCIlh, SCLi Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Start-bit detection: Level or edge detection is selectable. Simple I²C Simple SPI 9-bit transfer mode Bit rate modulation Double-speed mode - SCIg, SCIlh Average transfer rate clock can be input from TMR timers for SCIl5, SCIl6, and SCIl12 Event linking by the ELC (only on channel 5) - SCIlh Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format - SCLi Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit
	I ² C bus interface (RIICa)	3 channels (only channel 0 can be used in fast-mode plus) Communication formats I²C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) - Event linking by the ELC
	CAN module (CAN)	2 channels - Compliance with the ISO11898-1 specification (standard frame and extended frame) 32 mailboxes per channel
	Serial peripheral interface (RSPIC)	3 channels RSPIC transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPIC clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave - Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transit/receive data can be swapped in byte units - Buffered structure Double buffers for both transmission and reception - RSPCK can be stopped with the receive buffer full for master reception. - Event linking by the ELC
	Quad serial peripheral interface (QSPI)	1 channel - Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) - Programmable bit length and selectable active sense and phase of the clock signal - Sequential execution of transfer - LSB or MSB first is selectable

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock
	SSDA12	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RDX12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	RXD10 and RXD11	Input	Input pin for received data
	TXD10 and TXD11	Output	Output pin for transmitted data
	CTS10# and CTS11#	Input	Input pin for controlling the start of transmission and reception
	RTS10# and RTS11#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL10 and SSCL11	I/O	Input/output pin for the I ² C clock
	SSDA10 and SSDA11	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	SMISO10 and SMISO11	I/O	Input/output pin for slave transmission of data
	SMOSI10 and SMOSI11	I/O	Input/output pin for master transmission of data
	SS10# and SS11#	Input	Chip-select input pin
I ² C bus interface	SCL0[FM+], SCL1, SCL2, SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1, SDA2, SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (8/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
R9		P53*2	BCLK						
R10	VSS								
R11	VCC								
R12		P80	EDREQ0	MTIOC3B/ PO26	ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10#	QIO2-A/SDHI_WP/ MMC_D2-A	LCD_DA TA14-A		
R13		P76	CS6#	PO22	ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11	QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A	LCD_DA TA18-A		
R14		P74	A20/CS4#	PO19	ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11#		LCD_DA TA21-A		
R15		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A		LCD_DA TA22-A	IRQ12	

Note 1. The 176-pin LFBGA does not include the E5 pin.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (2/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
32		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
33		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
34	TCK	PF1			SCK1				
35	TDO	PF0			TXD1/SMOSI1/ SSDA1				
36		P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB- A				
37		P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
38		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0 #
39	VCC								
40		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
41	VSS								
42		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C/PIXD7			
43		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C/PIXD6			
44		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN	SDHI_CLK-C/ PIXD5		IRQ9	
45		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID	SDHI_CMD-C/ PIXD4		IRQ8	
46		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C/PIXD3		IRQ7	ADTRG1 #
47		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C/PIXD2			
48		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
49		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
50		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (5/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
K7		P51	WR1#/BC1#/WAIT#		SCK2/SSLB2-A				
K8	VCC								
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10#	QIO2-A/SDHI_WP/ MMC_D2-A			
K10	TRDATA6	P76	CS6#	PO22	ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11	QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A			
K11		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
K12		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
K13		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CL K-B*1		
L1		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0 #
L2		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#SS0#	SDHI_D1-C/PIXD7			
L3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOU	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
L4		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
L5		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1 #
L6		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7*1				
L7		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
L8	TRCLK	P83	EDACK1	MTIOC4C	ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10#				
L9		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A	MMC_D5-A			
L10		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMC11/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#SS8#/ SS10#CTS10#/ RTS10#SSLA0-A	QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A			

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (7/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
N7	TRDATA3	P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7*1/ SMOSI7*1/ SSDA7*1/CRX1			IRQ10	
N8	VSS								
N9	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A	MMC_D7-A		IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10	MMC_D4-A			
N11		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5	QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A			
N12	TRSYNC1	P75	CS5#	PO20	ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11#	SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A			
N13	TRDATA5	P74	A20/CS4#	PO19	ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11#				

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 4.1 List of I/O Registers (Address Order) (2 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0036h	SYSTM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK		Clock Generation Circuit
0008 0037h	SYSTM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK		Clock Generation Circuit
0008 003Ch	SYSTM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK		Clock Generation Circuit
0008 0040h	SYSTM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK		Clock Generation Circuit
0008 0041h	SYSTM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK		Clock Generation Circuit
0008 00A0h	SYSTM	Operating Power Control Register	OPCCR	8	8	3 ICLK		Low Power Consumption
0008 00A1h	SYSTM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK		Low Power Consumption
0008 00A2h	SYSTM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00A3h	SYSTM	Sub-Clock Oscillator Wait Control Register	SOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00C0h	SYSTM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets
0008 00C2h	SYSTM	Software Reset Register	SWRR	16	16	3 ICLK		Resets
0008 00E0h	SYSTM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA
0008 00E1h	SYSTM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK		LVDA
0008 00E2h	SYSTM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK		LVDA
0008 00E3h	SYSTM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK		LVDA
0008 03FEh	SYSTM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	2 ICLK		Flash
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	2 ICLK		Flash
0008 101Ch	SYSTM	ROM Wait Cycle Setting Register	ROMWT	8	8	2 ICLK		Clock Generation Circuit
0008 1200h	RAM	RAM Operating Mode Control Register	RAMMODE	8	8	2 ICLK		RAM
0008 1201h	RAM	RAM Error Status Register	RAMSTS	8	8	2 ICLK		RAM
0008 1204h	RAM	RAM Protection Register	RAMPRCR	8	8	2 ICLK		RAM
0008 1208h	RAM	RAM Error Address Capture Register	RAMECAD	32	32	2 ICLK		RAM
0008 1240h	RAM	Expansion RAM Operating Mode Control Register	EXRAMMODE	8	8	2 ICLK		RAM
0008 1241h	RAM	Expansion RAM Error Status Register	EXRAMSTS	8	8	2 ICLK		RAM
0008 1244h	RAM	Expansion RAM Protection Register	EXRAMPRCR	8	8	2 ICLK		RAM

Table 4.1 List of I/O Registers (Address Order) (4 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 20DFh	DMAC3	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2100h	DMAC4	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2104h	DMAC4	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2108h	DMAC4	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 211Fh	DMAC4	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 215Fh	DMAC5	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 219Fh	DMAC6	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 21DCh	DMAC7	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 21DDh	DMAC7	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 21DEh	DMAC7	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 21DFh	DMAC7	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2200h	DMAC	DMAC Module Start Register	DMAST	8	8	2	ICLK	DMACaA
0008 2204h	DMAC	DMAC74 Interrupt Status Monitor Register	DMIST	8	8	2	ICLK	DMACaA
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2	ICLK	DTCb
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2	ICLK	DTCb
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2	ICLK	DTCb

Table 4.1 List of I/O Registers (Address Order) (19 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9084h	S12AD	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 908Ch	S12AD	A/D Comparison Function Window A/B Status Monitoring Register	ADWINMON	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9090h	S12AD	A/D Comparison Function Control Register	ADCMPCR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9094h	S12AD	A/D Comparison Function Window A Channel Select Register 0	ADCMPSNR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9098h	S12AD	A/D Comparison Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 909Ch	S12AD	A/D Comparison Function Window A Lower Level Setting Register	ADCMPDR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 909Eh	S12AD	A/D Comparison Function Window A Upper Level Setting Register	ADCMPDR1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90A0h	S12AD	A/D Comparison Function Window A Channel Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90A6h	S12AD	A/D Comparison Function Window B Channel Select Register	ADCMPBNSR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90A8h	S12AD	A/D Comparison Function Window B Lower Level Setting Register	ADWINLLB	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90AAh	S12AD	A/D Comparison Function Window B Upper Level Setting Register	ADWINULB	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90ACh	S12AD	A/D Comparison Function Window B Channel Status Register	ADCMPBSR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90D4h	S12AD	A/D Channel Select Register C0	ADANSC0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90D9h	S12AD	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9100h	S12AD1	A/D Control Register	ADCSR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9104h	S12AD1	A/D Channel Select Register A0	ADANSA0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9106h	S12AD1	A/D Channel Select Register A1	ADANSA1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9108h	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 910Ah	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 910Ch	S12AD1	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 910Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa

Table 4.1 List of I/O Registers (Address Order) (26 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A068h	SCI3	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A069h	SCI3	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A06Ah	SCI3	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A06Bh	SCI3	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A06Ch	SCI3	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A06Dh	SCI3	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A06Eh	SCI3	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A06Fh	SCI3	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A06Eh	SCI3	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A070h	SCI3	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A071h	SCI3	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A070h	SCI3	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A072h	SCI3	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A080h	SCI4	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A081h	SCI4	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A082h	SCI4	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A083h	SCI4	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A084h	SCI4	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A085h	SCI4	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A086h	SMCI4	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A087h	SCI4	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A088h	SCI4	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A089h	SCI4	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i

Table 4.1 List of I/O Registers (Address Order) (27 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A08Ah	SCI4	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A08Bh	SCI4	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A08Ch	SCI4	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A091h	SCI4	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A090h	SCI4	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A092h	SCI4	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0A9h	SCI5	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0AAh	SCI5	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A0ABh	SCI5	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli

Table 4.1 List of I/O Registers (Address Order) (28 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (47 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 004Eh	USB0	Device State Change Register	DVCHGR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb

Table 4.1 List of I/O Registers (Address Order) (50 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0078h	EDMAC0	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMACa
000C 007Ch	EDMAC0	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMACa
000C 00C8h	EDMAC0	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMACa
000C 00CCh	EDMAC0	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMACa
000C 00D4h	EDMAC0	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMACa
000C 00D8h	EDMAC0	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMACa
000C 0100h	ETHERC0	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0108h	ETHERC0	Receive Frame Maximum Length Register	RFLR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0110h	ETHERC0	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0118h	ETHERC0	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0120h	ETHERC0	PHY Interface Register	PIR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0128h	ETHERC0	PHY Status Register	PSR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0140h	ETHERC0	Random Number Generation Counter Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0150h	ETHERC0	Interpacket Gap Register	IPGR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0154h	ETHERC0	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0158h	ETHERC0	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0160h	ETHERC0	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0164h	ETHERC0	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 0168h	ETHERC0	PAUSE Frame Retransmit Counter	TPAUSECR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 016Ch	ETHERC0	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01C0h	ETHERC0	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01C8h	ETHERC0	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01D0h	ETHERC0	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01D4h	ETHERC0	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01D8h	ETHERC0	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01DCh	ETHERC0	Carrier Not Detect Counter Register	CNDCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01E4h	ETHERC0	CRC Error Frame Receive Counter Register	CEFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01E8h	ETHERC0	Frame Receive Error Counter Register	FRECR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01ECh	ETHERC0	Too-Short Frame Receive Counter Register	TSFRRCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01F0h	ETHERC0	Too-Long Frame Receive Counter Register	TLFRRCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC
000C 01F4h	ETHERC0	Received Alignment Error Frame Counter Register	RFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHERC

Table 4.1 List of I/O Registers (Address Order) (56 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 006Ch	SCI11	I ² C Status Register	SISR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Dh	SCI11	SPI Mode Register	SPMR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Eh	SCI11	Transmit Data Register H	TDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Fh	SCI11	Transmit Data Register L	TDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Eh	SCI11	Transmit Data Register HL	TDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 006Eh	SCI11	Transmit FIFO Data Register	FTDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Fh	SCI11	Transmit FIFO Data Register	FTDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 006Eh	SCI11	Transmit FIFO Data Register	FTDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0070h	SCI11	Receive Data Register H	RDRH	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0071h	SCI11	Receive Data Register L	RDRL	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0070h	SCI11	Receive Data Register HL	RDRHL	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0070h	SCI11	Receive FIFO Data Register	FRDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0071h	SCI11	Receive FIFO Data Register	FRDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0070h	SCI11	Receive FIFO Data Register	FRDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0072h	SCI11	Modulation Duty Register	MDDR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0073h	SCI11	Data Comparison Control Register	DCCR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0074h	SCI11	FIFO Control Register	FCR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0075h	SCI11	FIFO Control Register	FCR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0074h	SCI11	FIFO Control Register	FCR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0076h	SCI11	FIFO Data Count Register	FDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0077h	SCI11	FIFO Data Count Register	FDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0076h	SCI11	FIFO Data Count Register	FDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 0078h	SCI11	Line Status Register	LSR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0079h	SCI11	Line Status Register	LSR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0078h	SCI11	Line Status Register	LSR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 007Ah	SCI11	Comparison Data Register	CDR.H	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 007Bh	SCI11	Comparison Data Register	CDR.L	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 007Ah	SCI11	Comparison Data Register	CDR	16	16	5, 6 PCLKA	1 to 3 ICLK	SCli
000D 007Ch	SCI11	Serial Port Register	SPTR	8	8	3, 4 PCLKA	1, 2 ICLK	SCli
000D 0100h	RSPI0	RSPI Control Register	SPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0101h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0102h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0103h	RSPI0	RSPI Status Register	SPSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0104h	RSPI0	RSPI Data Register	SPDR	32	8, 16, 32	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0108h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0109h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 010Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0110h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0112h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0114h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0116h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0118h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 011Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 011Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	−0.3 to +4.0	V
V _{BATT} power supply voltage		V _{BATT}	−0.3 to +4.0	V
Input voltage (except for ports for 5 V tolerant*1)		V _{in}	−0.3 to VCC + 0.3 (up to 4.0)	V
Input voltage (ports for 5 V tolerant*1)		V _{in}	−0.3 to VCC + 4.0 (up to 5.8)	V
Reference power supply voltage		VREFH0	−0.3 to AVCC0 + 0.3 (up to 4.0)	V
Analog power supply voltage		AVCC0, AVCC1*2	−0.3 to +4.0	V
Analog input voltage		V _{AN}	−0.3 to AVCC + 0.3 (up to 4.0)	V
Junction temperature	D version	T _j	−40 to +105	°C
	G version	T _j	−40 to +125	°C
Storage temperature		T _{stg}	−55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS.

When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively.

Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Table 5.2 Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage*1	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
V _{BATT} power supply voltage	V _{BATT}	2.0	—	3.6	V
USB power supply voltage	VCC_USB	—	VCC	—	V
	VSS_USB	—	0	—	V
Analog power supply voltage*1, *2	AVCC0	—	VCC	—	V
	AVSS0	—	0	—	V
	AVCC1	—	VCC	—	V
	AVSS1	—	0	—	V
	VREFH0	2.7	—	AVCC0	V
	VREFL0	—	0	—	V
Input voltage (except for 5 V tolerant ports, except for ports 03, 05 and 40 to 47)*3	V _{in}	−0.3	—	VCC + 0.3	V
Input voltage (ports 03, 05 and 40 to 47)	V _{in}	−0.3	—	AVCC + 0.3	V
Input voltage (5V tolerant ports 11 to 17, ports 20 and 21, ports 30 to 33, port 67, and ports C0 to C3)*4	V _{in}	−0.3	—	VCC + 3.6 (up to 5.5)	V
Input voltage (5V tolerant port 07)	V _{in}	−0.3	—	AVCC + 3.6 (up to 5.5)	V
Operating temperature (D version)	T _{opr}	−40	—	85	°C
Operating temperature (G version)	T _{opr}	−40	—	105	°C

Note 1. Comply with the following potential condition: VCC = AVCC0 = AVCC1 = VCC_USB

Note 2. For details, see section 53.6.11, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

Note 3. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 4. For P32, P31, and P30, input as follows when the V_{BATT} power supply is selected.

V_{in} Min. = −0.3, Max. = V_{BATT} + 0.3 (V_{BATT} = 2.0 to 3.6 V)

Table 5.34 SClg, SClh, and Scli Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
SClg, SClh	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 5.42
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PBcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	Figure 5.43
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	
Scli	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 5.42
		Clock synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PAcyc}	
		Clock synchronous		8	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Master	t_{TXD}	—	15	ns	Figure 5.43
		Slave		—	28		
	Receive data setup time	Clock synchronous	t_{RXS}	20	—	ns	
Receive data hold time	Clock synchronous	t_{RXH}	5	—			

Note 1. t_{PBcyc} : PCLKB cycle; t_{PAcyc} : PCLKA cycle

Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1

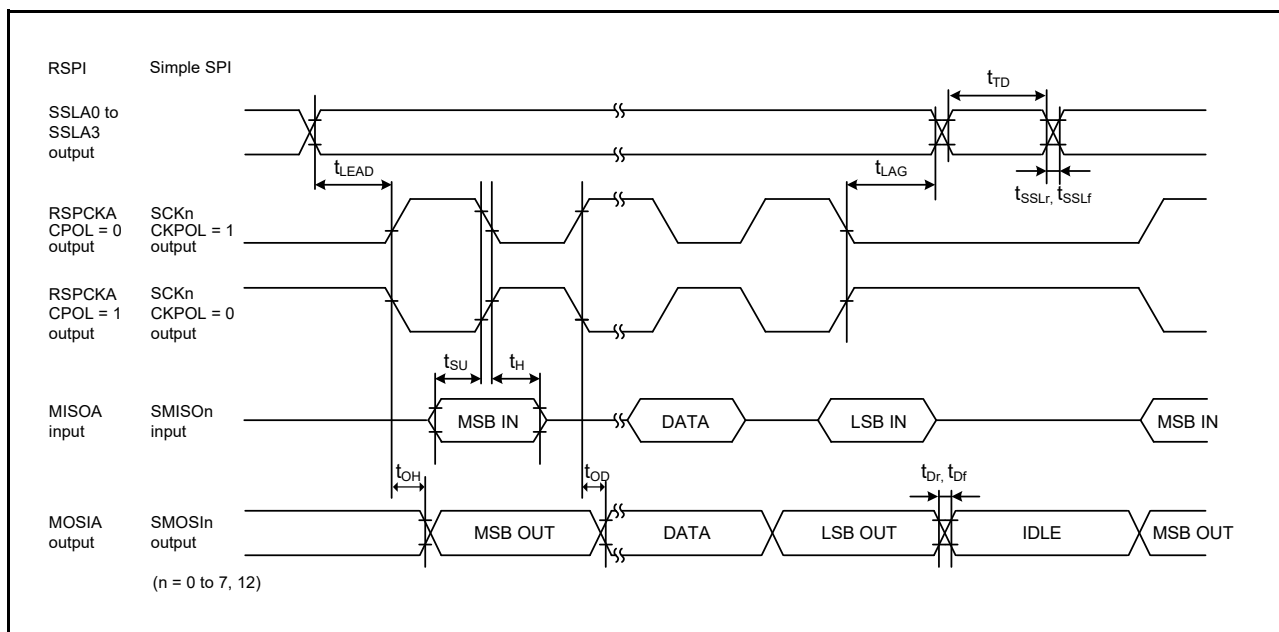


Figure 5.47 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

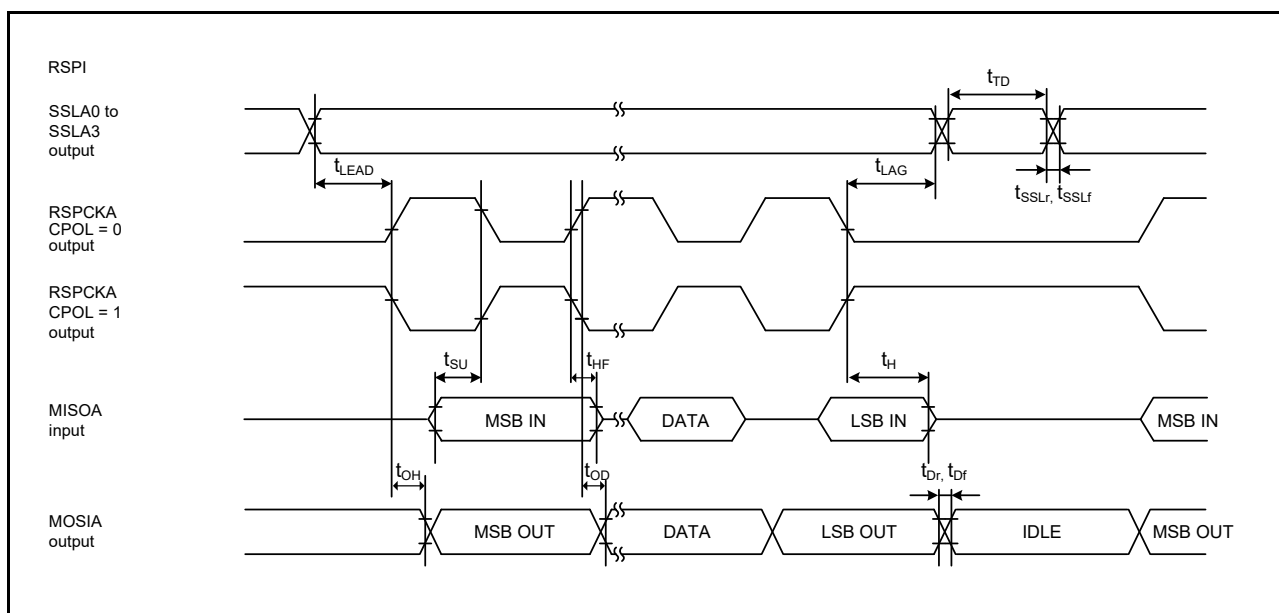


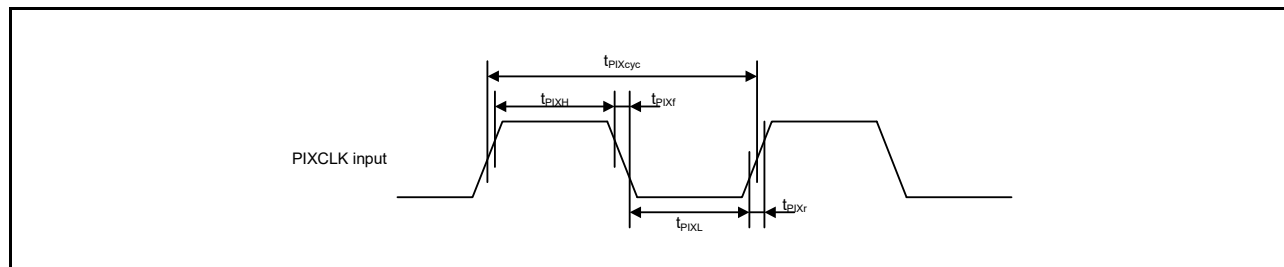
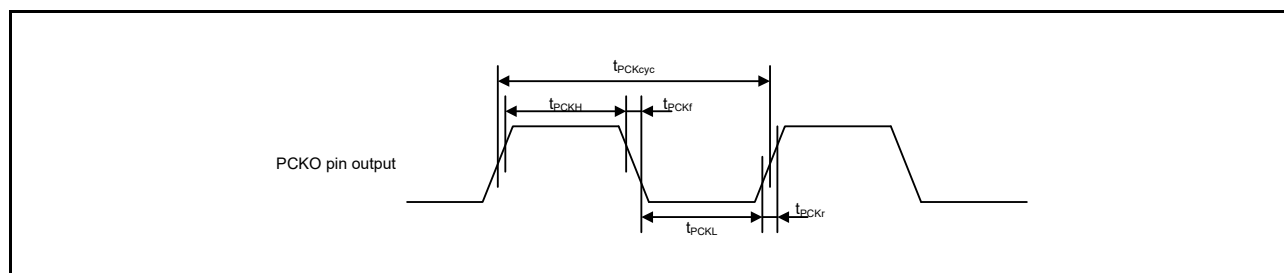
Figure 5.48 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

Table 5.42 PDC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	—	ns	Figure 5.66
	PIXCLK input high pulse width	t_{PIXH}	10	—	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	—	ns	
	PIXCLK rising time	t_{PIXr}	—	5	ns	
	PIXCLK falling time	t_{PIXf}	—	5	ns	
	PCKO output cycle time	t_{PCKcyc}	$2 \times t_{PBcyc}$	—	ns	Figure 5.67
	PCKO output high pulse width	t_{PCKH}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	—	ns	
	PCKO output low pulse width	t_{PCKL}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	—	ns	
	PCKO rising time	t_{PCKr}	—	5	ns	
	PCKO falling time	t_{PCKf}	—	5	ns	
	VSYNC/HSYNC input setup time	t_{SYNCS}	10	—	ns	Figure 5.68
	VSYNC/HSYNC input hold time	t_{SYNCH}	5	—	ns	
	PIXD input setup time	t_{PIXDS}	10	—	ns	
	PIXD input hold time	t_{PIXDH}	5	—	ns	

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.66 PDC Input Clock Timing****Figure 5.67 PDC Output Clock Timing**

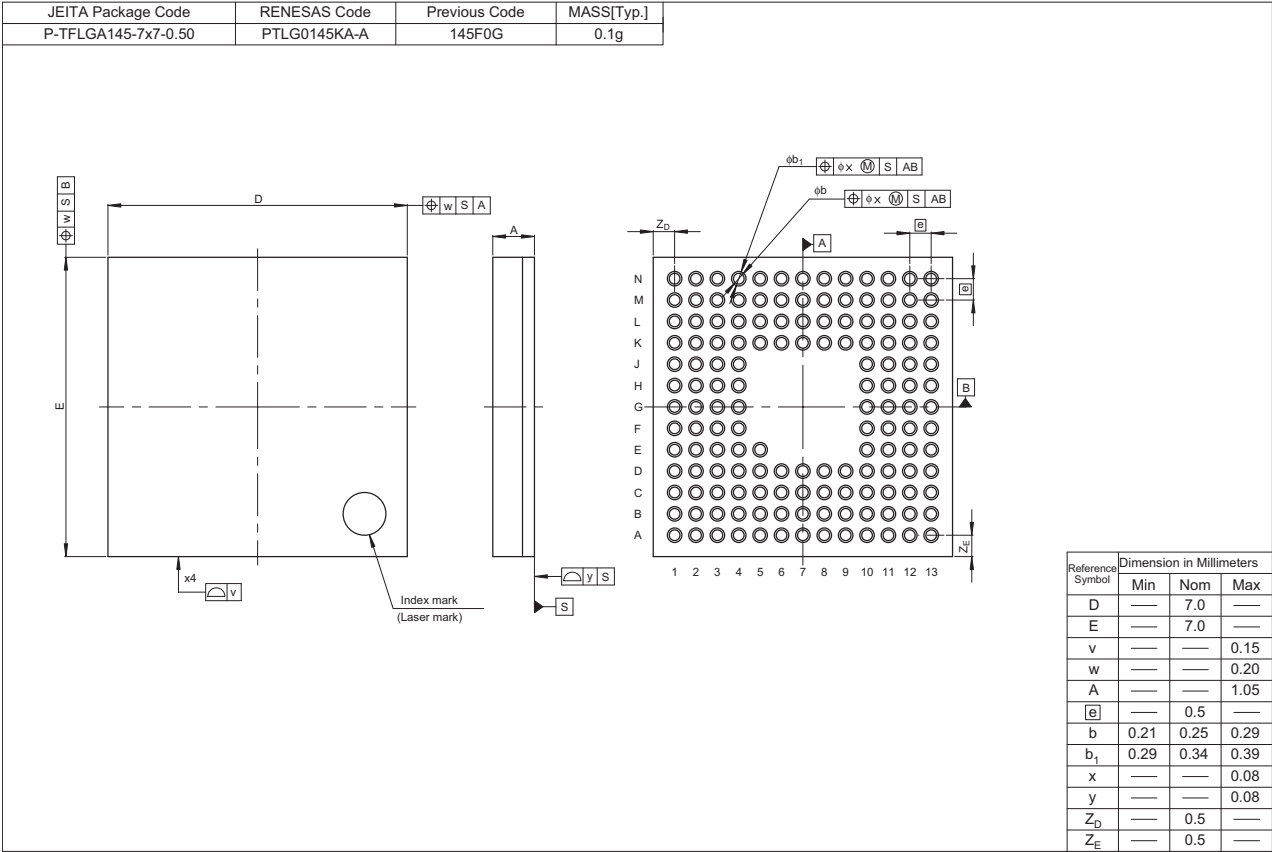


Figure D 145-Pin TFLGA (PTLG0145KA-A)