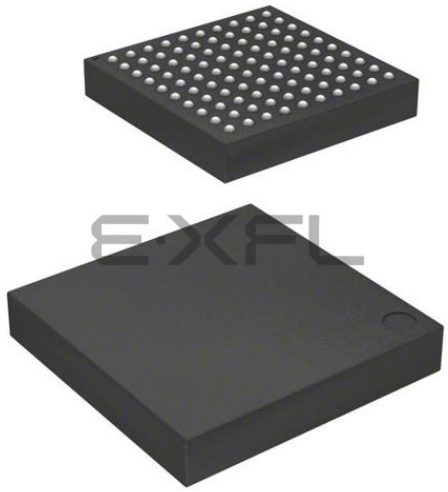
Renesas Electronics America Inc - R5F565N4BDLJ#20 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n4bdlj-20

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
	SD host interface (SDHI)*3	• 1 channel • Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
	SD slave interface (SDSI)*3	• 1 channel • Compliant with the SDIO Card Specification Ver.2.00 (CSA is not supported) • 1-bit SD/4-bit SD/SPI mode • SDIO Proprietary command is supported • SD/SPI Mandatory command is supported • Interrupt requests: 6
	MMC host interface (MMCIF)	• 1 channel • Transfer speed: Data transfer mode (30 MB/s), backward compatible mode (25 MB/s) • Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) • Interface for Multimedia Cards (MMCs) • Device buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt • DMA transfer requests: CE_DATA write and CE_DATA read • Support for card detection, boot operation, high priority interrupt (HPI)
	Parallel data capture unit (PDC)	• 1 channel • Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals • Setting of the image size when clipping of the output for a one-frame image is required
	Graphic-LCD controller (GLCDC)	• 1 channel • Various data formats and LCD panels are supported • Superposition of 3 planes (single-color background, graphic 1, graphic 2) • 32- and 16-bpp color data and 8-, 4-, and 1-bit CLUT data formats are supported
	2D drawing engine (DRW2D)	• 1 channel • Vector drawing (straight lines, triangles, and circles) • Bit blitting (with support for filling, copying, stretching, and rotation) • Bus master function for input and output of frame buffer data 32-, 16-, and 8-bit pixel graphics data are supported • Bus master function for input of texture data Input of texture data (32, 24, 16, 8, 4, 2, or 1 bit) are supported. Run length encoding is supported A CLUT is installed and index data can be converted into color data • Two rendering modes are supported (register mode and display list mode) • Performance counting • Interrupts in response to completion of rendering and processing of the display list

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_ USB	USB0_ DP	6
5	P46	P47	P45	P44	NC							PJ2	P12	VCC_ USB	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

RX65N Group, RX651 Group
PTLG0177KA-A
(177-Pin TFLGA)
(Upper Perspective View)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (7/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
134		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B		ANEX1
135		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B		ANEX0
136		P64	WE#/D3[A3/ D3]/CS4#						
137		P63	CAS#/ D2[A2/D2]/ CS3#						
138		P62	RAS#/ D1[A1/D1]/ CS2#						
139		P61	SDCS#/ D0[A0/D0]/ CS1#						
140	VSS								
141		P60	CS0#						
142	VCC								
143		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DATA17-B	IRQ7	AN107
144	TRDATA7	PG1	D25						
145		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106
146	TRDATA6	PG0	D24						
147		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113
148		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
149	TRSYNC1	P97	D23/A23						
150		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DATA21-B	IRQ3	AN111
151	VSS								
152	TRDATA5	P96	D22/A22						
153	VCC								
154		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2-B/MMC_D2-B	LCD_DATA22-B	IRQ2	AN110
155	TRDATA4	P95	D21/A21						
156		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B	IRQ1	AN109
157		P94	D20/A20						
158		PD0	D0[A0/D0]	POE4#			LCD_EXTCLK-B	IRQ0	AN108
159		P93	D19/A19	POE0#	CTS7#/RTS7#/ SS7#				AN117

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (8/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
160		P92	D18/A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
161		P91	D17/A17		SCK7				AN115
162	VSS								
163		P90	D16/A16		TXD7/SMOSI7/ SSDA7				AN114
164	VCC								
165		P47						IRQ15-DS	AN007
166		P46						IRQ14-DS	AN006
167		P45						IRQ13-DS	AN005
168		P44						IRQ12-DS	AN004
169		P43						IRQ11-DS	AN003
170		P42						IRQ10-DS	AN002
171		P41						IRQ9-DS	AN001
172	VREFL0								
173		P40						IRQ8-DS	AN000
174	VREFH0								
175	AVCC0								
176		P07						IRQ15	ADTRG0#

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 4.1 List of I/O Registers (Address Order) (9 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7709h	ICU	Software Configurable Interrupt B Request Register 9	PIBR9	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 770Ah	ICU	Software Configurable Interrupt B Request Register A	PIBRA	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 770Bh	ICU	Software Configurable Interrupt B Request Register B	PIBRB	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7780h	ICU	Software Configurable Interrupt B Source Select Register X128	SLIBXR128	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7781h	ICU	Software Configurable Interrupt B Source Select Register X129	SLIBXR129	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7782h	ICU	Software Configurable Interrupt B Source Select Register X130	SLIBXR130	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7783h	ICU	Software Configurable Interrupt B Source Select Register X131	SLIBXR131	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7784h	ICU	Software Configurable Interrupt B Source Select Register X132	SLIBXR132	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7785h	ICU	Software Configurable Interrupt B Source Select Register X133	SLIBXR133	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7786h	ICU	Software Configurable Interrupt B Source Select Register X134	SLIBXR134	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7787h	ICU	Software Configurable Interrupt B Source Select Register X135	SLIBXR135	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7788h	ICU	Software Configurable Interrupt B Source Select Register X136	SLIBXR136	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7789h	ICU	Software Configurable Interrupt B Source Select Register X137	SLIBXR137	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Ah	ICU	Software Configurable Interrupt B Source Select Register X138	SLIBXR138	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Bh	ICU	Software Configurable Interrupt B Source Select Register X139	SLIBXR139	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Ch	ICU	Software Configurable Interrupt B Source Select Register X140	SLIBXR140	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Dh	ICU	Software Configurable Interrupt B Source Select Register X141	SLIBXR141	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Eh	ICU	Software Configurable Interrupt B Source Select Register X142	SLIBXR142	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 778Fh	ICU	Software Configurable Interrupt B Source Select Register X143	SLIBXR143	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7790h	ICU	Software Configurable Interrupt B Source Select Register 144	SLIBR144	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7791h	ICU	Software Configurable Interrupt B Source Select Register 145	SLIBR145	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7792h	ICU	Software Configurable Interrupt B Source Select Register 146	SLIBR146	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7793h	ICU	Software Configurable Interrupt B Source Select Register 147	SLIBR147	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7794h	ICU	Software Configurable Interrupt B Source Select Register 148	SLIBR148	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7795h	ICU	Software Configurable Interrupt B Source Select Register 149	SLIBR149	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7796h	ICU	Software Configurable Interrupt B Source Select Register 150	SLIBR150	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7797h	ICU	Software Configurable Interrupt B Source Select Register 151	SLIBR151	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7798h	ICU	Software Configurable Interrupt B Source Select Register 152	SLIBR152	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7799h	ICU	Software Configurable Interrupt B Source Select Register 153	SLIBR153	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Ah	ICU	Software Configurable Interrupt B Source Select Register 154	SLIBR154	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Bh	ICU	Software Configurable Interrupt B Source Select Register 155	SLIBR155	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Ch	ICU	Software Configurable Interrupt B Source Select Register 156	SLIBR156	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (10 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 779Dh	ICU	Software Configurable Interrupt B Source Select Register 157	SLIBR157	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Eh	ICU	Software Configurable Interrupt B Source Select Register 158	SLIBR158	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Fh	ICU	Software Configurable Interrupt B Source Select Register 159	SLIBR159	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A0h	ICU	Software Configurable Interrupt B Source Select Register 160	SLIBR160	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A1h	ICU	Software Configurable Interrupt B Source Select Register 161	SLIBR161	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A2h	ICU	Software Configurable Interrupt B Source Select Register 162	SLIBR162	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A3h	ICU	Software Configurable Interrupt B Source Select Register 163	SLIBR163	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A4h	ICU	Software Configurable Interrupt B Source Select Register 164	SLIBR164	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A5h	ICU	Software Configurable Interrupt B Source Select Register 165	SLIBR165	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A6h	ICU	Software Configurable Interrupt B Source Select Register 166	SLIBR166	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A7h	ICU	Software Configurable Interrupt B Source Select Register 167	SLIBR167	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A8h	ICU	Software Configurable Interrupt B Source Select Register 168	SLIBR168	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A9h	ICU	Software Configurable Interrupt B Source Select Register 169	SLIBR169	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AAh	ICU	Software Configurable Interrupt B Source Select Register 170	SLIBR170	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ABh	ICU	Software Configurable Interrupt B Source Select Register 171	SLIBR171	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ACh	ICU	Software Configurable Interrupt B Source Select Register 172	SLIBR172	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ADh	ICU	Software Configurable Interrupt B Source Select Register 173	SLIBR173	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AEh	ICU	Software Configurable Interrupt B Source Select Register 174	SLIBR174	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AFh	ICU	Software Configurable Interrupt B Source Select Register 175	SLIBR175	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B0h	ICU	Software Configurable Interrupt B Source Select Register 176	SLIBR176	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B1h	ICU	Software Configurable Interrupt B Source Select Register 177	SLIBR177	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B2h	ICU	Software Configurable Interrupt B Source Select Register 178	SLIBR178	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B3h	ICU	Software Configurable Interrupt B Source Select Register 179	SLIBR179	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B4h	ICU	Software Configurable Interrupt B Source Select Register 180	SLIBR180	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B5h	ICU	Software Configurable Interrupt B Source Select Register 181	SLIBR181	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B6h	ICU	Software Configurable Interrupt B Source Select Register 182	SLIBR182	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B7h	ICU	Software Configurable Interrupt B Source Select Register 183	SLIBR183	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B8h	ICU	Software Configurable Interrupt B Source Select Register 184	SLIBR184	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B9h	ICU	Software Configurable Interrupt B Source Select Register 185	SLIBR185	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BAh	ICU	Software Configurable Interrupt B Source Select Register 186	SLIBR186	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BBh	ICU	Software Configurable Interrupt B Source Select Register 187	SLIBR187	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (11 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 77BCh	ICU	Software Configurable Interrupt B Source Select Register 188	SLIBR188	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BDh	ICU	Software Configurable Interrupt B Source Select Register 189	SLIBR189	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BEh	ICU	Software Configurable Interrupt B Source Select Register 190	SLIBR190	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BFh	ICU	Software Configurable Interrupt B Source Select Register 191	SLIBR191	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C0h	ICU	Software Configurable Interrupt B Source Select Register 192	SLIBR192	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C1h	ICU	Software Configurable Interrupt B Source Select Register 193	SLIBR193	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C2h	ICU	Software Configurable Interrupt B Source Select Register 194	SLIBR194	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C3h	ICU	Software Configurable Interrupt B Source Select Register 195	SLIBR195	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C4h	ICU	Software Configurable Interrupt B Source Select Register 196	SLIBR196	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C5h	ICU	Software Configurable Interrupt B Source Select Register 197	SLIBR197	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C6h	ICU	Software Configurable Interrupt B Source Select Register 198	SLIBR198	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C7h	ICU	Software Configurable Interrupt B Source Select Register 199	SLIBR199	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C8h	ICU	Software Configurable Interrupt B Source Select Register 200	SLIBR200	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C9h	ICU	Software Configurable Interrupt B Source Select Register 201	SLIBR201	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CAh	ICU	Software Configurable Interrupt B Source Select Register 202	SLIBR202	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CBh	ICU	Software Configurable Interrupt B Source Select Register 203	SLIBR203	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CCh	ICU	Software Configurable Interrupt B Source Select Register 204	SLIBR204	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CDh	ICU	Software Configurable Interrupt B Source Select Register 205	SLIBR205	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CEh	ICU	Software Configurable Interrupt B Source Select Register 206	SLIBR206	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CFh	ICU	Software Configurable Interrupt B Source Select Register 207	SLIBR207	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7830h	ICU	Group AL0 Interrupt Request Register	GRPAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7834h	ICU	Group AL1 Interrupt Request Register	GRPAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7870h	ICU	Group AL0 Interrupt Request Enable Register	GENAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7874h	ICU	Group AL1 Interrupt Request Enable Register	GENAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7900h	ICU	Software Configurable Interrupt A Request Register 0	PIAR0	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7901h	ICU	Software Configurable Interrupt A Request Register 1	PIAR1	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7902h	ICU	Software Configurable Interrupt A Request Register 2	PIAR2	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7903h	ICU	Software Configurable Interrupt A Request Register 3	PIAR3	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7904h	ICU	Software Configurable Interrupt A Request Register 4	PIAR4	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7905h	ICU	Software Configurable Interrupt A Request Register 5	PIAR5	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 790Bh	ICU	Software Configurable Interrupt A Request Register B	PIARB	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D0h	ICU	Software Configurable Interrupt A Source Select Register 208	SLIAR208	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D1h	ICU	Software Configurable Interrupt A Source Select Register 209	SLIAR209	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (15 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81E6h	PPG0	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E8h	PPG0	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E9h	PPG0	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EAh	PPG0	Output Data Registers H	PODRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EBh	PPG0	Output Data Registers L	PODRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81ECh	PPG0	Next Data Registers H*1	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EDh	PPG0	Next Data Registers L*2	NDRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EEh	PPG0	Next Data Registers H*1	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EFh	PPG0	Next Data Registers L*2	NDRL2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F0h	PPG1	PPG Trigger Select Register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F6h	PPG1	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F7h	PPG1	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F8h	PPG1	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F9h	PPG1	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FAh	PPG1	Output Data Registers H	PODRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FBh	PPG1	Output Data Registers L	PODRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FCh	PPG1	Next Data Registers H*3	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FDh	PPG1	Next Data Registers L*4	NDRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FEh	PPG1	Next Data Registers H*3	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FFh	PPG1	Next Data Registers L*4	NDRL2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR01	Time Constant Register A	TCORA	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR01	Time Constant Register B	TCORB	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR

Table 4.1 List of I/O Registers (Address Order) (21 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 918Ch	S12AD1	A/D Comparison Function Window A/B Status Monitoring Register	ADWINMON	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9190h	S12AD1	A/D Comparison Function Control Register	ADCMPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9192h	S12AD1	A/D Comparison Function Window A Extended Input Select Register	ADCMPANSER	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9193h	S12AD1	A/D Comparison Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9194h	S12AD1	A/D Comparison Function Window A Channel Select Register 0	ADCMPANSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9196h	S12AD1	A/D Comparison Function Window A Channel Select Register 1	ADCMPANSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9198h	S12AD1	A/D Comparison Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 919Ah	S12AD1	A/D Comparison Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 919Ch	S12AD1	A/D Comparison Function Window A Lower Level Setting Register	ADCMPDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 919Eh	S12AD1	A/D Comparison Function Window A Upper Level Setting Register	ADCMPDR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A0h	S12AD1	A/D Comparison Function Window A Channel Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A2h	S12AD1	A/D Comparison Function Window A Channel Status Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A4h	S12AD1	A/D Comparison Function Window A Extended Input Channel Status Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A6h	S12AD1	A/D Comparison Function Window B Channel Select Register	ADCMPBNSR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A8h	S12AD1	A/D Comparison Function Window B Lower Level Setting Register	ADWINLLB	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91AAh	S12AD1	A/D Comparison Function Window B Upper Level Setting Register	ADWINULB	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91ACh	S12AD1	A/D Comparison Function Window B Channel Status Register	ADCMPBSR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D8h	S12AD1	A/D Group C Extended Input Control Register	ADGCEXCR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91DEh	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91DFh	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADFa

Table 4.1 List of I/O Registers (Address Order) (25 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A046h	SMCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A049h	SCI2	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Ah	SCI2	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Bh	SCI2	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Ch	SCI2	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Eh	SCI2	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Fh	SCI2	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A04Eh	SCI2	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A050h	SCI2	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A051h	SCI2	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A050h	SCI2	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A052h	SCI2	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A066h	SMCI3	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (44 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	Hour Capture Register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	Second Capture Register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	BCNT0 Capture Register 2	BCNT0CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	Minute Capture Register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	BCNT1 Capture Register 2	BCNT1CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	Hour Capture Register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	BCNT2 Capture Register 2	BCNT2CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	Date Capture Register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	BCNT3 Capture Register 2	BCNT3CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ch	RTC	Month Capture Register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C4C0h	POE3	Input Level Control/Status Register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C2h	POE3	Output Level Control/Status Register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C4h	POE3	Input Level Control/Status Register 2	ICSR2	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C6h	POE3	Output Level Control/Status Register 2	OCSR2	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C8h	POE3	Input Level Control/Status Register 3	ICSR3	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4CAh	POE3	Software Port Output Enable Register	SPOER	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4CBh	POE3	Port Output Enable Control Register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4CCh	POE3	Port Output Enable Control Register 2	POECR2	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D0h	POE3	Port Output Enable Control Register 4	POECR4	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D2h	POE3	Port Output Enable Control Register 5	POECR5	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D6h	POE3	Input Level Control/Status Register 4	ICSR4	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D8h	POE3	Input Level Control/Status Register 5	ICSR5	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4DAh	POE3	Active Level Setting Register 1	ALR1	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4DCh	POE3	Input Level Control/Status Register 6	ICSR6	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E4h	POE3	MTU0 Pin Select Register 1	M0SELR1	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E5h	POE3	MTU0 Pin Select Register 2	M0SELR2	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E6h	POE3	MTU3 Pin Select Register	M3SELR	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E7h	POE3	MTU4 Pin Select Register 1	M4SELR1	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E8h	POE3	MTU4 Pin Select Register 2	M4SELR2	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4EAh	POE3	MTU6 Pin Select Register	M6SELR	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C500h	TEMPS	Temperature Sensor Control Register	TSCR	8	8	2, 3 PCLKB	2 ICLK	TEMPS
0008 C5C0h	DA	D/A A/D Synchronous Unit Select Register	DAADUSR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0009 0200h to 0009 03FFh	CAN0	Mailbox Registers 0 to 31	MB0 to 31	128	8, 16, 32*6	2, 3 PCLKB	2 ICLK	CAN
0009 0400h to 0009 041Fh	CAN0	Mask Registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0420h	CAN0	FIFO Received ID Compare Register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0424h	CAN0	FIFO Received ID Compare Register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0428h	CAN0	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 042Ch	CAN0	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN

Table 4.1 List of I/O Registers (Address Order) (52 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1290h	MTU0	Noise Filter Control Register 0	NFCR0	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1291h	MTU1	Noise Filter Control Register 1	NFCR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1292h	MTU2	Noise Filter Control Register 2	NFCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1293h	MTU3	Noise Filter Control Register 3	NFCR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1294h	MTU4	Noise Filter Control Register 4	NFCR4	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1298h	MTU8	Noise Filter Control Register 8	NFCR8	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1299h	MTU0	Noise Filter Control Register C	NFCRC	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1300h	MTU0	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1308h	MTU0	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1320h	MTU0	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1328h	MTU0	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1380h	MTU1	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1388h	MTU1	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1391h	MTU1	Timer Mode Register 3	TMDR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1394h	MTU1	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A0h	MTU1	Timer Longword Counter	TCNTLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A4h	MTU1	Timer Longword General Register	TGRALW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A8h	MTU1	Timer Longword General Register	TGRBLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1400h	MTU2	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (60 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 13D0h	GLCDC	Contrast Adjustment Register	CONTRAST	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13D4h	GLCDC	Panel Dither Control Register	PANELDTHA	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13E4h	GLCDC	Output Phase Control Register	CLKPHASE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1404h	GLCDC	Reference Timing Setting Register	TCONTIM	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1408h	GLCDC	Vertical Timing Setting Register A1	TCONSTVA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 140Ch	GLCDC	Vertical Timing Setting Register A2	TCONSTVA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1410h	GLCDC	Vertical Timing Setting Register B1	TCONSTVB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1414h	GLCDC	Vertical Timing Setting Register B2	TCONSTVB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1418h	GLCDC	Horizontal Timing Setting Register A1	TCONSTHA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 141Ch	GLCDC	Horizontal Timing Setting Register A2	TCONSTHA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1420h	GLCDC	Horizontal Timing Setting Register B1	TCONSTHB1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1424h	GLCDC	Horizontal Timing Setting Register B2	TCONSTHB2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1428h	GLCDC	Data Enable Polarity Setting Register	TCONDE	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1440h	GLCDC	Status Detection Control Register	DTCTEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1444h	GLCDC	Interrupt Request Enable Control Register	INTEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1448h	GLCDC	Detected Status Clear Register	STCLR	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 144Ch	GLCDC	Detected Status Monitor Register	STMON	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1450h	GLCDC	Panel Clock Control Register	PANELCLK	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 3000h	DRW2D	Geometry Control Register	CONTROL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3000h	DRW2D	Status Register	STATUS	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3004h	DRW2D	Surface Control Register	CONTROL2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3004h	DRW2D	Hardware Version Register	HWVER	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3010h	DRW2D	Limiter 1 Start Value Register	L1START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3014h	DRW2D	Limiter 2 Start Value Register	L2START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3018h	DRW2D	Limiter 3 Start Value Register	L3START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 301Ch	DRW2D	Limiter 4 Start Value Register	L4START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3020h	DRW2D	Limiter 5 Start Value Register	L5START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3024h	DRW2D	Limiter 6 Start Value Register	L6START	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3028h	DRW2D	Limiter 1 X-Axis Increment Register	L1XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 302Ch	DRW2D	Limiter 2 X-Axis Increment Register	L2XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3030h	DRW2D	Limiter 3 X-Axis Increment Register	L3XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3034h	DRW2D	Limiter 4 X-Axis Increment Register	L4XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3038h	DRW2D	Limiter 5 X-Axis Increment Register	L5XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 303Ch	DRW2D	Limiter 6 X-Axis Increment Register	L6XADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3040h	DRW2D	Limiter 1 Y-Axis Increment Register	L1YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3044h	DRW2D	Limiter 2 Y-Axis Increment Register	L2YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3048h	DRW2D	Limiter 3 Y-Axis Increment Register	L3YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 304Ch	DRW2D	Limiter 4 Y-Axis Increment Register	L4YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3050h	DRW2D	Limiter 5 Y-Axis Increment Register	L5YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3054h	DRW2D	Limiter 6 Y-Axis Increment Register	L6YADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3058h	DRW2D	Limiter 1 Band Width Parameter Register	L1BAND	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 305Ch	DRW2D	Limiter 2 Band Width Parameter Register	L2BAND	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3064h	DRW2D	Base Color Register	COLOR1	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3068h	DRW2D	Secondary Color Register	COLOR2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3074h	DRW2D	Pattern Register	PATTERN	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3078h	DRW2D	Bounding Box Dimension Register	SIZE	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 307Ch	DRW2D	Frame Buffer Pitch Register	PITCH	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3080h	DRW2D	Frame Buffer Base Address Register	ORIGIN	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3090h	DRW2D	U Limiter Start Value Register	LUST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 3094h	DRW2D	U Limiter X-Axis Increment Register	LUXADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D

Table 4.1 List of I/O Registers (Address Order) (61 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 3098h	DRW2D	U Limiter Y-Axis Increment Register	LUYADD	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 309Ch	DRW2D	V Limiter Start Value Integer Part Register	LVSTI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A0h	DRW2D	V Limiter Start Value Fractional Part Register	LVSTF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A4h	DRW2D	V Limiter X-Axis Increment Integer Part Register	LVXADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30A8h	DRW2D	V Limiter Y-Axis Increment Integer Part Register	LVYADDI	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30ACh	DRW2D	V Limiter Increment Fractional Parts Register	LVYXADDF	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B4h	DRW2D	Texels Per Texture Line Register	TEXPITCH	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30B8h	DRW2D	Texture Mask Register	TEXMSK	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30BCh	DRW2D	Texture Base Address Register	TEXORG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C0h	DRW2D	Interrupt Control Register	IRQCTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C4h	DRW2D	Cache Control Register	CACHECTL	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30C8h	DRW2D	Display List Start Address Register	DLISTST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30CCh	DRW2D	Performance Counter 1	PERFCNT1	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D0h	DRW2D	Performance Counter 2	PERFCNT2	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30D4h	DRW2D	Performance Counters Control Register	PERFTRG	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30DCh	DRW2D	CLUT Start Address Register	TEXCLADDR	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E0h	DRW2D	CLUT Data Register	TEXCLDATA	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E4h	DRW2D	CLUT Offset Register	TEXCLOFST	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
000E 30E8h	DRW2D	Chroma Key Register	COLKEY	32	32	2, 3 PCLKA	1, 2 ICLK	DRW2D
007F C040h	FLASH	Data Flash Memory Access Frequency Setting Register	EEPFCLK	8	8	2 FCLK		Flash
FE7F 7D7Ch	TEMPS	Temperature Sensor Calibration Data Register	TSCDR	32	32	1 to 3 ICLK		TEMPS
FE7F 7D90h	FLASH	Unique ID Register 0	UIDR0	32	32	1 to 3 ICLK		Flash
FE7F 7D94h	FLASH	Unique ID Register 1	UIDR1	32	32	1 to 3 ICLK		Flash
FE7F 7D98h	FLASH	Unique ID Register 2	UIDR2	32	32	1 to 3 ICLK		Flash
FE7F 7D9Ch	FLASH	Unique ID Register 3	UIDR3	32	32	1 to 3 ICLK		Flash

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 0008 81ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 0008 81EEh and 0008 81ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 0008 81EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 0008 81EFh and 0008 81EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 0008 81FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 0008 81FEh and 0008 81FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 0008 81FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 0008 81FFh and 0008 81FDh, respectively.

Note 5. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 6. The address must end with 0h, 4h, 8h, or Ch when access is made in 32-bit units. The address must end with 0h, 2h, 4h, 6h, 8h, Ah, Ch, or Eh when access is made in 16-bit units.

Note 7. When the register is accessed while the GLCDC is operating, a delay may be generated in accessing.

Table 5.4 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Input pull-up MOS current	Other than P35	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μA	V_{in} = VCC
Input capacitance	All input pins (except for ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	Ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM		—	—	16		

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

5.3.1 Reset Timing

Table 5.13 Reset Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	1	—	—	ms	Figure 5.1
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 5.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	54	—	55	t_{Lcyc}	Figure 5.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	100	—	108	t_{Lcyc}	

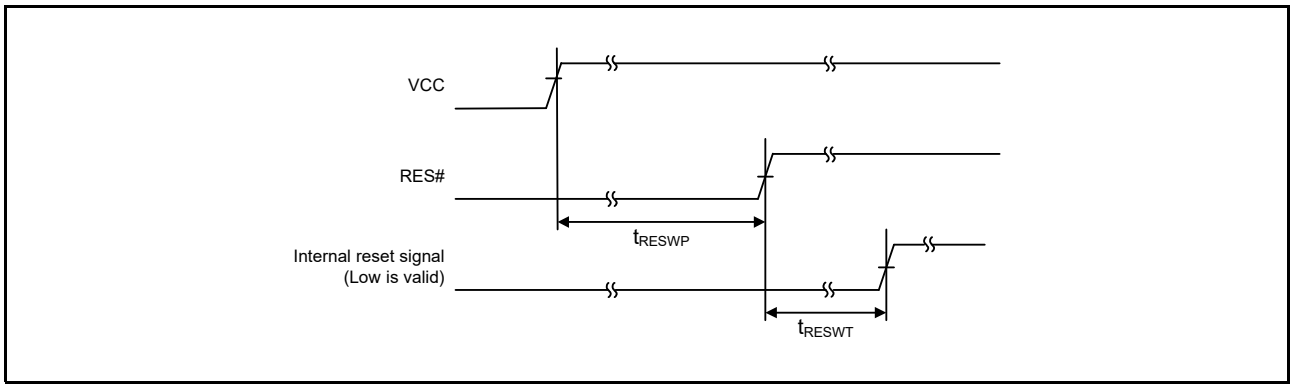


Figure 5.1 Reset Input Timing at Power-On

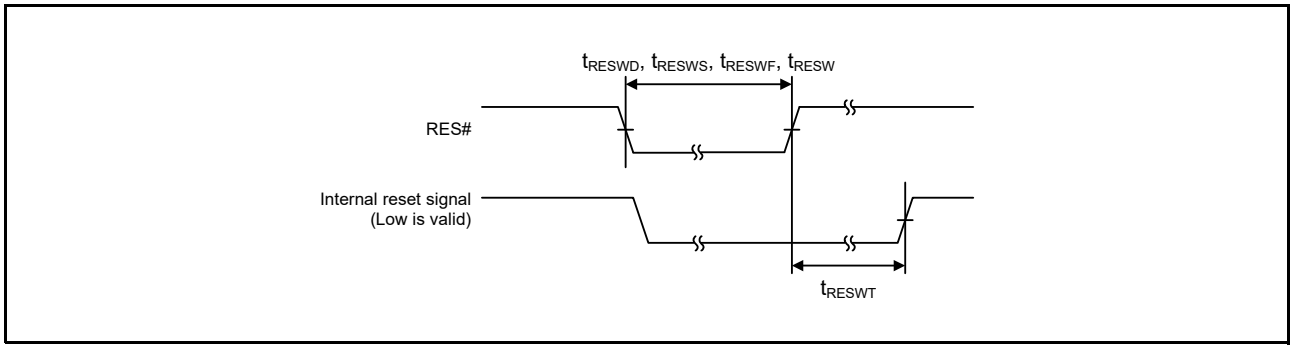
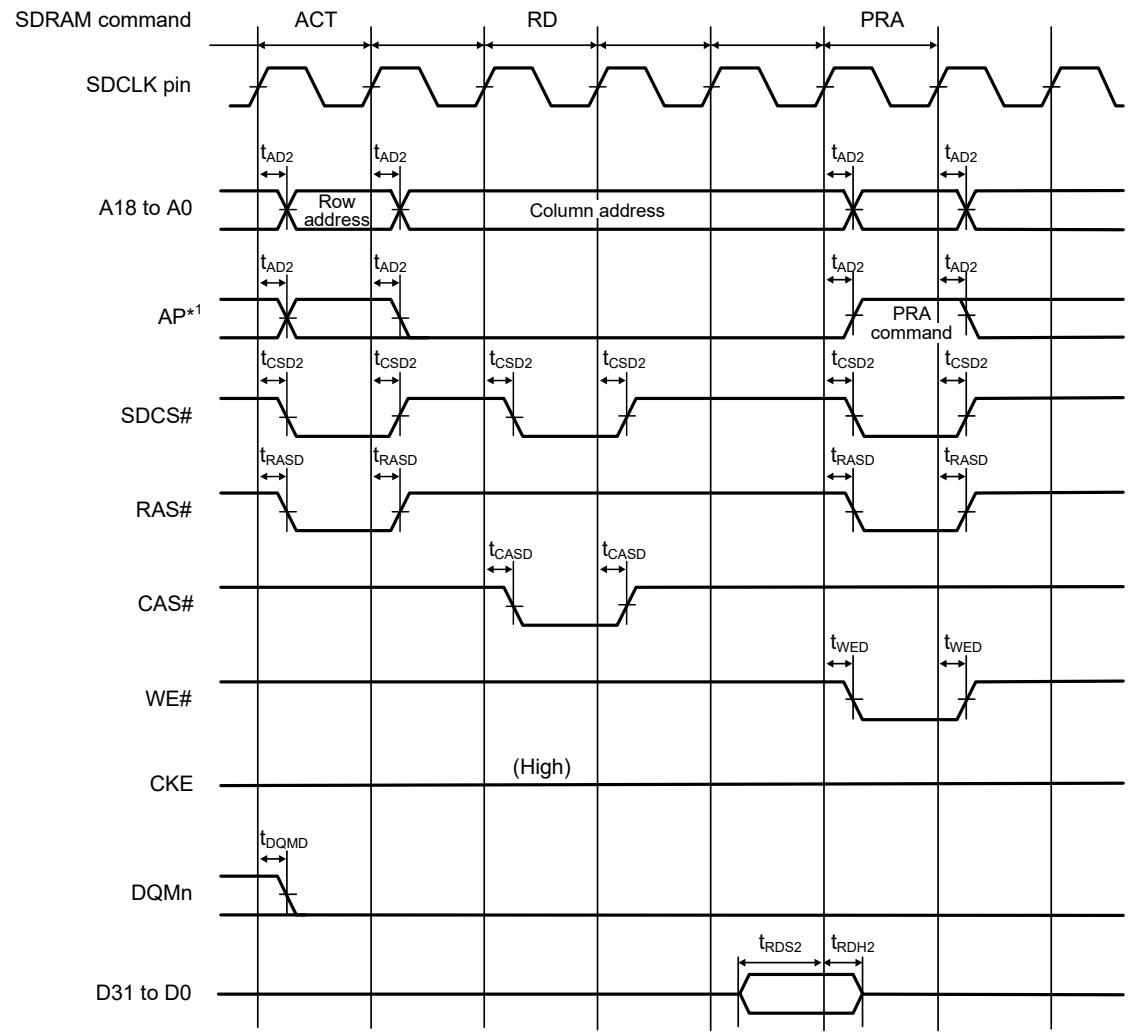


Figure 5.2 Reset Input Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.23 SDRAM Space Single Read Bus Timing

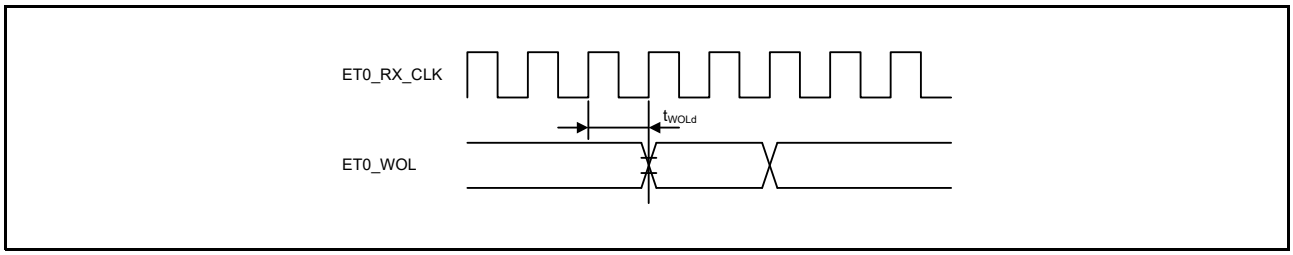


Figure 5.65 WOL Output Timing (MII)

Table 5.55 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.18	1.9	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.9	11	—	1.7	10	ms
	128 bytes	t_{DP128}	—	4.7	27	—	2.9	16	—	2.6	15	ms
	256 bytes	t_{DP256}	—	8.9	50	—	5.4	31	—	4.9	28	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	33	—	—	30	µs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	100000 *2	—	—	Times
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	132	—	—	120	µs
First suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	216	—	—	132	—	—	120	µs
	128 bytes	—	—	—	216	—	—	132	—	—	120	µs
	256 bytes	—	—	—	216	—	—	132	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Suspend delay time during erasing (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	10	—	—	Year

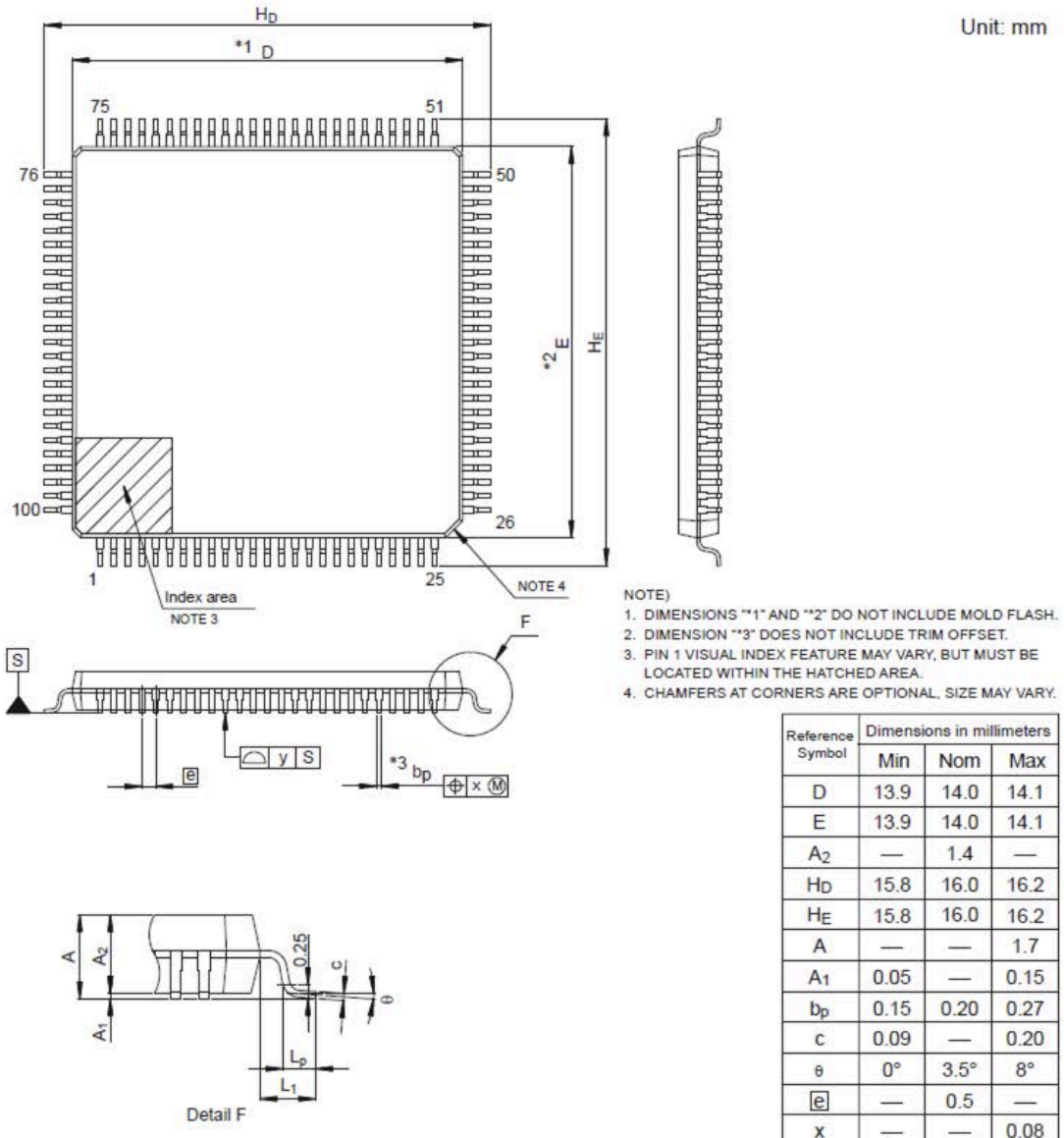
Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure G 100-Pin LFQFP (PLQP0100KB-B)