Renesas Electronics America Inc - R5F565N7ADFB#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n7adfb-30

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.

Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, see Table 1.2, Code Flash Memory Capacity and Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	• Capacity: 512 Kbytes/768 Kbytes/1 Mbyte/1.5 Mbytes/2 Mbytes • 50 MHz ≤ No-wait cycle access 100 MHz ≤ 1-wait cycle access 100 MHz ≥ 2-wait cycle access • Instructions hitting the ROM cache or operand = 120 MHz: No-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode) • Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. • A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	• Capacity: 32 Kbytes • Programming/erasing: 100,000 times
	RAM	• Capacity: 256 Kbytes (Products with 1 Mbyte of code flash memory or less) RAM: 256 Kbytes • Capacity: 640 Kbytes (Products with at least 1.5 Mbytes of code flash memory) RAM: 256 Kbytes Expansion RAM: 384 Kbytes • 120 MHz, no-wait access
	Standby RAM	• Capacity: 8 Kbytes • Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access

Table 1.1 Outline of Specifications (2/9)

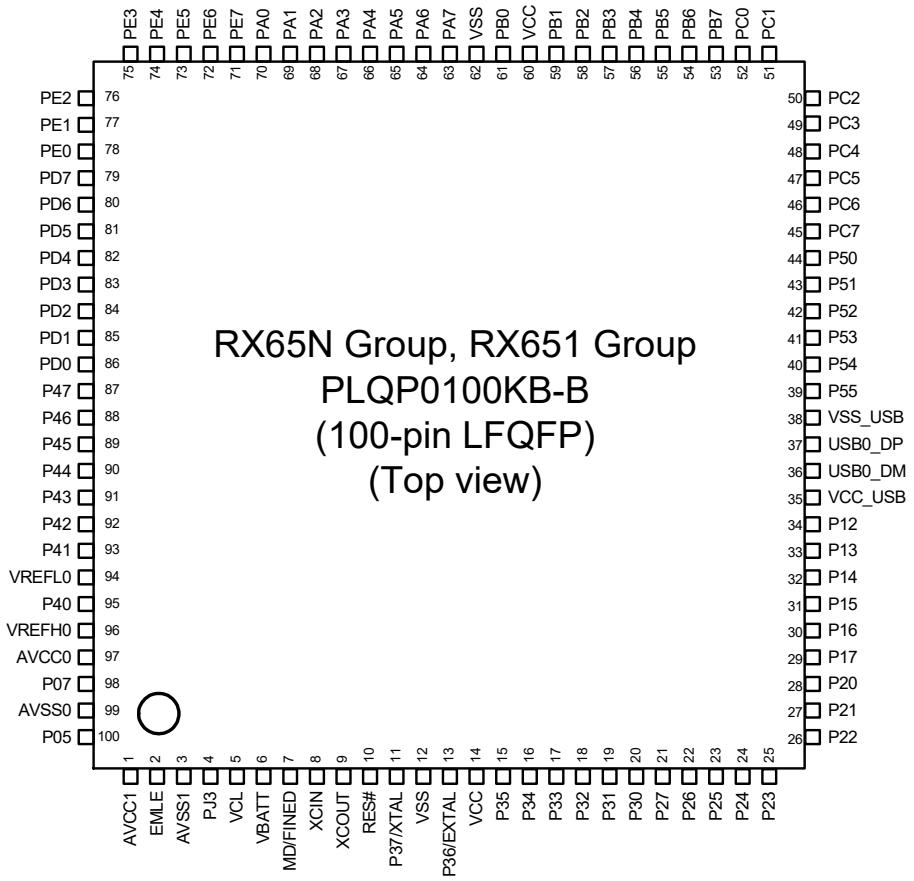
Classification	Module/Function	Description
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (for the SCI interface) Boot mode (for the USB interface) Boot mode (for the FINE interface) • Selection of operating mode by register setting Single-chip mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode • Endian selectable
Clock	Clock generation circuit	• Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz Peripheral modules of MTU3, RSPI, SCIi, ETHERC, EDMAC, AES, GLCDC, and DRW2D run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, 2.80 V) • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, 2.85 V) Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking

Table 1.1 Outline of Specifications (4/9)

Classification	Module/Function	Description
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 83 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Digital filtering of signals from the input capture pins • Event linking by the ELC
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/A32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU3 waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • Additional programming of output control target pins is enabled
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B/ RSPCKC-A/RSPCKC-B	I/O	Clock input/output pin
	MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B/ MOSIC-A/MOSIC-B	I/O	Inputs or outputs data output from the master
	MISOA-A/MISOA-B/ MISOB-A/MISOB-B/ MISOC-A/MISOC-B	I/O	Inputs or outputs data output from the slave
	SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B/ SSLC0-A/SSLC0-B	I/O	Input or output pin for slave selection
	SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B/ SSLC1-A/SSLC1-B, SSLA2-A/SSLA2-B/ SSLB2-A/SSLB2-B/ SSLC2-A/SSLC2-B, SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B/ SSLC3-A/SSLC3-B	Output	Output pin for slave selection
Quad serial peripheral interface	QSPCLK-A/QSPCLK-B	Output	QSPI clock output pin
	QSSL-A/QSSL-B	Output	QSPI slave output pin
	QMO-A/QMO-B, QIO0-A/QIO0-B	I/O	Master transmit data/data 0
	QMI-A/QMI-B, QIO1-A/QIO1-B	I/O	Master input data/data 1
	QIO2-A/QIO2-B, QIO3-A/QIO3-B	I/O	Data 2, data 3
MMC host interface	MMC_CLK-A/ MMC_CLK-B	Output	MMC clock pin
	MMC_CMD-A/ MMC_CMD-B	I/O	Command/response pin
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pin
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pin
SD host interface	SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C to SDHI_D0-A/ SDHI_D0-B/SDHI_D1-C	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
SD slave interface	SDSI_CLK-A/SDSI_CLK-B	Input	SD clock input pin
	SDSI_CMD-A/SDSI_CMD-B	I/O	SD command input, response output signal pin
	SDSI_D3-A/SDSI_D3-B, SDSI_D2-A/SDSI_D2-B, SDSI_D1-A/SDSI_D1-B, SDSI_D0-A/SDSI_D0-B	I/O	SD data bus pins



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.9 Pin Assignment (100-Pin LFQFP)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
A1	AVSS0								
A2	AVCC0								
A3	VREFL0								
A4		P42						IRQ10-DS	AN002
A5		P46						IRQ14-DS	AN006
A6	VCC								
A7	VSS								
A8		P94	D20/A20						
A9	VCC								
A10	TRSYNC1	P97	D23/A23						
A11		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106
A12		P60	CS0#						
A13		P63	CAS#/ D2[A2/D2]/ CS3#						
A14		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B		ANEX1
A15		PE2	D10[A10/ D10]/D2[A2/ D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100
B1		P05						IRQ13	DA1
B2		P07						IRQ15	ADTRG0#
B3		P40						IRQ8-DS	AN000
B4		P41						IRQ9-DS	AN001
B5		P47						IRQ15-DS	AN007
B6		P91	D17/A17		SCK7				AN115
B7		P92	D18/A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B	IRQ1	AN109
B9	TRDATA5	P96	D22/A22						
B10		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
B11	TRDATA7	PG1	D25						
B12	VSS								
B13		P64	WE#/D3[A3/ D3]/CS4#						
B14		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B		ANEX0

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (8/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
R9		P53*2	BCLK						
R10	VSS								
R11	VCC								
R12		P80	EDREQ0	MTIOC3B/ PO26	ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10#	QIO2-A/SDHI_WP/ MMC_D2-A	LCD_DATA14-A		
R13		P76	CS6#	PO22	ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11	QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A	LCD_DATA18-A		
R14		P74	A20/CS4#	PO19	ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11#		LCD_DATA21-A		
R15		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A		LCD_DATA22-A	IRQ12	

Note 1. The 176-pin LFBGA does not include the E5 pin.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (7/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
134		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B		ANEX1
135		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B		ANEX0
136		P64	WE#/D3[A3/ D3]/CS4#						
137		P63	CAS#/ D2[A2/D2]/ CS3#						
138		P62	RAS#/ D1[A1/D1]/ CS2#						
139		P61	SDCS#/ D0[A0/D0]/ CS1#						
140	VSS								
141		P60	CS0#						
142	VCC								
143		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DATA17-B	IRQ7	AN107
144	TRDATA7	PG1	D25						
145		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106
146	TRDATA6	PG0	D24						
147		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113
148		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
149	TRSYNC1	P97	D23/A23						
150		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DATA21-B	IRQ3	AN111
151	VSS								
152	TRDATA5	P96	D22/A22						
153	VCC								
154		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2-B/MMC_D2-B	LCD_DATA22-B	IRQ2	AN110
155	TRDATA4	P95	D21/A21						
156		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B	IRQ1	AN109
157		P94	D20/A20						
158		PD0	D0[A0/D0]	POE4#			LCD_EXTCLK-B	IRQ0	AN108
159		P93	D19/A19	POE0#	CTS7#/RTS7#/ SS7#				AN117

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (3/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
49	VSS_USB								
50		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7*1				
51	TRDATA3	P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7*1/ SMOSI7*1/ SSDA7*1/CRX1			IRQ10	
52	TRDATA2	P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
53		P53*2	BCLK						
54		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
55		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
56		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
57	VSS								
58	TRCLK	P83	EDACK1	MTIOC4C	ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10#				
59	VCC								
60	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A	MMC_D7-A		IRQ14	
61		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A		IRQ13	
62		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A	MMC_D5-A			
63	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10	MMC_D4-A			
64	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A			
65	TRDATA0	P80	EDREQ0	MTIOC3B/ PO26	ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10#	QIO2-A/SDHI_WP/ MMC_D2-A			
66		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A	QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A			
67		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5	QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A			
68	TRDATA7	P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A			

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (5/5)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
J6	VCC_USB								
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
J8		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A				
J9		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
J10		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
K1		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#				
K2		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB				
K3		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID			IRQ8	
K4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA			IRQ4	
K5					USB0_DM				
K6					USB0_DP				
K7		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
K8		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A				
K9		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5				
K10		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A				

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 4.1 List of I/O Registers (Address Order) (21 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 918Ch	S12AD1	A/D Comparison Function Window A/B Status Monitoring Register	ADWINMON	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9190h	S12AD1	A/D Comparison Function Control Register	ADCMPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9192h	S12AD1	A/D Comparison Function Window A Extended Input Select Register	ADCMPANSER	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9193h	S12AD1	A/D Comparison Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9194h	S12AD1	A/D Comparison Function Window A Channel Select Register 0	ADCMPANSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9196h	S12AD1	A/D Comparison Function Window A Channel Select Register 1	ADCMPANSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 9198h	S12AD1	A/D Comparison Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 919Ah	S12AD1	A/D Comparison Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 919Ch	S12AD1	A/D Comparison Function Window A Lower Level Setting Register	ADCMPDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 919Eh	S12AD1	A/D Comparison Function Window A Upper Level Setting Register	ADCMPDR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A0h	S12AD1	A/D Comparison Function Window A Channel Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A2h	S12AD1	A/D Comparison Function Window A Channel Status Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A4h	S12AD1	A/D Comparison Function Window A Extended Input Channel Status Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A6h	S12AD1	A/D Comparison Function Window B Channel Select Register	ADCMPBNSR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91A8h	S12AD1	A/D Comparison Function Window B Lower Level Setting Register	ADWINLLB	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91AAh	S12AD1	A/D Comparison Function Window B Upper Level Setting Register	ADWINULB	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91ACh	S12AD1	A/D Comparison Function Window B Channel Status Register	ADCMPBSR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D8h	S12AD1	A/D Group C Extended Input Control Register	ADGCEXCR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91DEh	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91DFh	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADFa
0008 91E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADFa

Table 4.1 List of I/O Registers (Address Order) (27 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A08Ah	SCI4	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Bh	SCI4	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Ch	SCI4	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A091h	SCI4	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A090h	SCI4	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A092h	SCI4	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A9h	SCI5	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0AAh	SCI5	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0ABh	SCI5	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (41 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B8h	MPC	PF0 Pin Function Control Register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B9h	MPC	PF1 Pin Function Control Register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1BDh	MPC	PF5 Pin Function Control Register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D0h	MPC	PJ0 Pin Function Control Register	PJ0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D1h	MPC	PJ1 Pin Function Control Register	PJ1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D2h	MPC	PJ2 Pin Function Control Register	PJ2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D5h	MPC	PJ5 Pin Function Control Register	PJ5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption

Table 4.1 List of I/O Registers (Address Order) (48 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb

Table 4.1 List of I/O Registers (Address Order) (52 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1290h	MTU0	Noise Filter Control Register 0	NFCR0	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1291h	MTU1	Noise Filter Control Register 1	NFCR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1292h	MTU2	Noise Filter Control Register 2	NFCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1293h	MTU3	Noise Filter Control Register 3	NFCR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1294h	MTU4	Noise Filter Control Register 4	NFCR4	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1298h	MTU8	Noise Filter Control Register 8	NFCR8	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1299h	MTU0	Noise Filter Control Register C	NFCRC	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1300h	MTU0	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1308h	MTU0	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1320h	MTU0	Timer General Register E	TGRE	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1328h	MTU0	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1380h	MTU1	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1388h	MTU1	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1391h	MTU1	Timer Mode Register 3	TMDR3	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1394h	MTU1	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A0h	MTU1	Timer Longword Counter	TCNTLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A4h	MTU1	Timer Longword General Register	TGRALW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 13A8h	MTU1	Timer Longword General Register	TGRBLW	32	32	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1400h	MTU2	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

5.3.4 Control Signal Timing

Table 5.23 Control Signal Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 5.14
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 5.14
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 5.15
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 5.15

Note 1. t_{PBcyc}: PCLKB cycle

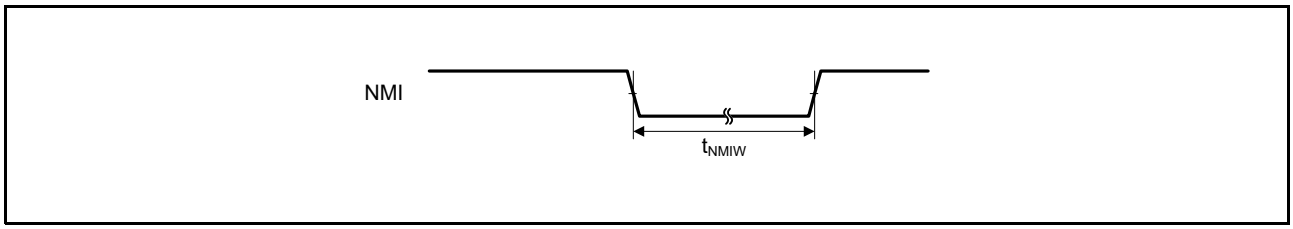


Figure 5.14 NMI Interrupt Input Timing

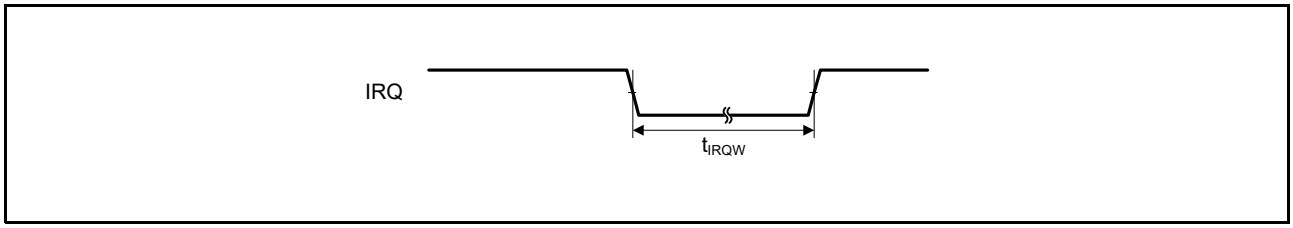
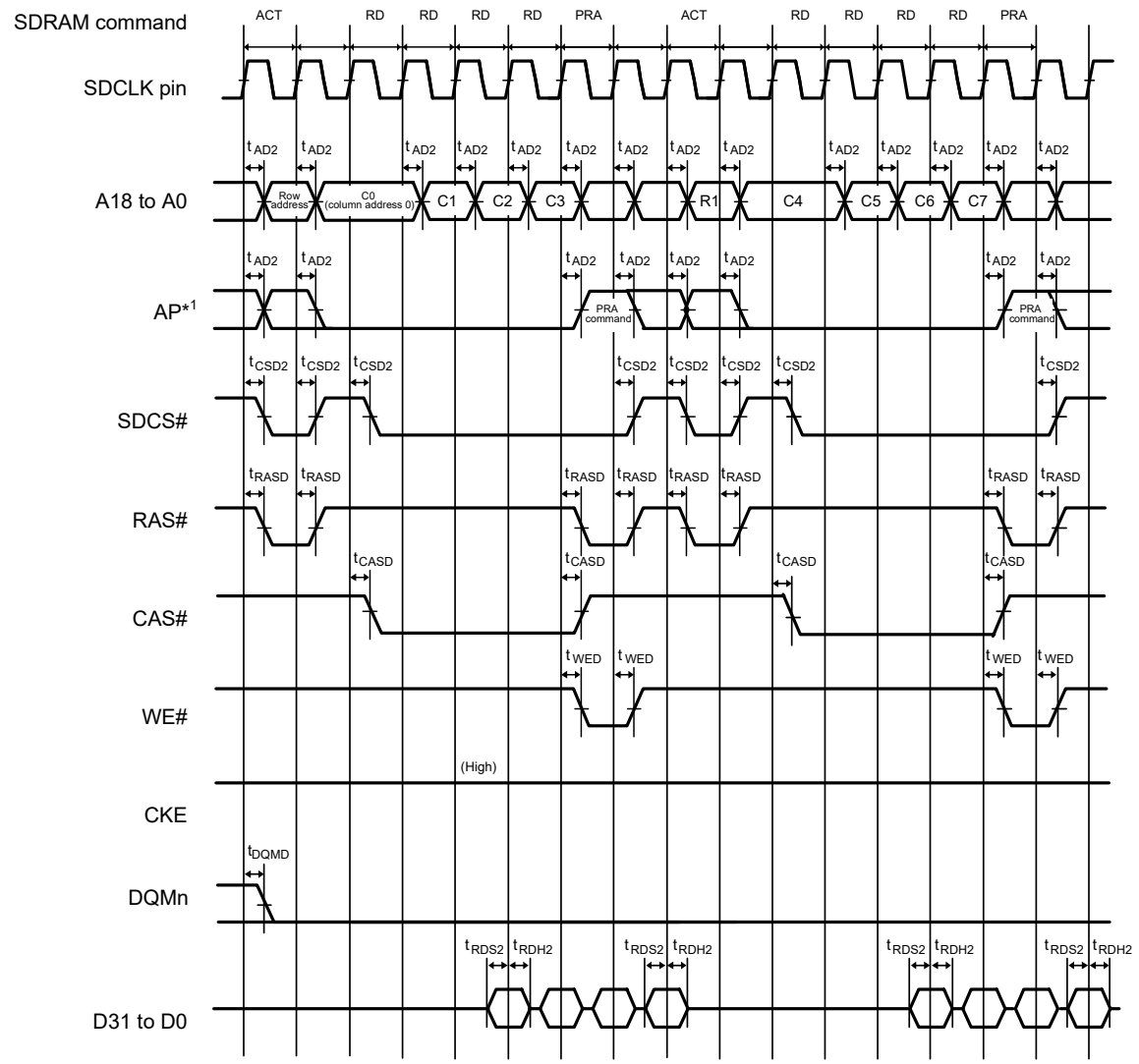


Figure 5.15 IRQ Interrupt Input Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.27 SDRAM Space Multiple Read Line Stride Bus Timing

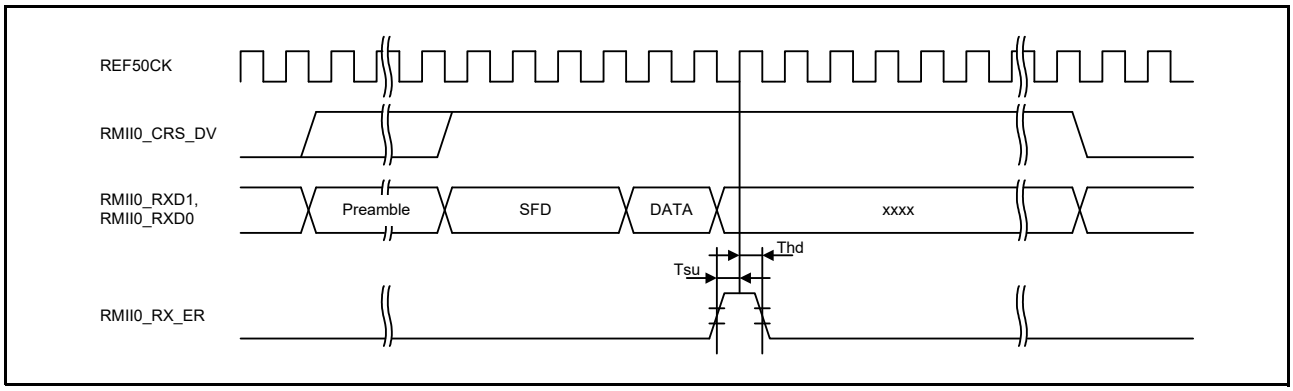


Figure 5.59 RMII Reception Timing (Error Occurrence)

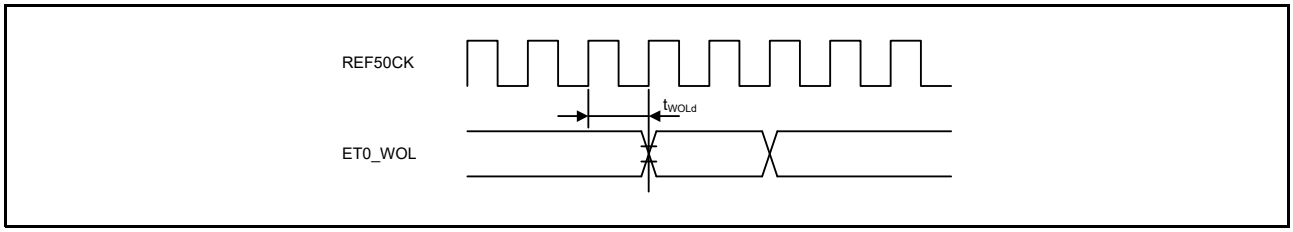


Figure 5.60 WOL Output Timing (RMII)

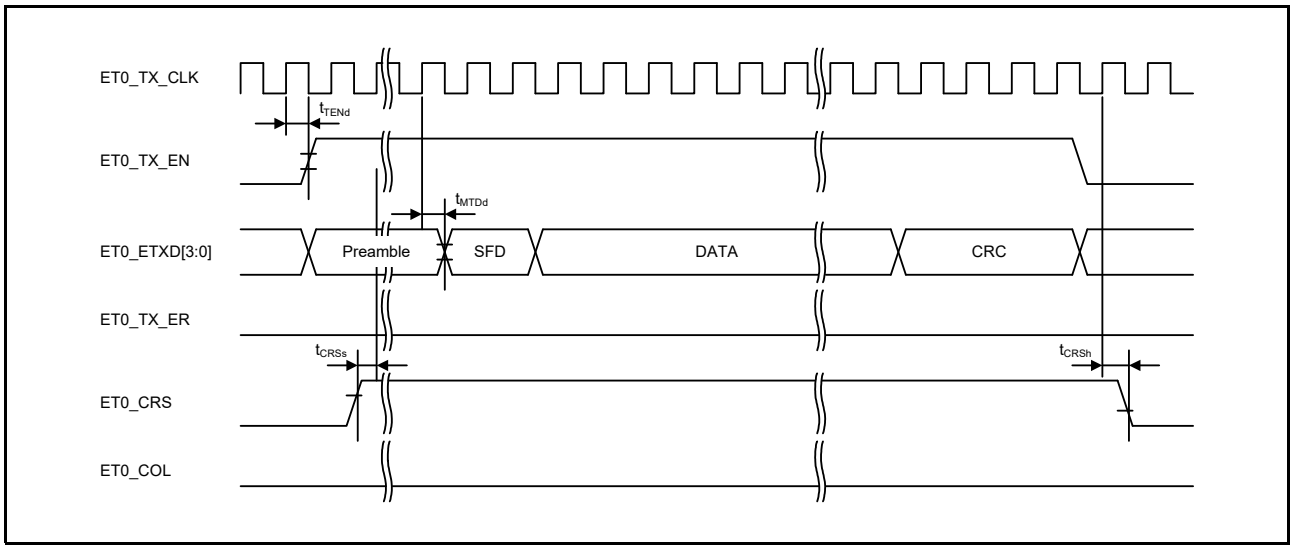


Figure 5.61 MII Transmission Timing (Normal Operation)

5.5 A/D Conversion Characteristics

Table 5.46 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	1.6 (0.4 + 0.25) *2	—	—	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error	—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 – 0.25 V
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±3.0	±5.5	LSB	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±1.5	±3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	µs	
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
	Offset error	—	±1.0	±2.5	LSB	
	Full-scale error	—	±1.0	±2.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.5	±4.5	LSB	
	DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
	INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.