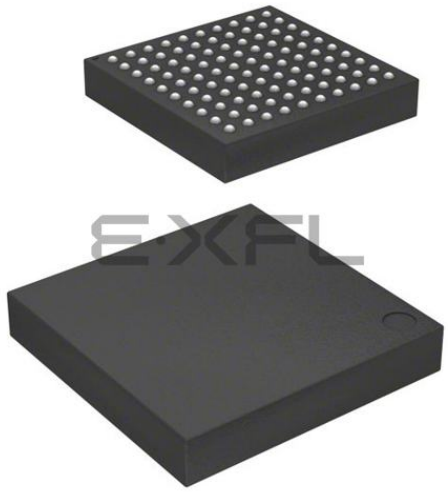
Renesas Electronics America Inc - R5F565N7ADLJ#20 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n7adlj-20

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
	SD host interface (SDHI)*3	• 1 channel • Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
	SD slave interface (SDSI)*3	• 1 channel • Compliant with the SDIO Card Specification Ver.2.00 (CSA is not supported) • 1-bit SD/4-bit SD/SPI mode • SDIO Proprietary command is supported • SD/SPI Mandatory command is supported • Interrupt requests: 6
	MMC host interface (MMCIF)	• 1 channel • Transfer speed: Data transfer mode (30 MB/s), backward compatible mode (25 MB/s) • Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) • Interface for Multimedia Cards (MMCs) • Device buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt • DMA transfer requests: CE_DATA write and CE_DATA read • Support for card detection, boot operation, high priority interrupt (HPI)
	Parallel data capture unit (PDC)	• 1 channel • Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals • Setting of the image size when clipping of the output for a one-frame image is required
	Graphic-LCD controller (GLCDC)	• 1 channel • Various data formats and LCD panels are supported • Superposition of 3 planes (single-color background, graphic 1, graphic 2) • 32- and 16-bpp color data and 8-, 4-, and 1-bit CLUT data formats are supported
	2D drawing engine (DRW2D)	• 1 channel • Vector drawing (straight lines, triangles, and circles) • Bit blitting (with support for filling, copying, stretching, and rotation) • Bus master function for input and output of frame buffer data 32-, 16-, and 8-bit pixel graphics data are supported • Bus master function for input of texture data Input of texture data (32, 24, 16, 8, 4, 2, or 1 bit) are supported. Run length encoding is supported A CLUT is installed and index data can be converted into color data • Two rendering modes are supported (register mode and display list mode) • Performance counting • Interrupts in response to completion of rendering and processing of the display list

Table 1.1 Outline of Specifications (8/9)

Classification	Module/Function	Description
12-bit A/D converter (S12ADFa)		• 12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels) • 12-bit resolution (switchable between 8, 10, and 12 bits) • Conversion time 0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control (only for 3 group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU3, TMR, TPU) trigger, external trigger • Event linking by the ELC
12-bit D/A converter (R12DA)		• 2 channels • 12-bit resolution • Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output) • Buffered output or unbuffered output can be selected. • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ± 1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available

Table 1.3 List of Products (2/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N7ADFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N7BDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N7EDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N7FDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565N4ADFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N4BDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N4EDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N4FDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565NEDDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NEHDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565NCDDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NCHDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565NEDDLC	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NEHDLC	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565NCDDLC	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NCHDLC	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565NEDDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NEHDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565NCDDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NCHDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565N9ADLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N9BDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N9EDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N9FDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565N7ADLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N7BDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N7EDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N7FDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565N4ADLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N4BDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85

Table 1.3 List of Products (7/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F5651EDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F56519ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56519BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56519EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56519FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56517ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56517BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56517EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56517FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56514ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56514BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56514EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56514FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
RX651 (G version)	R5F5651EDGFC	PLQP0176KB-A *1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F5651EHGFC	PLQP0176KB-A *1	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F5651CDGFC	PLQP0176KB-A *1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F5651CHGFC	PLQP0176KB-A *1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F5651EDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F5651EHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F5651CDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F5651CHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F56519AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F56519BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F56519EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F56519FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105
	R5F56517AGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F56517BGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	RXD10 and RXD11	Input	Input pin for received data
	TXD10 and TXD11	Output	Output pin for transmitted data
	CTS10# and CTS11#	Input	Input pin for controlling the start of transmission and reception
	RTS10# and RTS11#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL10 and SSCL11	I/O	Input/output pin for the I^2C clock
	SSDA10 and SSDA11	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	SMISO10 and SMISO11	I/O	Input/output pin for slave transmission of data
	SMOSI10 and SMOSI11	I/O	Input/output pin for master transmission of data
	SS10# and SS11#	Input	Chip-select input pin
I^2C bus interface	SCL0[FM+], SCL1, SCL2, SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1, SDA2, SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

Table 1.4 Pin Functions (5/8)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK0	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.
	RMII0_CRS_DV	Input	Indicate that there are carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode
	RMII0_RX_ER	Input	Indicate an error has occurred during reception of data in RMII mode.
	ET0_CRS	Input	Carrier detection/data reception enable pins
	ET0_RX_DV	Input	Indicate that there are valid receive data on ET0_ERXD3 to ET0_ERXD0.
	ET0_EXOUT	Output	General-purpose external output pins
	ET0_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable pins. Function as signals indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0.
	ET0_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY-LSI of an error during transmission.
	ET0_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timings from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER.
	ET0_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timings to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER.
	ET0_COL	Input	Input collision detection signals.
	ET0_WOL	Output	Receive Magic packets.
	ET0_MDC	Output	Output reference clock signals for information transfer via ET0_MDIO.
	ET0_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.
USB 2.0 host/function module	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB0_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA/ USB0_OVRCURB	Input	USB overcurrent pins
	USB0_VBUS	Input	USB cable connection/disconnection detection input pins
CAN module	CRX0, CRX1, CRX1-DS	Input	Input pins
	CTX0, CTX1	Output	Output pins

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
D14		PE7	D15[A15/D15]/D7[A7/D7]	MTIOC6A/TOC1	MISOB-B	SDHI_WP/MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105
D15		P65	CKE/CS5#						
E1		PJ5		POE8#	CTS2#/RTS2#/SS2#				
E2	EMLE								
E3		PF5						IRQ4	
E4	VSS								
E5 *1	NC								
E12		PE6	D14[A14/D14]/D6[A6/D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/MMC_CD-B	LCD_DATA10-B	IRQ6	AN104
E13	TRDATA0	PG2	D26						
E14	TRDATA1	PG3	D27						
E15		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	VBATT								
F2	VCL								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#				
F4	BSCANP								
F12		P66	DQM0/CS6#	MTIOC7D					
F13	TRSYNC	PG4	D28						
F14		PA0	DQM2/BC0#/A0	MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF	ET0_TX_EN/RMII0_TXD_EN/SSLA1-B		LCD_DATA8-B		
F15	VSS								
G1	XCIN								
G2	XCOUT								
G3	MD/FINED								
G4	TRST#	PF4							
G12	TRCLK	PG5	D29						
G13	TRDATA2	PG6	D30						
G14		PA1	DQM3/A1	MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17	ET0_WOL/SCK5/SSLA2-B		LCD_DATA7-B	IRQ11	
G15	VCC								
H1	XTAL	P37							
H2	VSS								
H3	RES#								
H4	UPSEL	P35						NMI	
H12		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B		LCD_DATA4-B	IRQ5-DS	

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (1/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
1	AVSS0								
2		P05						IRQ13	DA1
3	AVCC1								
4		P03						IRQ11	DA0
5	AVSS1								
6		P02		TMCI1	SCK6			IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/ SSCL6			IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6			IRQ8	AN118
9		PF5						IRQ4	
10	EMLE								
11		PJ5		POE8#	CTS2#/RTS2#/ SS2#				
12	VSS								
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
14	VCL								
15	VBATT								
16	NC								
17	TRST#	PF4							
18	MD/FINED								
19	XCIN								
20	XCOUT								
21	RES#								
22	XTAL	P37							
23	VSS								
24	EXTAL	P36							
25	VCC								
26	UPSEL	P35						NMI	
27		P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
28		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0	PCKO		IRQ3-DS	
29		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC		IRQ2-DS	
30	TMS	PF3							
31	TDI	PF2			RXD1/SMISO1/ SSCL1				

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (6/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
110		PE1	D9[A9/D9]/ D1[A1/D1]*1	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B*1		ANEX1
111		PE0	D8[A8/D8]/ D0[A0/D0]*1	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B*1		ANEX0
112		P64	WE#/D3[A3/ D3]*1/CS4#						
113		P63	CAS#/ D2[A2/D2]*1/ CS3#						
114		P62	RAS#/ D1[A1/D1]*1/ CS2#						
115		P61	SDCS#/ D0[A0/D0]*1/ CS1#						
116	VSS								
117		P60	CS0#						
118	VCC								
119		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DATA17-B*1	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B*1	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B*1	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B*1	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DATA21-B*1	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2-B/MMC_D2-B	LCD_DATA22-B*1	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B*1	IRQ1	AN109
126		PD0	D0[A0/D0]	POE4#			LCD_EXTCLK-B*1	IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/ SS7#				AN117
128		P92	A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
129		P91	A17		SCK7				AN115
130	VSS								
131		P90	A16		TXD7/SMOSI7/ SSDA7				AN114
132	VCC								
133		P47						IRQ15-DS	AN007
134		P46						IRQ14-DS	AN006
135		P45						IRQ13-DS	AN005

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

(5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

Table 4.1 List of I/O Registers (Address Order) (11 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 77BCh	ICU	Software Configurable Interrupt B Source Select Register 188	SLIBR188	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BDh	ICU	Software Configurable Interrupt B Source Select Register 189	SLIBR189	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BEh	ICU	Software Configurable Interrupt B Source Select Register 190	SLIBR190	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BFh	ICU	Software Configurable Interrupt B Source Select Register 191	SLIBR191	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C0h	ICU	Software Configurable Interrupt B Source Select Register 192	SLIBR192	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C1h	ICU	Software Configurable Interrupt B Source Select Register 193	SLIBR193	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C2h	ICU	Software Configurable Interrupt B Source Select Register 194	SLIBR194	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C3h	ICU	Software Configurable Interrupt B Source Select Register 195	SLIBR195	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C4h	ICU	Software Configurable Interrupt B Source Select Register 196	SLIBR196	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C5h	ICU	Software Configurable Interrupt B Source Select Register 197	SLIBR197	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C6h	ICU	Software Configurable Interrupt B Source Select Register 198	SLIBR198	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C7h	ICU	Software Configurable Interrupt B Source Select Register 199	SLIBR199	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C8h	ICU	Software Configurable Interrupt B Source Select Register 200	SLIBR200	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C9h	ICU	Software Configurable Interrupt B Source Select Register 201	SLIBR201	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CAh	ICU	Software Configurable Interrupt B Source Select Register 202	SLIBR202	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CBh	ICU	Software Configurable Interrupt B Source Select Register 203	SLIBR203	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CCh	ICU	Software Configurable Interrupt B Source Select Register 204	SLIBR204	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CDh	ICU	Software Configurable Interrupt B Source Select Register 205	SLIBR205	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CEh	ICU	Software Configurable Interrupt B Source Select Register 206	SLIBR206	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CFh	ICU	Software Configurable Interrupt B Source Select Register 207	SLIBR207	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7830h	ICU	Group AL0 Interrupt Request Register	GRPAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7834h	ICU	Group AL1 Interrupt Request Register	GRPAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7870h	ICU	Group AL0 Interrupt Request Enable Register	GENAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7874h	ICU	Group AL1 Interrupt Request Enable Register	GENAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7900h	ICU	Software Configurable Interrupt A Request Register 0	PIAR0	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7901h	ICU	Software Configurable Interrupt A Request Register 1	PIAR1	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7902h	ICU	Software Configurable Interrupt A Request Register 2	PIAR2	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7903h	ICU	Software Configurable Interrupt A Request Register 3	PIAR3	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7904h	ICU	Software Configurable Interrupt A Request Register 4	PIAR4	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7905h	ICU	Software Configurable Interrupt A Request Register 5	PIAR5	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 790Bh	ICU	Software Configurable Interrupt A Request Register B	PIARB	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D0h	ICU	Software Configurable Interrupt A Source Select Register 208	SLIAR208	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D1h	ICU	Software Configurable Interrupt A Source Select Register 209	SLIAR209	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (17 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8320h	RIIC1	I²C-bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8321h	RIIC1	I²C-bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8322h	RIIC1	I²C-bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8323h	RIIC1	I²C-bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8324h	RIIC1	I²C-bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8325h	RIIC1	I²C-bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8326h	RIIC1	I²C-bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8327h	RIIC1	I²C-bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8328h	RIIC1	I²C-bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8329h	RIIC1	I²C-bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8330h	RIIC1	I²C-bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8331h	RIIC1	I²C-bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8332h	RIIC1	I²C-bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8333h	RIIC1	I²C-bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8340h	RIIC2	I²C-bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8341h	RIIC2	I²C-bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8342h	RIIC2	I²C-bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8343h	RIIC2	I²C-bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8344h	RIIC2	I²C-bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8345h	RIIC2	I²C-bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8346h	RIIC2	I²C-bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8347h	RIIC2	I²C-bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8348h	RIIC2	I²C-bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8349h	RIIC2	I²C-bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ah	RIIC2	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Bh	RIIC2	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ch	RIIC2	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Dh	RIIC2	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Eh	RIIC2	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Fh	RIIC2	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8350h	RIIC2	I²C-bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8351h	RIIC2	I²C-bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8352h	RIIC2	I²C-bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8353h	RIIC2	I²C-bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8500h	MMCIF	Command Setting Register	CECMDSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8508h	MMCIF	Argument Register	CEARG	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 850Ch	MMCIF	Automatically Issued CMD12 Argument Register	CEARGCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8510h	MMCIF	Command Control Register	CECMDCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8514h	MMCIF	Transfer Block Setting Register	CEBLOCKSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8518h	MMCIF	Clock Control Register	CECLKCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 851Ch	MMCIF	Buffer Access Setting Register	CEBUFACC	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8520h	MMCIF	Response Register 3	CERESP3	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8524h	MMCIF	Response Register 2	CERESP2	32	32	2, 3 PCLKB	2 ICLK	MMCIF

Table 4.1 List of I/O Registers (Address Order) (23 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A006h	SMCI0	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Eh	SCI0	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Fh	SCI0	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A00Eh	SCI0	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A010h	SCI0	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A011h	SCI0	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A010h	SCI0	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A012h	SCI0	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (29 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E0h	SCI7	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E1h	SCI7	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E2h	SCI7	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E3h	SCI7	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E4h	SCI7	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E5h	SCI7	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E6h	SMCI7	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E7h	SCI7	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E8h	SCI7	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0E9h	SCI7	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EAh	SCI7	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EBh	SCI7	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0ECh	SCI7	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EDh	SCI7	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EEh	SCI7	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0EFh	SCI7	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 5.8 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}	—	—	3.8	mA
	All output pins*3	High-speed interface high-drive	I_{OL}	—	—	7.5	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}	—	—	7.6	mA
	All output pins*3	High-speed interface high-drive	I_{OL}	—	—	15	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–3.8	mA
	All output pins*3	High-speed interface high-drive	I_{OH}	—	—	–7.5	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–7.6	mA
	All output pins*3	High-speed interface high-drive	I_{OH}	—	—	–15	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

Table 5.9 Heat Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Heat resistance	176-pin LFQFP (PLQP0176KB-A)	θ_{ja}	48.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		50.9		
	100-pin LFQFP (PLQP0100KB-B)		52.5		
	177-pin TFLGA (PTLG0177KA-A)		36.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		35.4		
	145-pin TFLGA (PTLG0145KA-A)		34.6		
	100-pin TFLGA (PTLG0100JA-A)		34.1		
	176-pin LFQFP (PLQP0176KB-A)	Ψ_{jt}	1.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		1.5		
	100-pin LFQFP (PLQP0100KB-B)		1.5		
	177-pin TFLGA (PTLG0177KA-A)		0.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		0.3		
	145-pin TFLGA (PTLG0145KA-A)		0.4		
	100-pin TFLGA (PTLG0100JA-A)		0.4		

Note: The values are reference values when the 4-layer board is used. Heat resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

5.3.1 Reset Timing

Table 5.13 Reset Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	1	—	—	ms	Figure 5.1
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 5.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	54	—	55	t_{Lcyc}	Figure 5.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	100	—	108	t_{Lcyc}	

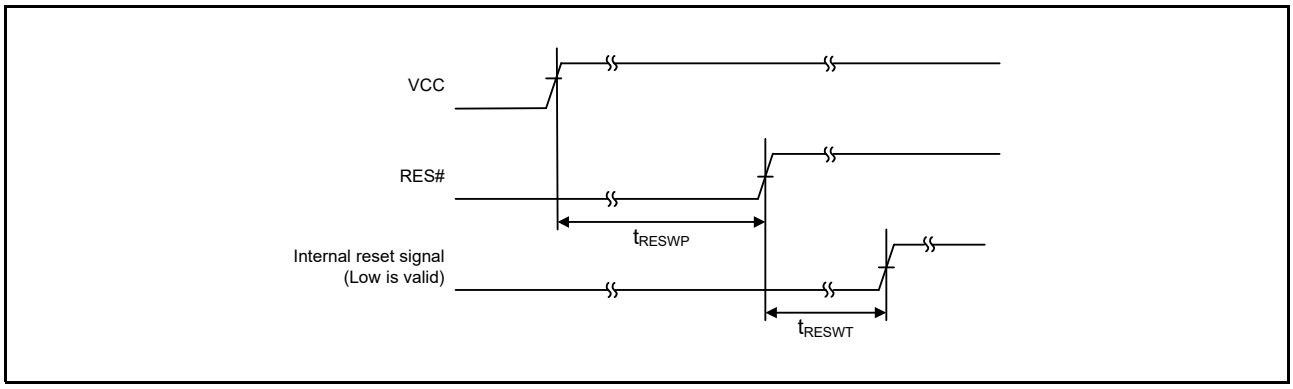

Figure 5.1 Reset Input Timing at Power-On

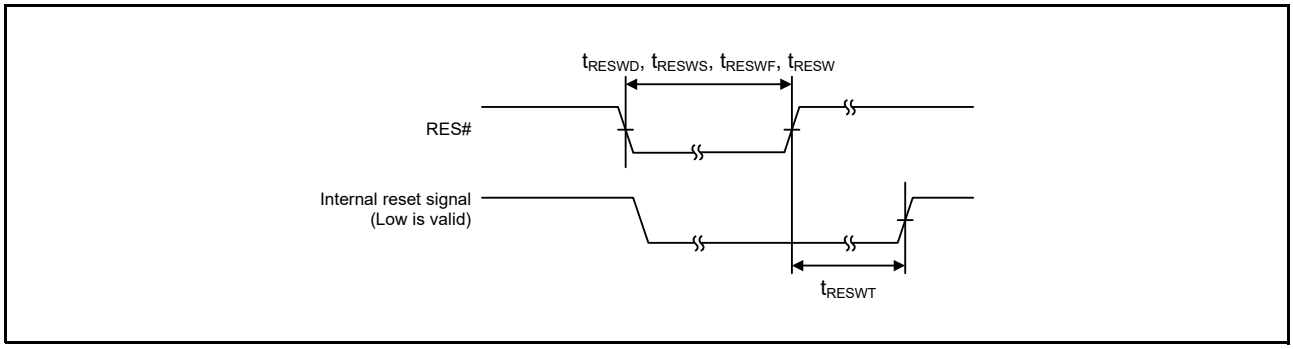

Figure 5.2 Reset Input Timing

Table 5.17 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.63	4.16	3.78	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 5.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	9.26	8.33	7.57	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 5.7

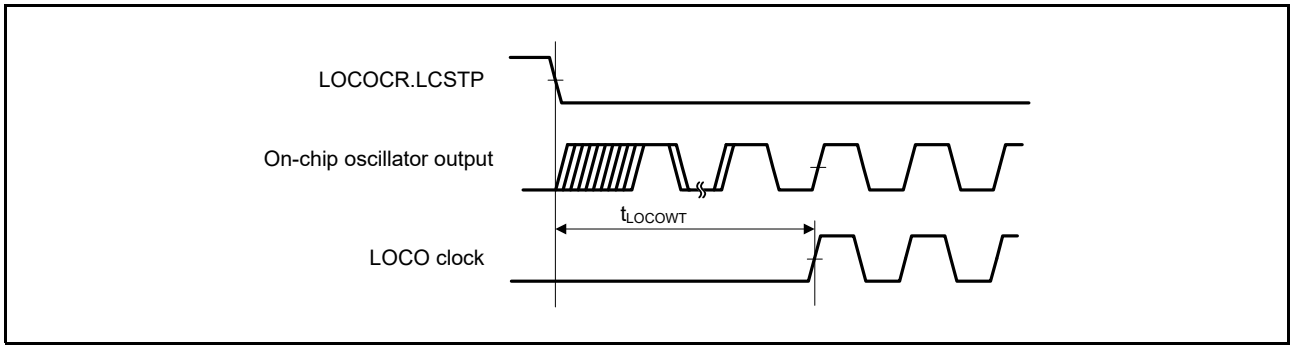

Figure 5.6 LOCO Clock Oscillation Start Timing

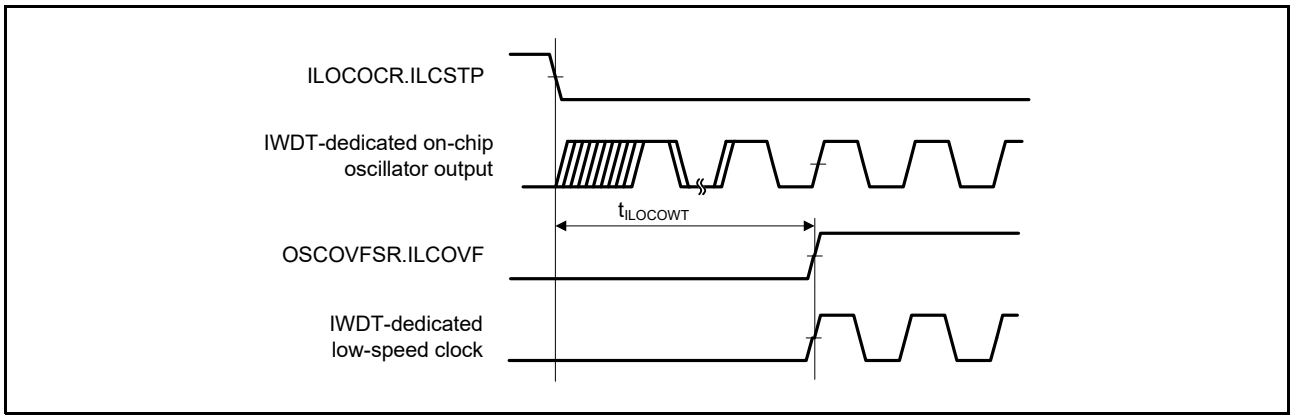

Figure 5.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 5.28 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 5.36
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

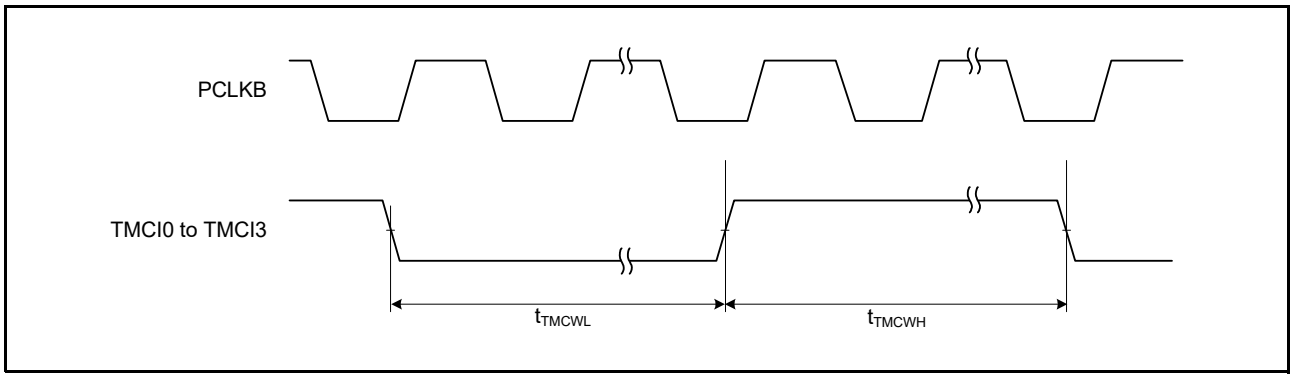

Figure 5.36 TMR Clock Input Timing

Table 5.29 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 5.37
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

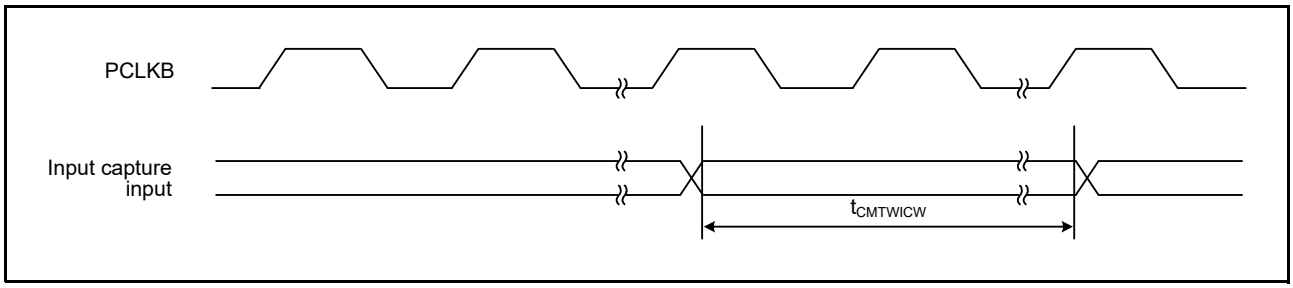

Figure 5.37 CMTW Input Capture Input Timing

5.11 Flash Memory Characteristics

Table 5.54 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N_{PEC} ≤ 100 times	128 bytes	t_{P128}	—	0.75	13.2	—	0.38	6.6	—	0.34	6	ms
	8 Kbytes	t_{P8K}	—	49	176	—	25	88	—	22	80	ms
	32 Kbytes	t_{P32K}	—	194	704	—	97	352	—	88	320	ms
Programming time N_{PEC} > 100 times	128 bytes	t_{P128}	—	0.91	15.8	—	0.46	8	—	0.41	7.2	ms
	8 Kbytes	t_{P8K}	—	60	212	—	30	106	—	27	96	ms
	32 Kbytes	t_{P32K}	—	234	848	—	117	424	—	106	384	ms
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	78	216	—	48	132	—	43	120	ms
	32 Kbytes	t_{E32K}	—	283	864	—	173	528	—	157	480	ms
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	94	260	—	58	158	—	52	144	ms
	32 Kbytes	t_{E32K}	—	341	1040	—	208	632	—	189	576	ms
Reprogramming/erasure cycle*1		N_{PEC}	10000 *2	—	—	10000 *2	—	—	10000 *2	—	—	Times
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	132	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	132	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	—	—	1.7	ms
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs
Data hold time*3		t_{DRP}	10	—	—	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

REVISION HISTORY	RX65N Group, RX651 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Aug 24, 2016	—	First edition, issued	
2.10	Oct 02, 2017	—	Products with at least 1.5 Mbytes of code flash memory added The conventional products indicated as “products with 1 Mbyte of code flash memory or less”	
		1. Overview		
		6, 9	Table 1.1 Outline of Specifications (5/9), Note added	TN-RX*-A164B/E
		8	Table 1.1 Outline of Specifications (8/9) Description of the 12-bit D/A converter (R12DA) changed	TN-RX*-A165A/E
		4. I/O Registers		
		131	Table 4.1 List of I/O Registers (Address Order) (46 / 61), changed	TN-RX*-A176A/E
		5. Electrical Characteristics		
		147	Table 5.1 Absolute Maximum Rating, changed	
		150	Table 5.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less), changed	TN-RX*-A164B/E
		152	Table 5.7 DC Characteristics (4), changed	TN-RX*-A164B/E TN-RX*-A176A/E
		153	Table 5.9 Heat Resistance Value (Reference), added	
		162	Table 5.21 Timing of Recovery from Low Power Consumption Modes (1), changed	TN-RX*-A176A/E
		189	Table 5.35 RSPI Timing, changed	
		212	Table 5.49 D/A Conversion Characteristics, changed	TN-RX*-A165A/E
		218	Table 5.54 Code Flash Memory Characteristics, changed	
		219	Table 5.55 Data Flash Memory Characteristics, changed	