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Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n7bdfp-30

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Timers	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)*4	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
Communication function	Ethernet controller (ETHERC)	• Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a “wake-on-LAN” signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards
	DMA controller for Ethernet controller (EDMACa)	• Alleviation of CPU load by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 FS host/function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus power are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required

Table 1.3 List of Products (4/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (G version)	R5F565N7AGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N7BGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N7EGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N7FGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105
	R5F565N4AGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N4BGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N4EGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N4FGFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105
	R5F565NEDGFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565N9AGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N9BGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N9EGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N9FGFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105
	R5F565N7AGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N7BGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N7EGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N7FGFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105
	R5F565N4AGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N4BGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N4EGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N4FGFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105



Figure 1.1 How to Read the Product Part Number

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock
	SSDA12	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	RXD10 and RXD11	Input	Input pin for received data
	TXD10 and TXD11	Output	Output pin for transmitted data
	CTS10# and CTS11#	Input	Input pin for controlling the start of transmission and reception
	RTS10# and RTS11#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL10 and SSCL11	I/O	Input/output pin for the I ² C clock
	SSDA10 and SSDA11	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	SMISO10 and SMISO11	I/O	Input/output pin for slave transmission of data
	SMOSI10 and SMOSI11	I/O	Input/output pin for master transmission of data
	SS10# and SS11#	Input	Chip-select input pin
I ² C bus interface	SCL0[FM+], SCL1, SCL2, SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1, SDA2, SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R		
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15	
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14	
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13	
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12	
11	PD6	PG1	VCC	P61	RX65N Group, RX651 Group PTLG0177KA-A (177-Pin TFLGA) (Upper Perspective View)							P81	P82	PC6	VCC	11	
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10	
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9	
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8	
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7	
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_ USB	USB0_ DP	6	
5	P46	P47	P45	P44	NC								PJ2	P12	VCC_ USB	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4	
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3	
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2	
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R		

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61	RX65N Group, RX651 Group PTBG0176GA-A (176-Pin LFBGA) (Upper Perspective View)							P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_USB	USB0_DP	6
5	P46	P47	P45	P44								PJ2	P12	VCC_USB	USB0_DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX65N Group, RX651 Group PTLG0145KA-A (145-Pin TFLGA) (Upper Perspective View)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	AVCC1	AVSS1	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
B15		PE3	D11[A11/ D11]/D3[A3/ D3]	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#/SS12#	MMC_D7-B	LCD_DA TA13-B		AN101
C1	AVSS1								
C2	AVCC1								
C3	VREFH0								
C4		P43						IRQ11- DS	AN003
C5		P45						IRQ13- DS	AN005
C6		P90	D16/A16		TXD7/SMOSI7/ SSDA7				AN114
C7		PD0	D0[A0/D0]	POE4#			LCD_EX TCLK-B	IRQ0	AN108
C8		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2- B/MMC_D2-B	LCD_DA TA22-B	IRQ2	AN110
C9		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3- B/MMC_D3-B	LCD_DA TA21-B	IRQ3	AN111
C10	TRDATA6	PG0	D24						
C11	VCC								
C12		P62	RAS#/ D1[A1/D1]/ CS2#						
C13		PE4	D12[A12/ D12]/D4[A4/ D4]	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DA TA12-B		AN102
C14	VSS								
C15		P70	SDCLK						
D1		P01		TMC10	RXD6/SMISO6/ SSCL6			IRQ9	AN119
D2		P02		TMC11	SCK6			IRQ10	AN120
D3		P03						IRQ11	DA0
D4		P00		TMR10	TXD6/SMOSI6/ SSDA6			IRQ8	AN118
D5		P44						IRQ12- DS	AN004
D6		P93	D19/A19	POE0#	CTS7#/RTS7#/ SS7#				AN117
D7	TRDATA4	P95	D21/A21						
D8	VSS								
D9		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DA TA19-B	IRQ5	AN113
D10		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DA TA17-B	IRQ7	AN107
D11		P61	SDCS#/ D0[A0/D0]/ CS1#						
D12		PE5	D13[A13/ D13]/D5[A5/ D5]	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DA TA11-B	IRQ5	AN103
D13	VCC								

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (2/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
32		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
33		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
34	TCK	PF1			SCK1				
35	TDO	PF0			TXD1/SMOSI1/ SSDA1				
36		P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB- A				
37		P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
38		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0 #
39	VCC								
40		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
41	VSS								
42		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C/PIXD7			
43		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C/PIXD6			
44		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN	SDHI_CLK-C/ PIXD5		IRQ9	
45		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID	SDHI_CMD-C/ PIXD4		IRQ8	
46		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C/PIXD3		IRQ7	ADTRG1 #
47		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C/PIXD2			
48		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
49		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
50		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)

Pin Number				Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDI, MMCIF, PDC)			
145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC				GLCDC	Interrupt	A/D D/A
E4	EMLE								
E5		P44						IRQ12- DS	AN004
E10		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DA TA8-B*1		
E11		P66	DQM0/CS6#	MTIOC7D					
E12		P65	CKE/CS5#						
E13		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	XCIN								
F2	XCOUT								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
F4	VBATT								
F10		PA3	A3	MTIOC0D/ MTCLKD/ TIOC0D/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DA TA5-B*1	IRQ6-DS	
F11	VSS								
F12		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DA TA7-B*1	IRQ11	
F13		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DA TA6-B*1		
G1	XTAL	P37							
G2	RES#								
G3	MD/FINED								
G4	BSCANP								
G10		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DA TA3-B*1		
G11		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DA TA2-B*1		
G12	VCC								
G13		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DA TA4-B*1	IRQ5-DS	
H1	EXTAL	P36							
H2	VCC								
H3	VSS								
H4	UPSEL	P35						NMI	
H10		P72	A19/CS2#		ET0_MDC				
H11		P71	A18/CS1#		ET0_MDIO				

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface			
145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCI, RSPI, RIIC, CAN, USB)	(QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
L11		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A			
L12	TRDATA4	P73	CS3#	PO16	ET0_WOL				
L13	VSS								
M1		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C*1/ PIXD6			
M2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C*1/ PIXD3		IRQ7	ADTRG1 #
M3		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
M4		P12		TMC11	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
M5	VCC_USB								
M6	VSS_USB								
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
M8		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMC12/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A		IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A			
M10	TRDATA7	P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A			
M11		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
M12		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
M13	VCC								
N1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN	SDHI_CLK-C*1/ PIXD5		IRQ9	
N2		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID	SDHI_CMD-C*1/ PIXD4		IRQ8	
N3		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C*1/ PIXD2			
N4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
N5					USB0_DM				
N6					USB0_DP				

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
J6	VCC_USB								
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
J8		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMC11/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A				
J9		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
J10		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
K1		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOC3D/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#				
K2		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B				
K3		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID			IRQ8	
K4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
K5					USB0_DM				
K6					USB0_DP				
K7		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
K8		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A				
K9		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5				
K10		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A				

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (2/5)

Pin Number				Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC						
26		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B				
27		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN			IRQ9	
28		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID			IRQ8	
29		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS			IRQ7	ADTRG1 #
30		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOU	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
31		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS			IRQ5	
32		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
33		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1 #
34		P12		TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
35	VCC_USB								
36					USB0_DM				
37					USB0_DP				
38	VSS_USB								
39		P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ CRX1			IRQ10	
40		P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
41		P53*2	BCLK						
42		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
43		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				

Table 4.1 List of I/O Registers (Address Order) (14 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8040h	DA	D/A Data Register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	R12DA
0008 8042h	DA	D/A Data Register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK	R12DA
0008 8044h	DA	D/A Control Register	DACR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8045h	DA	DADRm Format Select Register	DADPR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8046h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8048h	DA	D/A Output Amplifier Control Register	DAAMPCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 805Ch	DA	D/A Output Amplifier Stabilization Wait Control Register	DAASWCR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0008 8100h	TPUA	Timer Start Register	TSTR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8101h	TPUA	Timer Synchronous Register	TSYR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8111h	TPU0	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8112h	TPU0	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8113h	TPU0	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8114h	TPU0	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8115h	TPU0	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8116h	TPU0	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8118h	TPU0	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa

Table 4.1 List of I/O Registers (Address Order) (22 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 91E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E4h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E5h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E6h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E7h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E8h	S12AD1	A/D Sampling State Register 8	ADSSTR8	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E9h	S12AD1	A/D Sampling State Register 9	ADSSTR9	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EAh	S12AD1	A/D Sampling State Register 10	ADSSTR10	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EBh	S12AD1	A/D Sampling State Register 11	ADSSTR11	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91ECh	S12AD1	A/D Sampling State Register 12	ADSSTR12	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EDh	S12AD1	A/D Sampling State Register 13	ADSSTR13	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EEh	S12AD1	A/D Sampling State Register 14	ADSSTR14	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EFh	S12AD1	A/D Sampling State Register 15	ADSSTR15	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Set Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E24h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 2	SPBMUL2	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E28h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 3	SPBMUL3	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 A000h	SCIO	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, SCli
0008 A001h	SCIO	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (31 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A126h	SMCI9	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A129h	SCI9	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A12Ah	SCI9	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A12Bh	SCI9	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A12Ch	SCI9	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A131h	SCI9	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i

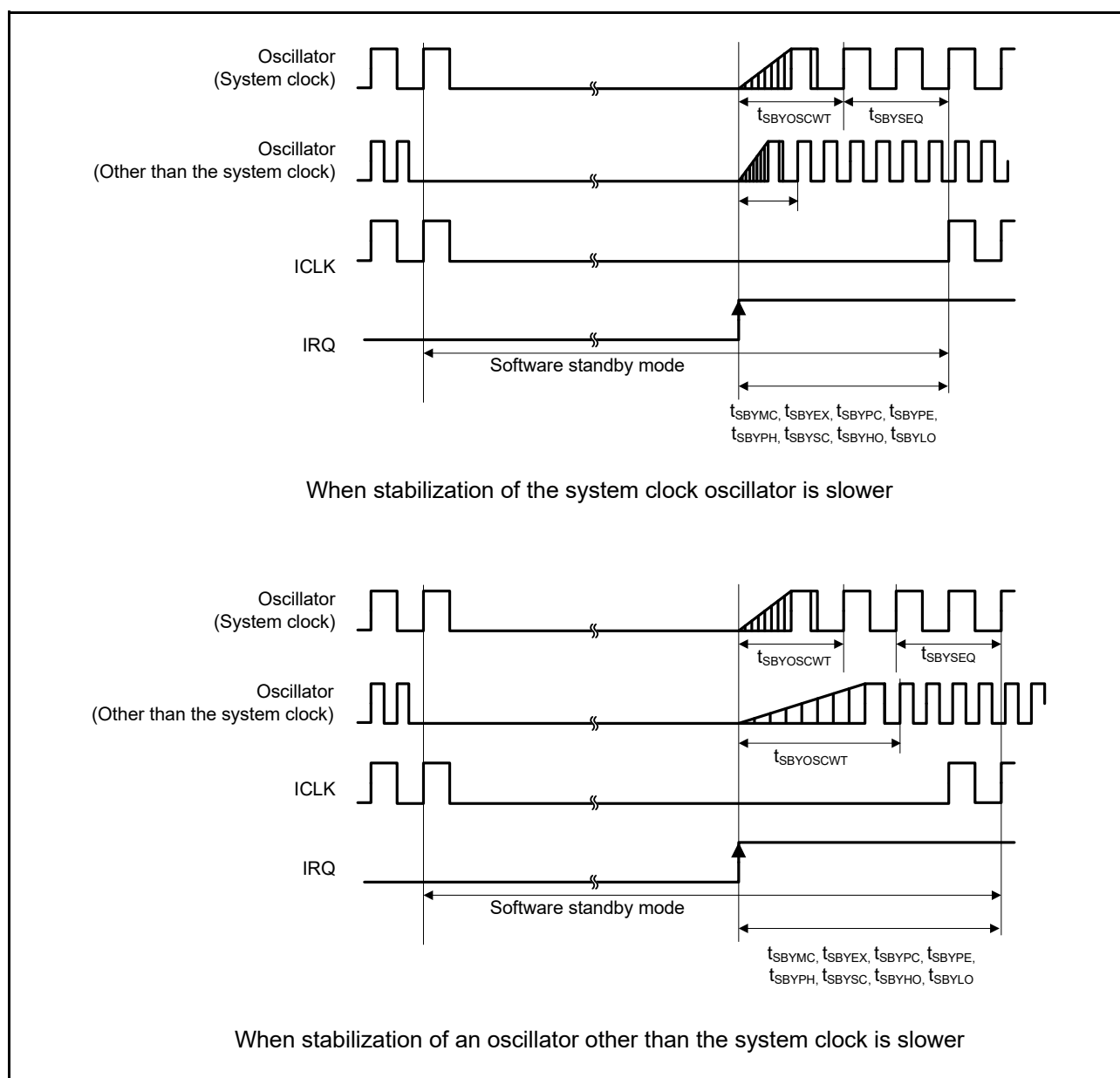


Figure 5.12 Software Standby Mode Cancellation Timing

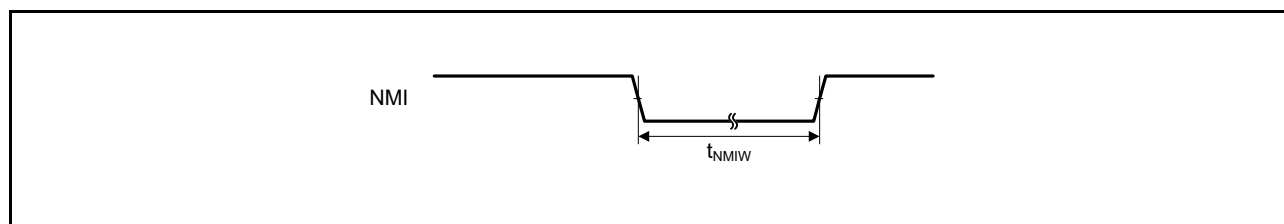
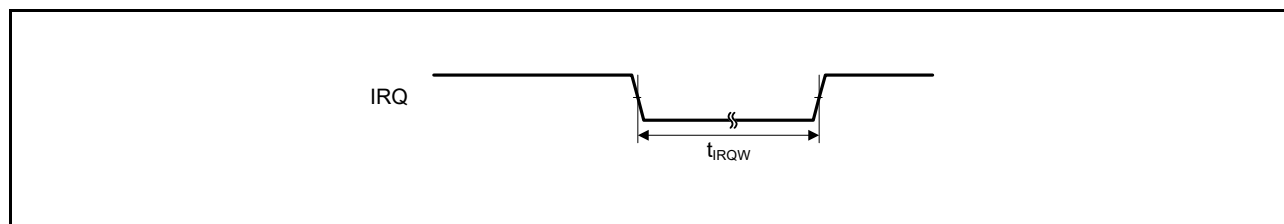
5.3.4 Control Signal Timing

Table 5.23 Control Signal Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.14
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 5.14
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.15
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 5.15

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.14 NMI Interrupt Input Timing****Figure 5.15 IRQ Interrupt Input Timing**

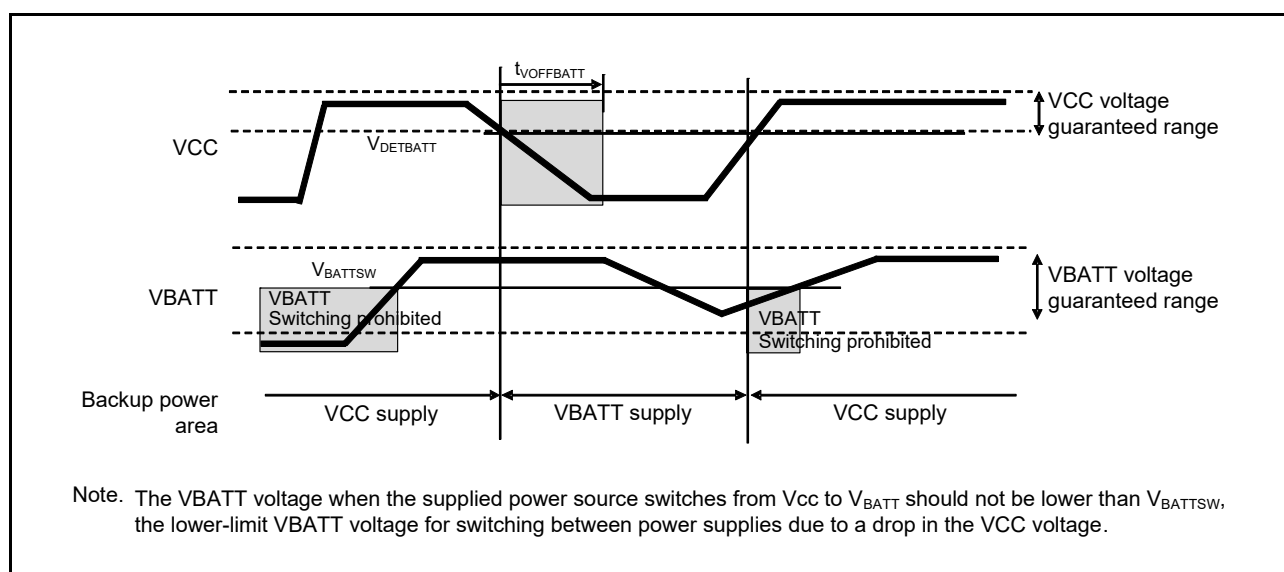
5.10 Battery Backup Function Characteristics

Table 5.53 Battery Backup Function Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $V_{BATT} = 2.0$ to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 5.81
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	μ s	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

**Figure 5.81 Battery Backup Function Characteristics**

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

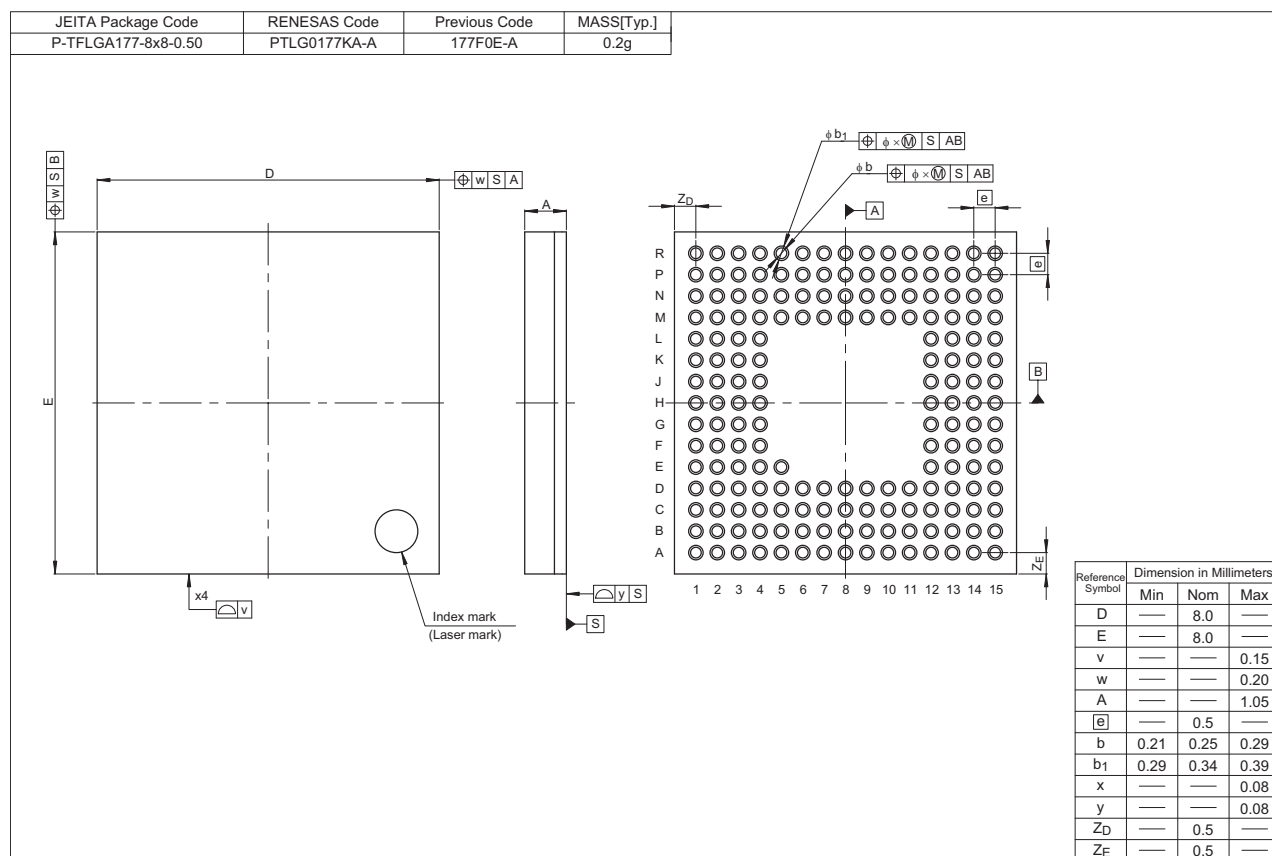


Figure A 177-Pin TFLGA (PTLG0177KA-A)