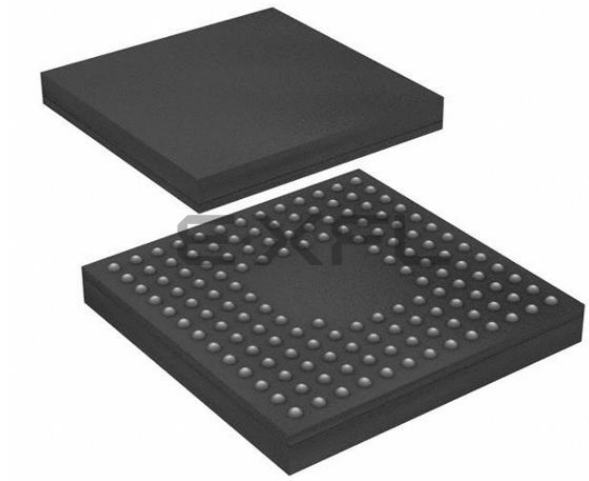
# Renesas Electronics America Inc - R5F565N7BDLK#20 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 111 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 29x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 145-TFLGA |
| Supplier Device Package | 145-TFLGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n7bdlk-20 |

## 1.4 Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4 Pin Functions (1/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Digital power supply | VCC | Input | Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VCL | Input | Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VBATT | Input | Backup power pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the SDRAM-dedicated clock. |
| | XCOUT | Output | Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| Clock frequency accuracy measurement | CACREF | Input | Reference clock input pin for the clock frequency accuracy measurement circuit |
| Operating mode control | MD | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| | UB | Input | USB boot mode enable pin |
| | UPSEL | Input | Selects the power supply method in USB boot mode.<br>The low level selects self-power mode and the high level selects bus power mode. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| On-chip emulator | FINED | I/O | Fine interface pin |
| | TRST# | Input | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC<br>TRSYNC1 | Output | This pin indicates that output from the TRDATA0 to TRDATA7 pins is valid. |
| | TRDATA0<br>TRDATA1<br>TRDATA2<br>TRDATA3<br>TRDATA4<br>TRDATA5<br>TRDATA6<br>TRDATA7 | Output | These pins output the trace information. |
| Address bus | A0 to A23 | Output | Output pins for the address |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| D14 | | PE7 | D15[A15/D15]/D7[A7/D7] | MTIOC6A/TOC1 | MISOB-B | SDHI_WP/MMC_RES#-B | LCD_DATA9-B | IRQ7 | AN105 |
| D15 | | P65 | CKE/CS5# | | | | | | |
| E1 | | PJ5 | | POE8# | CTS2#/RTS2#/SS2# | | | | |
| E2 | EMLE | | | | | | | | |
| E3 | | PF5 | | | | | | IRQ4 | |
| E4 | VSS | | | | | | | | |
| E5 *1 | NC | | | | | | | | |
| E12 | | PE6 | D14[A14/D14]/D6[A6/D6] | MTIOC6C/TIC1 | MOSIB-B | SDHI_CD/MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| E13 | TRDATA0 | PG2 | D26 | | | | | | |
| E14 | TRDATA1 | PG3 | D27 | | | | | | |
| E15 | | P67 | DQM1/CS7# | MTIOC7C | | | | IRQ15 | |
| F1 | VBATT | | | | | | | | |
| F2 | VCL | | | | | | | | |
| F3 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0# | | | | |
| F4 | BSCANP | | | | | | | | |
| F12 | | P66 | DQM0/CS6# | MTIOC7D | | | | | |
| F13 | TRSYNC | PG4 | D28 | | | | | | |
| F14 | | PA0 | DQM2/BC0#/A0 | MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF | ET0_TX_EN/RMII0_TXD_EN/SSLA1-B | | LCD_DATA8-B | | |
| F15 | VSS | | | | | | | | |
| G1 | XCIN | | | | | | | | |
| G2 | XCOUT | | | | | | | | |
| G3 | MD/FINED | | | | | | | | |
| G4 | TRST# | PF4 | | | | | | | |
| G12 | TRCLK | PG5 | D29 | | | | | | |
| G13 | TRDATA2 | PG6 | D30 | | | | | | |
| G14 | | PA1 | DQM3/A1 | MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17 | ET0_WOL/SCK5/SSLA2-B | | LCD_DATA7-B | IRQ11 | |
| G15 | VCC | | | | | | | | |
| H1 | XTAL | P37 | | | | | | | |
| H2 | VSS | | | | | | | | |
| H3 | RES# | | | | | | | | |
| H4 | UPSEL | P35 | | | | | | NMI | |
| H12 | | PA4 | A4 | MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20 | ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B | | LCD_DATA4-B | IRQ5-DS | |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (8/8)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| R9 | | P53*2 | BCLK | | | | | | |
| R10 | VSS | | | | | | | | |
| R11 | VCC | | | | | | | | |
| R12 | | P80 | EDREQ0 | MTIOC3B/ PO26 | ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10# | QIO2-A/SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| R13 | | P76 | CS6# | PO22 | ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11 | QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| R14 | | P74 | A20/CS4# | PO19 | ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11# | | LCD_DATA21-A | | |
| R15 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | LCD_DATA22-A | IRQ12 | |

Note 1. The 176-pin LFBGA does not include the E5 pin.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (4/8)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 74 | | P83 | EDACK1 | MTIOC4C | ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10# | | LCD_DATA8-A | | |
| 75 | VCC | | | | | | | | |
| 76 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | MMC_D7-A | LCD_DATA9-A | IRQ14 | |
| 77 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | MMC_D6-A | LCD_DATA10-A | IRQ13 | |
| 78 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | MMC_D5-A | LCD_DATA11-A | | |
| 79 | | P82 | EDREQ1 | MTIOC4A/ PO28 | ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10 | MMC_D4-A | LCD_DATA12-A | | |
| 80 | | P81 | EDACK0 | MTIOC3D/ PO27 | ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10 | QIO3-A/SDHI_CD/ MMC_D3-A | LCD_DATA13-A | | |
| 81 | | P80 | EDREQ0 | MTIOC3B/ PO26 | ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10# | QIO2-A/SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| 82 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A | LCD_DATA15-A | | |
| 83 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A | LCD_DATA16-A | | |
| 84 | | P77 | CS7# | PO23 | ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11 | QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A | LCD_DATA17-A | | |
| 85 | | P76 | CS6# | PO22 | ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11 | QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| 86 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A | LCD_DATA19-A | | |
| 87 | | P75 | CS5# | PO20 | ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11# | SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A | LCD_DATA20-A | | |
| 88 | | P74 | A20/CS4# | PO19 | ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11# | | LCD_DATA21-A | | |
| 89 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | LCD_DATA22-A | IRQ12 | |
| 90 | VCC | | | | | | | | |
| 91 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |

**Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/5)**

| Pin Number 100-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| H1 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| H2 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | | | | ADTRG0# |
| H3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | IRQ6 | ADTRG0# |
| H4 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS | | | IRQ5 | |
| H5 | | P55 | D0[A0/D0]*1/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | ET0_EXOUT/ CRX1 | | | IRQ10 | |
| H6 | | P54 | ALE/D1[A1/ D1]*1/ EDACK0 | MTIOC4B/ TMCI1 | ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1 | | | | |
| H7 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | | | IRQ14 | |
| H8 | | PC6 | D2[A2/D2]*1/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | | | IRQ13 | |
| H9 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| H10 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |
| J1 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | | | | |
| J2 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN | | | IRQ9 | |
| J3 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS | | | IRQ7 | ADTRG1# |
| J4 | | P13 | | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/ SDA0[FM+] | | | IRQ3 | ADTRG1# |
| J5 | VSS_USB | | | | | | | | |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (1/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 1 | AVCC1 | | | | | | | | |
| 2 | EMLE | | | | | | | | |
| 3 | AVSS1 | | | | | | | | |
| 4 | | PJ3 | EDACK1 | MTIOC3C | ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0# | | | | |
| 5 | VCL | | | | | | | | |
| 6 | VBATT | | | | | | | | |
| 7 | MD/FINED | | | | | | | | |
| 8 | XCIN | | | | | | | | |
| 9 | XCOUT | | | | | | | | |
| 10 | RES# | | | | | | | | |
| 11 | XTAL | P37 | | | | | | | |
| 12 | VSS | | | | | | | | |
| 13 | EXTAL | P36 | | | | | | | |
| 14 | VCC | | | | | | | | |
| 15 | UPSEL | P35 | | | | | | NMI | |
| 16 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | ET0_LINKSTA/ SCK6/SCK0 | | | IRQ4 | |
| 17 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0 | | | IRQ3-DS | |
| 18 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN | | | IRQ2-DS | |
| 19 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0-A | | | IRQ1-DS | |
| 20 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | RXD1/SMISO1/ SSCL1/MISOB-A | | | IRQ0-DS | |
| 21 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB-A | | | | |
| 22 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A | | | | |
| 23 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3 | | | | ADTRG0# |
| 24 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | SCK3/ USB0_VBUSEN | | | | |
| 25 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0# | | | | |

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB) | Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC) | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|
| 45 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A | | | IRQ14 | |
| 46 | | PC6 | D2[A2/D2]*1/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A | | | IRQ13 | |
| 47 | | PC5 | D3[A3/D3]*1/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A | | | | |
| 48 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A | | | | |
| 49 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | ET0_TX_ER/ TXD5/SMOSI5/ SSDA5 | | | | |
| 50 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A | | | | |
| 51 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | ET0_ERXD2/ SCK5/SSLA2-A | | | IRQ12 | |
| 52 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A | | | IRQ14 | |
| 53 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11 | SDSI_D1-B | | | |
| 54 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11 | SDSI_D0-B | | | |
| 55 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11 | SDSI_CLK-B | LCD_CLK-B*1 | | |
| 56 | | PB4 | A12 | TIOCA4/PO28 | ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11# | SDSI_CMD-B | LCD_TCON0-B*1 | | |
| 57 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | ET0_RX_ER/ RMII0_RX_ER/ SCK6 | SDSI_D3-B | LCD_TCON1-B*1 | | |
| 58 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6# | SDSI_D2-B | LCD_TCON2-B*1 | | |
| 59 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6 | | LCD_TCON3-B*1 | IRQ4-DS | |

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

### (3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

### (4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

### (5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

**Table 4.1 List of I/O Registers (Address Order) (11 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 77BCh | ICU | Software Configurable Interrupt B Source Select Register 188 | SLIBR188 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BDh | ICU | Software Configurable Interrupt B Source Select Register 189 | SLIBR189 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BEh | ICU | Software Configurable Interrupt B Source Select Register 190 | SLIBR190 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77BFh | ICU | Software Configurable Interrupt B Source Select Register 191 | SLIBR191 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C0h | ICU | Software Configurable Interrupt B Source Select Register 192 | SLIBR192 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C1h | ICU | Software Configurable Interrupt B Source Select Register 193 | SLIBR193 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C2h | ICU | Software Configurable Interrupt B Source Select Register 194 | SLIBR194 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C3h | ICU | Software Configurable Interrupt B Source Select Register 195 | SLIBR195 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C4h | ICU | Software Configurable Interrupt B Source Select Register 196 | SLIBR196 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C5h | ICU | Software Configurable Interrupt B Source Select Register 197 | SLIBR197 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C6h | ICU | Software Configurable Interrupt B Source Select Register 198 | SLIBR198 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C7h | ICU | Software Configurable Interrupt B Source Select Register 199 | SLIBR199 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C8h | ICU | Software Configurable Interrupt B Source Select Register 200 | SLIBR200 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77C9h | ICU | Software Configurable Interrupt B Source Select Register 201 | SLIBR201 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CAh | ICU | Software Configurable Interrupt B Source Select Register 202 | SLIBR202 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CBh | ICU | Software Configurable Interrupt B Source Select Register 203 | SLIBR203 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CCh | ICU | Software Configurable Interrupt B Source Select Register 204 | SLIBR204 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CDh | ICU | Software Configurable Interrupt B Source Select Register 205 | SLIBR205 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CEh | ICU | Software Configurable Interrupt B Source Select Register 206 | SLIBR206 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 77CFh | ICU | Software Configurable Interrupt B Source Select Register 207 | SLIBR207 | 8 | 8 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUB |
| 0008 7830h | ICU | Group AL0 Interrupt Request Register | GRPAL0 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7834h | ICU | Group AL1 Interrupt Request Register | GRPAL1 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7870h | ICU | Group AL0 Interrupt Request Enable Register | GENAL0 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7874h | ICU | Group AL1 Interrupt Request Enable Register | GENAL1 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7900h | ICU | Software Configurable Interrupt A Request Register 0 | PIAR0 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7901h | ICU | Software Configurable Interrupt A Request Register 1 | PIAR1 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7902h | ICU | Software Configurable Interrupt A Request Register 2 | PIAR2 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7903h | ICU | Software Configurable Interrupt A Request Register 3 | PIAR3 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7904h | ICU | Software Configurable Interrupt A Request Register 4 | PIAR4 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7905h | ICU | Software Configurable Interrupt A Request Register 5 | PIAR5 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 790Bh | ICU | Software Configurable Interrupt A Request Register B | PIARB | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D0h | ICU | Software Configurable Interrupt A Source Select Register 208 | SLIAR208 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79D1h | ICU | Software Configurable Interrupt A Source Select Register 209 | SLIAR209 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |

**Table 4.1 List of I/O Registers (Address Order) (13 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 79F1h | ICU | Software Configurable Interrupt A Source Select Register 241 | SLIAR241 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F2h | ICU | Software Configurable Interrupt A Source Select Register 242 | SLIAR242 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F3h | ICU | Software Configurable Interrupt A Source Select Register 243 | SLIAR243 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F4h | ICU | Software Configurable Interrupt A Source Select Register 244 | SLIAR244 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F5h | ICU | Software Configurable Interrupt A Source Select Register 245 | SLIAR245 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F6h | ICU | Software Configurable Interrupt A Source Select Register 246 | SLIAR246 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F7h | ICU | Software Configurable Interrupt A Source Select Register 247 | SLIAR247 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F8h | ICU | Software Configurable Interrupt A Source Select Register 248 | SLIAR248 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79F9h | ICU | Software Configurable Interrupt A Source Select Register 249 | SLIAR249 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FAh | ICU | Software Configurable Interrupt A Source Select Register 250 | SLIAR250 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FBh | ICU | Software Configurable Interrupt A Source Select Register 251 | SLIAR251 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FCh | ICU | Software Configurable Interrupt A Source Select Register 252 | SLIAR252 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FDh | ICU | Software Configurable Interrupt A Source Select Register 253 | SLIAR253 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FEh | ICU | Software Configurable Interrupt A Source Select Register 254 | SLIAR254 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 79FFh | ICU | Software Configurable Interrupt A Source Select Register 255 | SLIAR255 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUB |
| 0008 7A00h | ICU | Software Configurable Interrupt Source Select Register Write Protect Register | SLIPRCR | 8 | 8 | 2 ICLK to 1 PCLKA/B | 2 ICLK | ICUB |
| 0008 7A01h | ICU | EXDMAC Trigger Select Register | SELEXDR | 8 | 8 | 2 ICLK to 1 PCLKA/B | 2 ICLK | ICUB |
| 0008 8000h | CMT | Compare Match Timer Start Register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8002h | CMT0 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8004h | CMT0 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8006h | CMT0 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8008h | CMT1 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 800Ah | CMT1 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 800Ch | CMT1 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8010h | CMT | Compare Match Timer Start Register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8012h | CMT2 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8014h | CMT2 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8016h | CMT2 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8018h | CMT3 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 801Ah | CMT3 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 801Ch | CMT3 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8020h | WDT | WDT Refresh Register | WDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8022h | WDT | WDT Control Register | WDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8024h | WDT | WDT Status Register | WDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8026h | WDT | WDT Reset Control Register | WDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8030h | IWDT | IWDT Refresh Register | IWDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8032h | IWDT | IWDT Control Register | IWDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8034h | IWDT | IWDT Status Register | IWDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8036h | IWDT | IWDT Reset Control Register | IWDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8038h | IWDT | IWDT Count Stop Control Register | IWDTCSTPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |

**Table 4.1 List of I/O Registers (Address Order) (19 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 9080h | S12AD | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9084h | S12AD | A/D Data Duplication Register A | ADDBLDRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9086h | S12AD | A/D Data Duplication Register B | ADDBLDRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 908Ch | S12AD | A/D Comparison Function Window A/B Status Monitoring Register | ADWINMON | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9090h | S12AD | A/D Comparison Function Control Register | ADCMPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9094h | S12AD | A/D Comparison Function Window A Channel Select Register 0 | ADCMPANSR 0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9098h | S12AD | A/D Comparison Function Window A Comparison Condition Setting Register 0 | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 909Ch | S12AD | A/D Comparison Function Window A Lower Level Setting Register | ADCMPDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 909Eh | S12AD | A/D Comparison Function Window A Upper Level Setting Register | ADCMPDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90A0h | S12AD | A/D Comparison Function Window A Channel Status Register 0 | ADCMPSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90A6h | S12AD | A/D Comparison Function Window B Channel Select Register | ADCMPBNS R | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90A8h | S12AD | A/D Comparison Function Window B Lower Level Setting Register | ADWINLLB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90AAh | S12AD | A/D Comparison Function Window B Upper Level Setting Register | ADWINULB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90ACh | S12AD | A/D Comparison Function Window B Channel Status Register | ADCMPBSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90D4h | S12AD | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90D9h | S12AD | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E0h | S12AD | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E1h | S12AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E2h | S12AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E3h | S12AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E4h | S12AD | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E5h | S12AD | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E6h | S12AD | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 90E7h | S12AD | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9100h | S12AD1 | A/D Control Register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9104h | S12AD1 | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9106h | S12AD1 | A/D Channel Select Register A1 | ADANSA1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 9108h | S12AD1 | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 910Ah | S12AD1 | A/D-Converted Value Addition/Average Function Channel Select Register 1 | ADADS1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 910Ch | S12AD1 | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |
| 0008 910Eh | S12AD1 | A/D Control Extended Register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12AD Fa |

**Table 4.1 List of I/O Registers (Address Order) (22 / 61)**

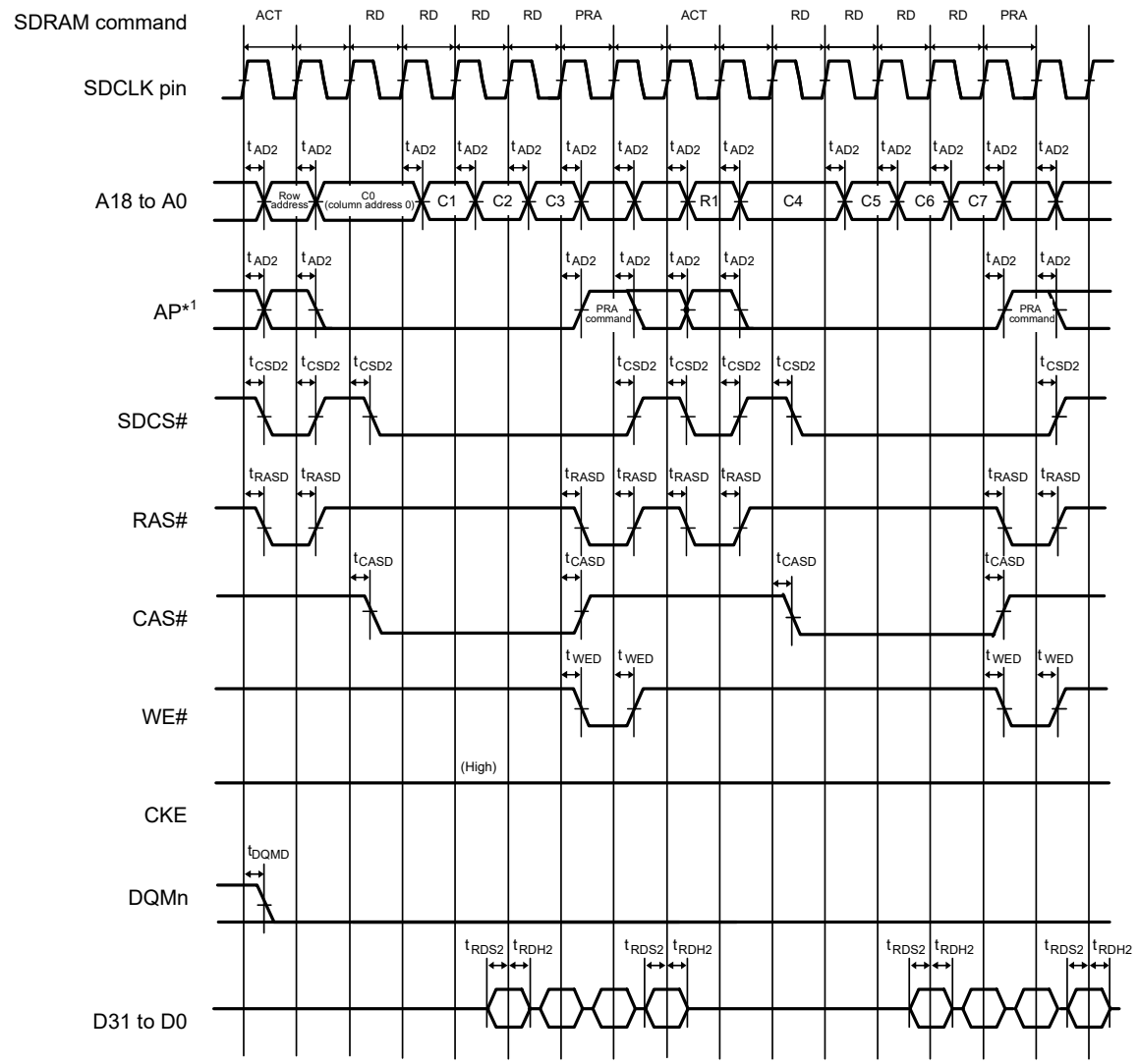
| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 91E3h | S12AD1 | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E4h | S12AD1 | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E5h | S12AD1 | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E6h | S12AD1 | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E7h | S12AD1 | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E8h | S12AD1 | A/D Sampling State Register 8 | ADSSTR8 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91E9h | S12AD1 | A/D Sampling State Register 9 | ADSSTR9 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EAh | S12AD1 | A/D Sampling State Register 10 | ADSSTR10 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EBh | S12AD1 | A/D Sampling State Register 11 | ADSSTR11 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91ECh | S12AD1 | A/D Sampling State Register 12 | ADSSTR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EDh | S12AD1 | A/D Sampling State Register 13 | ADSSTR13 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EEh | S12AD1 | A/D Sampling State Register 14 | ADSSTR14 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 91EFh | S12AD1 | A/D Sampling State Register 15 | ADSSTR15 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADFa |
| 0008 9E00h | QSPI | QSPI Control Register | SPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E01h | QSPI | QSPI Slave Select Polarity Register | SSLP | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E02h | QSPI | QSPI Pin Control Register | SPPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E03h | QSPI | QSPI Status Register | SPSR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E04h | QSPI | QSPI Data Register | SPDR | 32 | 8, 16, 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E08h | QSPI | QSPI Sequence Control Register | SPSCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E09h | QSPI | QSPI Sequence Status Register | SPSSR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Ah | QSPI | QSPI Bit Rate Register | SPBR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Bh | QSPI | QSPI Data Control Register | SPDCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Ch | QSPI | QSPI Clock Delay Register | SPCKD | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Dh | QSPI | QSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Eh | QSPI | QSPI Next-Access Delay Register | SPND | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E10h | QSPI | QSPI Command Register 0 | SPCMD0 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E12h | QSPI | QSPI Command Register 1 | SPCMD1 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E14h | QSPI | QSPI Command Register 2 | SPCMD2 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E16h | QSPI | QSPI Command Register 3 | SPCMD3 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E18h | QSPI | QSPI Buffer Control Register | SPBFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E1Ah | QSPI | QSPI Buffer Data Count Set Register | SPBDCR | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E1Ch | QSPI | QSPI Transfer Data Length Multiplier Setting Register 0 | SPBMUL0 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E20h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 1 | SPBMUL1 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E24h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 2 | SPBMUL2 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E28h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 3 | SPBMUL3 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 A000h | SCI0 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |
| 0008 A001h | SCI0 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh, SCIi |

**Table 4.1 List of I/O Registers (Address Order) (39 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C102h | MPC | CS Output Pin Select Register 0 | PFCSS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C103h | MPC | CS Output Pin Select Register 1 | PFCSS1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C104h | MPC | Address Output Enable Register 0 | PFAOE0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C105h | MPC | Address Output Enable Register 1 | PFAOE1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C106h | MPC | External Bus Control Register 0 | PFBCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C107h | MPC | External Bus Control Register 1 | PFBCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C108h | MPC | External Bus Control Register 2 | PFBCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C109h | MPC | External Bus Control Register 3 | PFBCR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C10Eh | MPC | Ethernet Control Register | PFENET | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C128h | PORT0 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C129h | PORT1 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Ah | PORT2 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Bh | PORT3 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Dh | PORT5 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C12Fh | PORT7 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C130h | PORT8 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C131h | PORT9 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C132h | PORTA | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C133h | PORTB | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C134h | PORTC | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C135h | PORTD | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C136h | PORTE | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C138h | PORTG | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C13Ah | PORTJ | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C140h | MPC | P00 Pin Function Control Register | P00PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C141h | MPC | P01 Pin Function Control Register | P01PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C142h | MPC | P02 Pin Function Control Register | P02PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C143h | MPC | P03 Pin Function Control Register | P03PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C145h | MPC | P05 Pin Function Control Register | P05PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C147h | MPC | P07 Pin Function Control Register | P07PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C148h | MPC | P10 Pin Function Control Register | P10PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C149h | MPC | P11 Pin Function Control Register | P11PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ah | MPC | P12 Pin Function Control Register | P12PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Bh | MPC | P13 Pin Function Control Register | P13PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ch | MPC | P14 Pin Function Control Register | P14PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Dh | MPC | P15 Pin Function Control Register | P15PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Eh | MPC | P16 Pin Function Control Register | P16PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Fh | MPC | P17 Pin Function Control Register | P17PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C150h | MPC | P20 Pin Function Control Register | P20PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C151h | MPC | P21 Pin Function Control Register | P21PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |

**Table 4.1 List of I/O Registers (Address Order) (54 / 61)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1A38h | MTU6 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A39h | MTU7 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A3Ah | MTU | Timer Interrupt Skipping Mode Register B | TITMRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A3Bh | MTU | Timer Interrupt Skipping Set Register 2B | TITCR2B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A3Ch | MTU | Timer Interrupt Skipping Counter 2B | TITCNT2B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A40h | MTU7 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A44h | MTU7 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A46h | MTU7 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A48h | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A4Ah | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A4Ch | MTU6 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A4Dh | MTU7 | Timer Control Register 2 | TCR2 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A50h | MTU6 | Timer Synchronous Clear Register | TSYCR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A60h | MTU | Timer Waveform Control Register B | TWCRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A70h | MTU | Timer Mode Register 2B | TMDR2B | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A72h | MTU6 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A74h | MTU7 | Timer General Register E | TGRE | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A76h | MTU7 | Timer General Register F | TGRF | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A80h | MTU | Timer Start Register B | TSTRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A81h | MTU | Timer Synchronous Register B | TSYRB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A84h | MTU | Timer Read/Write Enable Register B | TRWERB | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A93h | MTU6 | Noise Filter Control Register 6 | NFCR6 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A94h | MTU7 | Noise Filter Control Register 7 | NFCR7 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1A95h | MTU5 | Noise Filter Control Register 5 | NFCR5 | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C80h | MTU5 | Timer Counter U | TCNTU | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C82h | MTU5 | Timer General Register U | TGRU | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C84h | MTU5 | Timer Control Register U | TCRU | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C85h | MTU5 | Timer Control Register 2 | TCR2U | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C86h | MTU5 | Timer I/O Control Register U | TIORU | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C90h | MTU5 | Timer Counter V | TCNTV | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C92h | MTU5 | Timer General Register V | TGRV | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C94h | MTU5 | Timer Control Register V | TCRV | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C95h | MTU5 | Timer Control Register 2 | TCR2V | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1C96h | MTU5 | Timer I/O Control Register V | TIORV | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA0h | MTU5 | Timer Counter W | TCNTW | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA2h | MTU5 | Timer General Register W | TGRW | 16 | 16 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA4h | MTU5 | Timer Control Register W | TCRW | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA5h | MTU5 | Timer Control Register 2 | TCR2W | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CA6h | MTU5 | Timer I/O Control Register W | TIORW | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CB2h | MTU5 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CB4h | MTU5 | Timer Start Register | TSTR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 1CB6h | MTU5 | Timer Compare Match Clear Register | TCNTCMPCLR | 8 | 8 | 4, 5 PCLKA | 1, 2 ICLK | MTU3a |
| 000C 5800h | BSC | Extended Bus Master Priority Control Register | EBMAPCR | 32 | 32 | 1, 2 PCLKA | 1 ICLK | BSC |
| 000D 0040h | SCI10 | Serial Mode Register | SMR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0041h | SCI10 | Bit Rate Register | BRR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0042h | SCI10 | Serial Control Register | SCR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |
| 000D 0043h | SCI10 | Transmit Data Register | TDR | 8 | 8 | 3, 4 PCLKA | 1, 2 ICLK | SCIi |




Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.27 SDRAM Space Multiple Read Line Stride Bus Timing**

## 5.3.6 EXDMAC Timing

**Table 5.25 EXDMAC Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| EXDMAC | EDREQ setup time | $t_{EDRQS}$ | 13 | — | ns | Figure 5.30 |
| | EDREQ hold time | $t_{EDRQH}$ | 2 | — | ns | |
| | EDACK delay time | $t_{EDACD}$ | — | 13 | ns | Figure 5.31, Figure 5.32 |

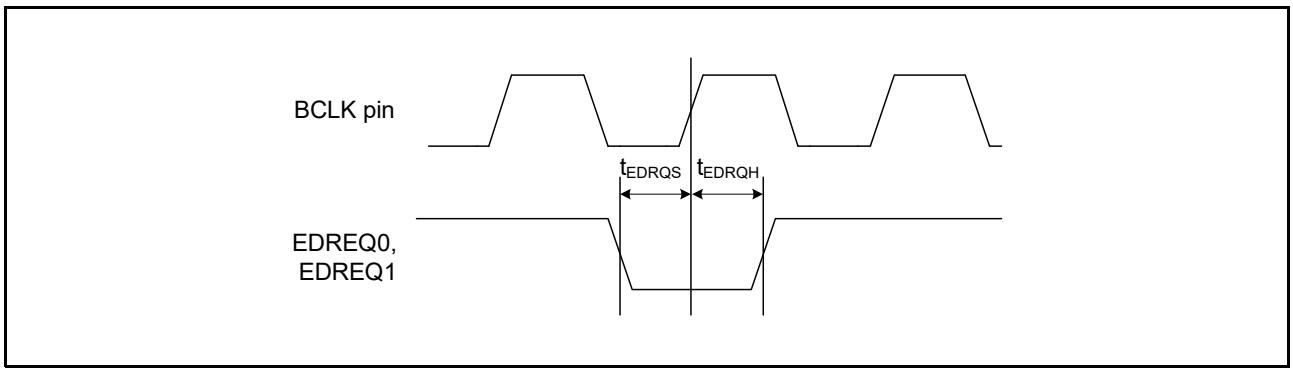



**Figure 5.30 EDREQ0 and EDREQ1 Input Timing**

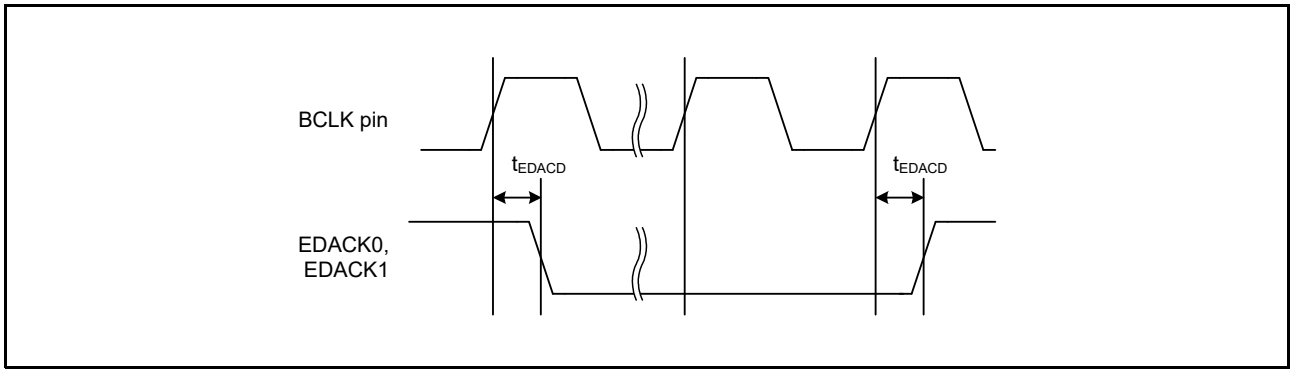



**Figure 5.31 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)**

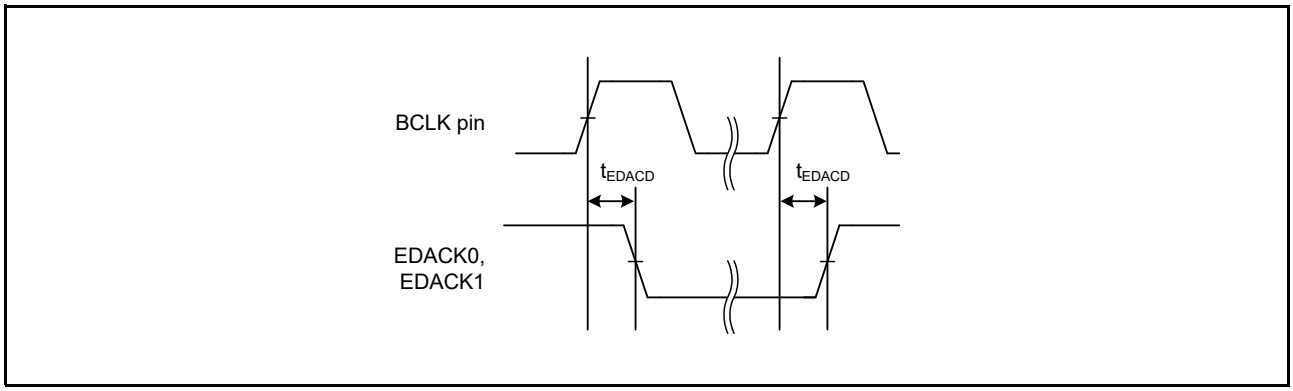



**Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

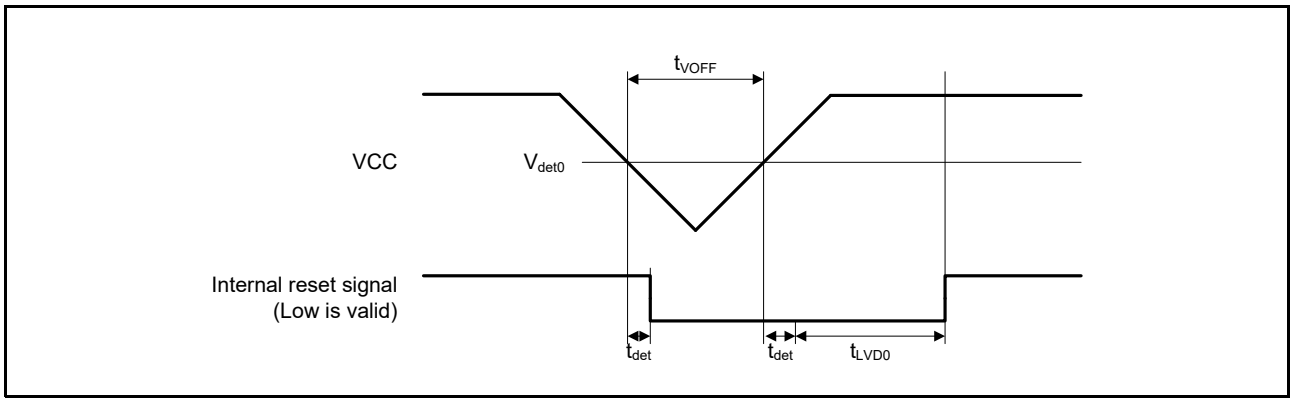



**Figure 5.77 Voltage Detection Circuit Timing ($V_{det0}$)**

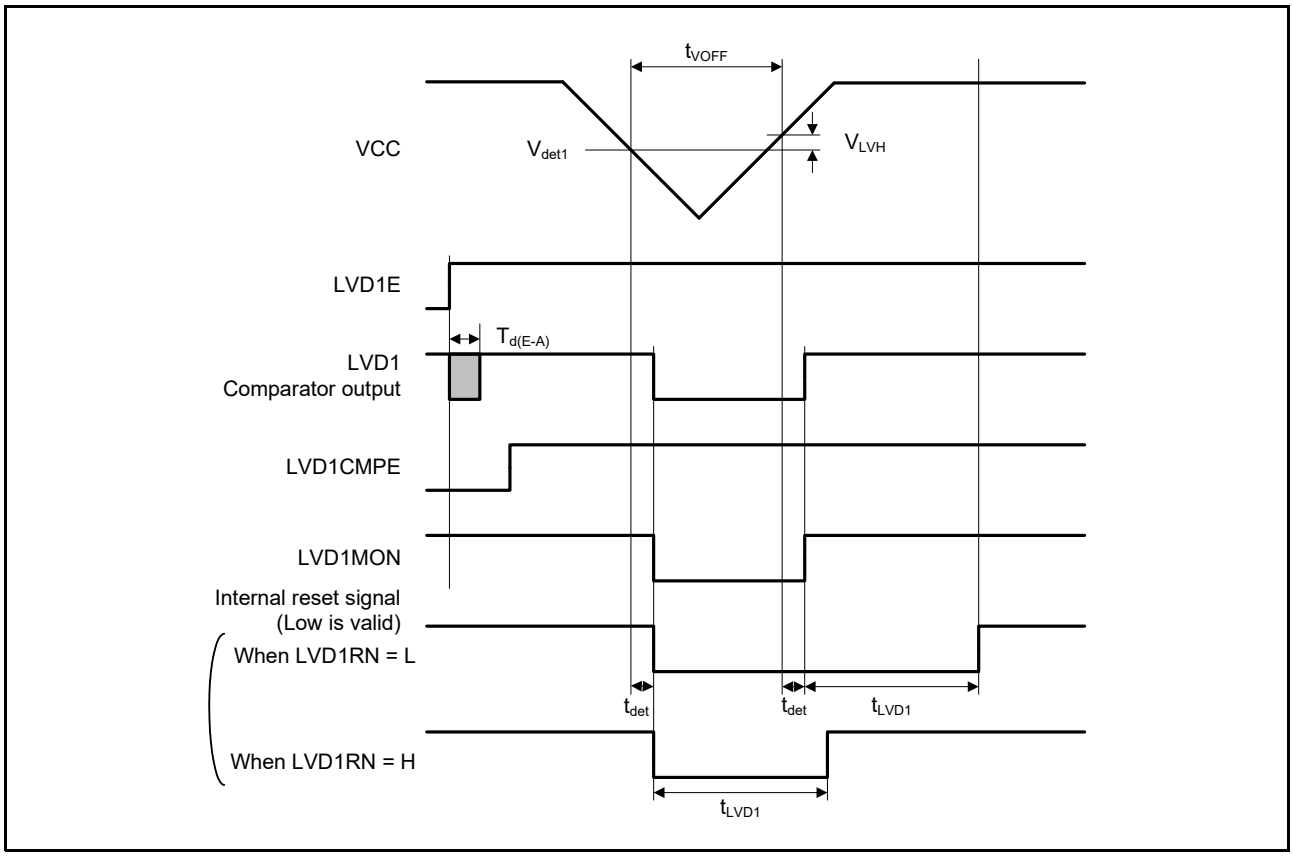



**Figure 5.78 Voltage Detection Circuit Timing ($V_{det1}$)**

## 5.11 Flash Memory Characteristics

**Table 5.54 Code Flash Memory Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

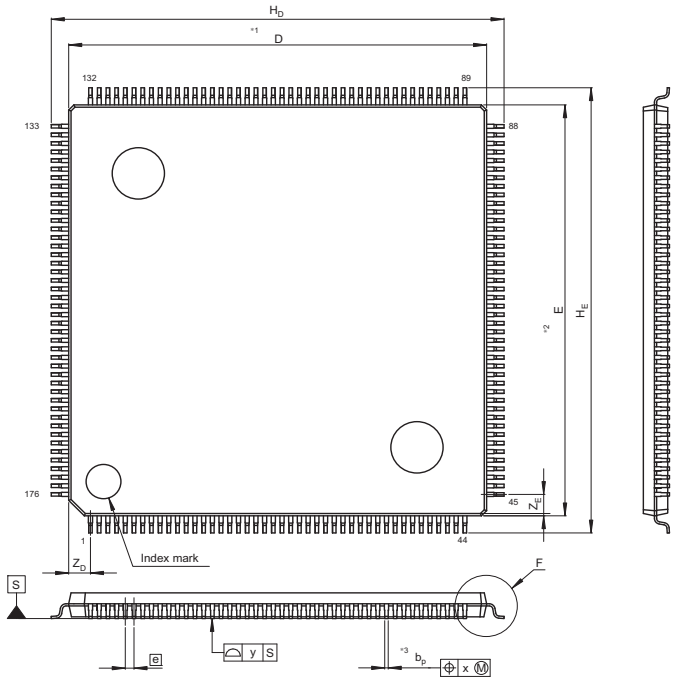
| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 15 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time $N_{PEC}$ ≤ 100 times | 128 bytes | $t_{P128}$ | — | 0.75 | 13.2 | — | 0.38 | 6.6 | — | 0.34 | 6 | ms |
| | 8 Kbytes | $t_{P8K}$ | — | 49 | 176 | — | 25 | 88 | — | 22 | 80 | ms |
| | 32 Kbytes | $t_{P32K}$ | — | 194 | 704 | — | 97 | 352 | — | 88 | 320 | ms |
| Programming time $N_{PEC}$ > 100 times | 128 bytes | $t_{P128}$ | — | 0.91 | 15.8 | — | 0.46 | 8 | — | 0.41 | 7.2 | ms |
| | 8 Kbytes | $t_{P8K}$ | — | 60 | 212 | — | 30 | 106 | — | 27 | 96 | ms |
| | 32 Kbytes | $t_{P32K}$ | — | 234 | 848 | — | 117 | 424 | — | 106 | 384 | ms |
| Erasure time $N_{PEC}$ ≤ 100 times | 8 Kbytes | $t_{E8K}$ | — | 78 | 216 | — | 48 | 132 | — | 43 | 120 | ms |
| | 32 Kbytes | $t_{E32K}$ | — | 283 | 864 | — | 173 | 528 | — | 157 | 480 | ms |
| Erasure time $N_{PEC}$ > 100 times | 8 Kbytes | $t_{E8K}$ | — | 94 | 260 | — | 58 | 158 | — | 52 | 144 | ms |
| | 32 Kbytes | $t_{E32K}$ | — | 341 | 1040 | — | 208 | 632 | — | 189 | 576 | ms |
| Reprogramming/erasure cycle*1 | | $N_{PEC}$ | 10000 *2 | — | — | 10000 *2 | — | — | 10000 *2 | — | — | Times |
| Suspend delay time during programming | | $t_{SPD}$ | — | — | 264 | — | — | 132 | — | — | 120 | µs |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 216 | — | — | 132 | — | — | 120 | µs |
| Second suspend delay time during erasure (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.7 | — | — | 1.7 | ms |
| Suspend delay time during erasure (in erasure priority mode) | | $t_{SEED}$ | — | — | 1.7 | — | — | 1.7 | — | — | 1.7 | ms |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 22 | — | — | 20 | µs |
| Data hold time*3 | | $t_{DRP}$ | 10 | — | — | 10 | — | — | 10 | — | — | Year |

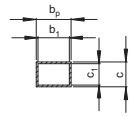
Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

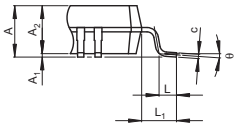
Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP176-24x24-0.50 | PLQP0176KB-A | 176P6Q-A/FP-176E/FP-176EV | 1.8g |




Terminal cross section




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 23.9 | 24.0 | 24.1 |
| E | 23.9 | 24.0 | 24.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 25.8 | 26.0 | 26.2 |
| $H_E$ | 25.8 | 26.0 | 26.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure C 176-Pin LFQFP (PLQP0176KB-A)