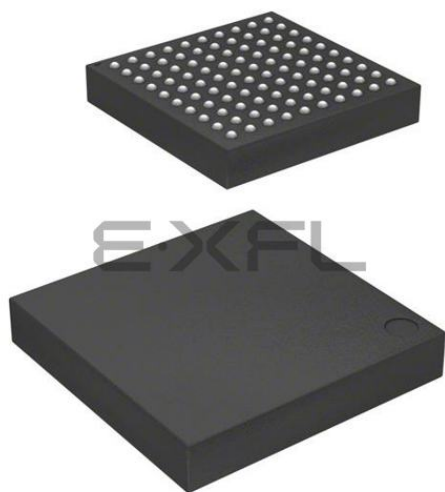




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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n9adlj-20

Table 1.3 List of Products (7/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F5651EDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651EHDJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F5651CDDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651CHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F56519ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56519BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56519EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56519FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56517ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56517BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56517EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56517FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56514ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56514BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56514EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56514FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
RX651 (G version)	R5F5651EDGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651EHGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651CDGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651CHGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651EDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651EHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651CDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651CHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F56519AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F56519BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F56519EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F56519FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105
	R5F56517AGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F56517BGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R								
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15							
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14							
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13							
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12							
11	PD6	PG1	VCC	P61	RX65N Group, RX651 Group PTLG0177KA-A (177-Pin TFLGA) (Upper Perspective View)							P81	P82	PC6	VCC	11							
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10							
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9							
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8							
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7							
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_ USB	USB0_ DP	6							
5	P46	P47	P45	P44	NC	RX65N Group, RX651 Group PTLG0177KA-A (177-Pin TFLGA) (Upper Perspective View)							PJ2	P12	VCC_ USB	USB0_ DM	5						
4	P42	P41	P43	P00	VSS								BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5								PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE								VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5								VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E								F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
74		P83	EDACK1	MTIOC4C	ET0_CRS/ RMII0_CRS_DV/ SCK10/SS10#/ CTS10#		LCD_DA TA8-A		
75	VCC								
76	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A	MMC_D7-A	LCD_DA TA9-A	IRQ14	
77		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A	MMC_D6-A	LCD_DA TA10-A	IRQ13	
78		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A	MMC_D5-A	LCD_DA TA11-A		
79		P82	EDREQ1	MTIOC4A/ PO28	ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10	MMC_D4-A	LCD_DA TA12-A		
80		P81	EDACK0	MTIOC3D/ PO27	ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/RXD10	QIO3-A/SDHI_CD/ MMC_D3-A	LCD_DA TA13-A		
81		P80	EDREQ0	MTIOC3B/ PO26	ET0_TX_EN/ RMII0_TXD_EN/ SCK10/RTS10#	QIO2-A/SDHI_WP/ MMC_D2-A	LCD_DA TA14-A		
82		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A	QMI-A/QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A	LCD_DA TA15-A		
83		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5	QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A	LCD_DA TA16-A		
84		P77	CS7#	PO23	ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/TXD11	QSPCLK-A/ SDHI_CLK-A/ SDSI_CLK-A/ MMC_CLK-A	LCD_DA TA17-A		
85		P76	CS6#	PO22	ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/RXD11	QSSL-A/ SDHI_CMD-A/ SDSI_CMD-A/ MMC_CMD-A	LCD_DA TA18-A		
86		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A	SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A	LCD_DA TA19-A		
87		P75	CS5#	PO20	ET0_ERXD0/ RMII0_RXD0/ SCK11/RTS11#	SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A	LCD_DA TA20-A		
88		P74	A20/CS4#	PO19	ET0_ERXD1/ RMII0_RXD1/ SS11#/CTS11#		LCD_DA TA21-A		
89		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A		LCD_DA TA22-A	IRQ12	
90	VCC								
91		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
B13		PE4	D12[A12/D12]/D4[A4/D4]*1	MTIOC4D/MTIOC1A/PO28	ET0_ERXD2/SSLB0-B		LCD_DA TA12-B*1		AN102
C1	AVSS1								
C2		P02		TMC11	SCK6			IRQ10	AN120
C3	VREFH0								
C4		P41						IRQ9-DS	AN001
C5		P46						IRQ14-DS	AN006
C6	VSS								
C7		PD1	D1[A1/D1]	MTIOC4B/POE0#	MOSIC-A/CTX0		LCD_DA TA23-B*1	IRQ1	AN109
C8		PD3	D3[A3/D3]	MTIOC8D/TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3-B/MMC_D3-B	LCD_DA TA21-B*1	IRQ3	AN111
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3-A	QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B	LCD_DA TA17-B*1	IRQ7	AN107
C10		P63	CAS#/D2[A2/D2]*1/CS3#						
C11		PE0	D8[A8/D8]/D0[A0/D0]*1	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DA TA16-B*1		ANEX0
C12		P70	SDCLK						
C13	VSS								
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6			IRQ8	AN118
D2		PF5						IRQ4	
D3		P03						IRQ11	DA0
D4		P01		TMC10	RXD6/SMISO6/SSCL6			IRQ9	AN119
D5	VCC								
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#				AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/POE10#	SSLC1-A	QSPCLK-B/SDHI_CLK-B/MMC_CLK-B	LCD_DA TA19-B*1	IRQ5	AN113
D8		P60	CS0#						
D9		P64	WE#/D3[A3/D3]*1/CS4#						
D10		PE7	D15[A15/D15]/D7[A7/D7]*1	MTIOC6A/TOC1	MISOB-B	SDHI_WP/MMC_RES#-B	LCD_DA TA9-B*1	IRQ7	AN105
D11	VCC								
D12		PE5	D13[A13/D13]/D5[A5/D5]*1	MTIOC4C/MTIOC2B	ET0_RX_CLK/REF50CK0/RSPCKB-B		LCD_DA TA11-B*1	IRQ5	AN103
D13		PE6	D14[A14/D14]/D6[A6/D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/MMC_CD-B	LCD_DA TA10-B*1	IRQ6	AN104
E1	VSS								
E2	VCL								
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#				

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/5)

Pin Number				Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)			
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC				GLCDC	Interrupt	A/D D/A
C7		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2- B/MMC_D2-B	LCD_DA TA22-B*1	IRQ2	AN110
C8		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DA TA19-B*1	IRQ5	AN113
C9		PE5	D13[A13/ D13]/D5[A5/ D5]*1	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DA TA11-B*1	IRQ5	AN103
C10		PE4	D12[A12/ D12]/D4[A4/ D4]*1	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DA TA12-B*1		AN102
D1	XCIN								
D2	XCOUT								
D3	MD/FINED								
D4	VBATT								
D5		P45						IRQ13- DS	AN005
D6		P46						IRQ14- DS	AN006
D7		PE6	D14[A14/ D14]/D6[A6/ D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DA TA10-B*1	IRQ6	AN104
D8		PE7	D15[A15/ D15]/D7[A7/ D7]*1	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DA TA9-B*1	IRQ7	AN105
D9		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOC0B/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DA TA7-B*1	IRQ11	
D10		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DA TA8-B*1		
E1	XTAL	P37							
E2	VSS								
E3	RES#								
E4	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
E5		P41						IRQ9-DS	AN001
E6		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DA TA6-B*1		
E7		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DA TA2-B*1		
E8		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DA TA4-B*1	IRQ5-DS	
E9		PA5	A5	MTIOC6B/ TIOC81/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DA TA3-B*1		
E10		PA3	A3	MTIOC0D/ MTCLKD/ TIOC0D/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DA TA5-B*1	IRQ6-DS	
F1	EXTAL	P36							

Table 4.1 List of I/O Registers (Address Order) (10 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 779Dh	ICU	Software Configurable Interrupt B Source Select Register 157	SLIBR157	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Eh	ICU	Software Configurable Interrupt B Source Select Register 158	SLIBR158	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Fh	ICU	Software Configurable Interrupt B Source Select Register 159	SLIBR159	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A0h	ICU	Software Configurable Interrupt B Source Select Register 160	SLIBR160	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A1h	ICU	Software Configurable Interrupt B Source Select Register 161	SLIBR161	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A2h	ICU	Software Configurable Interrupt B Source Select Register 162	SLIBR162	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A3h	ICU	Software Configurable Interrupt B Source Select Register 163	SLIBR163	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A4h	ICU	Software Configurable Interrupt B Source Select Register 164	SLIBR164	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A5h	ICU	Software Configurable Interrupt B Source Select Register 165	SLIBR165	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A6h	ICU	Software Configurable Interrupt B Source Select Register 166	SLIBR166	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A7h	ICU	Software Configurable Interrupt B Source Select Register 167	SLIBR167	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A8h	ICU	Software Configurable Interrupt B Source Select Register 168	SLIBR168	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A9h	ICU	Software Configurable Interrupt B Source Select Register 169	SLIBR169	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AAh	ICU	Software Configurable Interrupt B Source Select Register 170	SLIBR170	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ABh	ICU	Software Configurable Interrupt B Source Select Register 171	SLIBR171	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ACh	ICU	Software Configurable Interrupt B Source Select Register 172	SLIBR172	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ADh	ICU	Software Configurable Interrupt B Source Select Register 173	SLIBR173	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AEh	ICU	Software Configurable Interrupt B Source Select Register 174	SLIBR174	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AFh	ICU	Software Configurable Interrupt B Source Select Register 175	SLIBR175	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B0h	ICU	Software Configurable Interrupt B Source Select Register 176	SLIBR176	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B1h	ICU	Software Configurable Interrupt B Source Select Register 177	SLIBR177	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B2h	ICU	Software Configurable Interrupt B Source Select Register 178	SLIBR178	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B3h	ICU	Software Configurable Interrupt B Source Select Register 179	SLIBR179	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B4h	ICU	Software Configurable Interrupt B Source Select Register 180	SLIBR180	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B5h	ICU	Software Configurable Interrupt B Source Select Register 181	SLIBR181	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B6h	ICU	Software Configurable Interrupt B Source Select Register 182	SLIBR182	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B7h	ICU	Software Configurable Interrupt B Source Select Register 183	SLIBR183	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B8h	ICU	Software Configurable Interrupt B Source Select Register 184	SLIBR184	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B9h	ICU	Software Configurable Interrupt B Source Select Register 185	SLIBR185	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BAh	ICU	Software Configurable Interrupt B Source Select Register 186	SLIBR186	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BBh	ICU	Software Configurable Interrupt B Source Select Register 187	SLIBR187	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (24 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A026h	SMC11	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A029h	SCI1	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A02Ah	SCI1	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A02Bh	SCI1	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A02Ch	SCI1	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A040h	SCI2	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A041h	SCI2	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A042h	SCI2	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A043h	SCI2	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A044h	SCI2	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A045h	SCI2	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli

Table 4.1 List of I/O Registers (Address Order) (27 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A08Ah	SCI4	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A08Bh	SCI4	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A08Ch	SCI4	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A091h	SCI4	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A090h	SCI4	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A092h	SCI4	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0A9h	SCI5	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0AAh	SCI5	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0ABh	SCI5	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i

Table 4.1 List of I/O Registers (Address Order) (28 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (36 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C04Bh	PORTB	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C04Ch	PORTC	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C04Dh	PORTD	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C04Eh	PORTE	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C04Fh	PORTF	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C050h	PORTG	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C052h	PORTJ	Port Input Register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C066h	PORT6	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C070h	PORTG	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C080h	PORT0	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C081h	PORT0	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C082h	PORT1	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C083h	PORT1	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C084h	PORT2	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C085h	PORT2	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports

Table 4.1 List of I/O Registers (Address Order) (44 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	Hour Capture Register 1	RHRCPP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	Second Capture Register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C472h	RTC	BCNT0 Capture Register 2	BCNT0CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	Minute Capture Register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C474h	RTC	BCNT1 Capture Register 2	BCNT1CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	Hour Capture Register 2	RHRCPP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C476h	RTC	BCNT2 Capture Register 2	BCNT2CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	Date Capture Register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ah	RTC	BCNT3 Capture Register 2	BCNT3CP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C47Ch	RTC	Month Capture Register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C4C0h	POE3	Input Level Control/Status Register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C2h	POE3	Output Level Control/Status Register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C4h	POE3	Input Level Control/Status Register 2	ICSR2	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C6h	POE3	Output Level Control/Status Register 2	OCSR2	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4C8h	POE3	Input Level Control/Status Register 3	ICSR3	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4CAh	POE3	Software Port Output Enable Register	SPOER	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4CBh	POE3	Port Output Enable Control Register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4CCh	POE3	Port Output Enable Control Register 2	POECR2	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D0h	POE3	Port Output Enable Control Register 4	POECR4	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D2h	POE3	Port Output Enable Control Register 5	POECR5	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D6h	POE3	Input Level Control/Status Register 4	ICSR4	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4D8h	POE3	Input Level Control/Status Register 5	ICSR5	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4DAh	POE3	Active Level Setting Register 1	ALR1	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4DCh	POE3	Input Level Control/Status Register 6	ICSR6	16	16	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E4h	POE3	MTU0 Pin Select Register 1	M0SELR1	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E5h	POE3	MTU0 Pin Select Register 2	M0SELR2	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E6h	POE3	MTU3 Pin Select Register	M3SELR	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E7h	POE3	MTU4 Pin Select Register 1	M4SELR1	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4E8h	POE3	MTU4 Pin Select Register 2	M4SELR2	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C4EAh	POE3	MTU6 Pin Select Register	M6SELR	8	8	2, 3 PCLKB	2 ICLK	POE3a
0008 C500h	TEMPS	Temperature Sensor Control Register	TSCR	8	8	2, 3 PCLKB	2 ICLK	TEMPS
0008 C5C0h	DA	D/A A/D Synchronous Unit Select Register	DAADUSR	8	8	2, 3 PCLKB	2 ICLK	R12DA
0009 0200h to 0009 03FFh	CAN0	Mailbox Registers 0 to 31	MB0 to 31	128	8, 16, 32*6	2, 3 PCLKB	2 ICLK	CAN
0009 0400h to 0009 041Fh	CAN0	Mask Registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0420h	CAN0	FIFO Received ID Compare Register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0424h	CAN0	FIFO Received ID Compare Register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0428h	CAN0	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 042Ch	CAN0	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN

Table 4.1 List of I/O Registers (Address Order) (51 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 01F8h	ETHER C0	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 1200h	MTU3	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ch	MTU3	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1231h	MTU	Timer Interrupt Skipping Counter 1A	TITCNT1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ch	MTU	Timer Interrupt Skipping Counter 2A	TITCNT2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

5.3.2 Clock Timing

Table 5.14 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	Figure 5.3
	100-pin package		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	

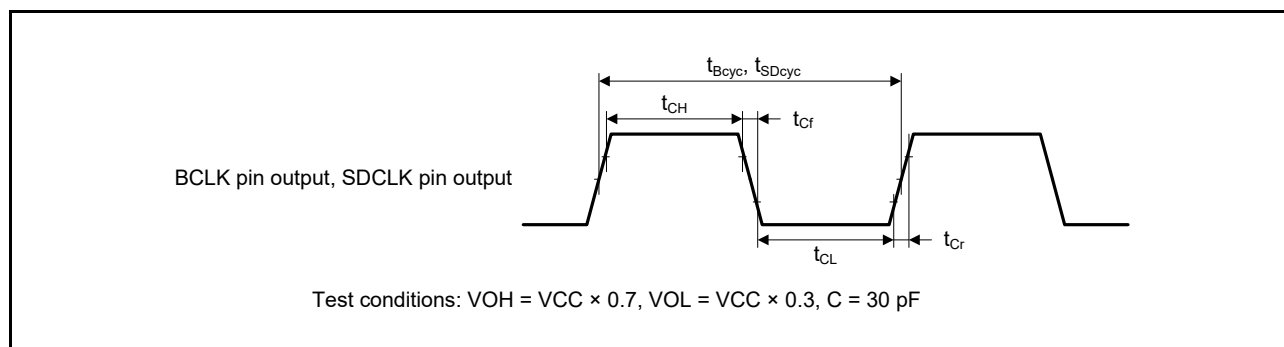
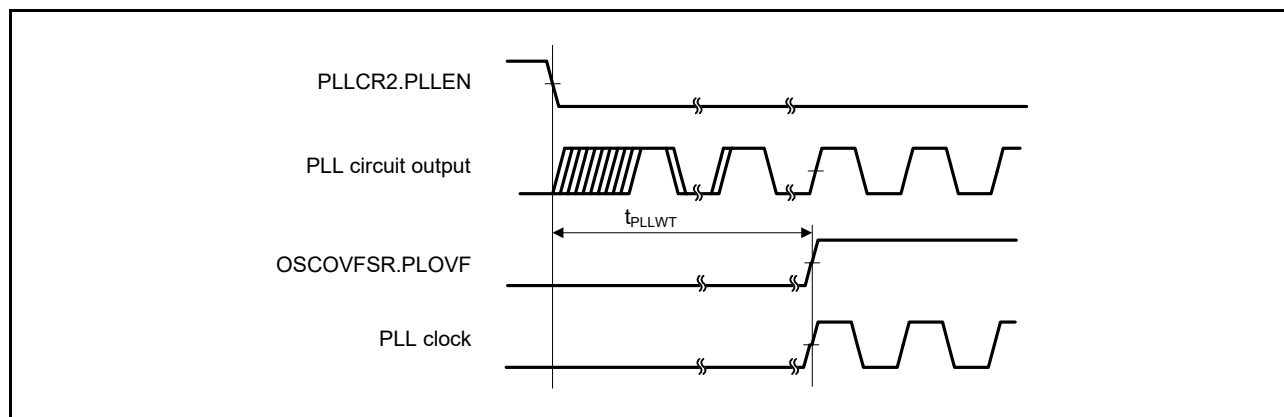
**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

Table 5.19 PLL Clock Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	μ s	Figure 5.10

**Figure 5.10 PLL Clock Oscillation Start Timing****Table 5.20 Sub-Clock Timing**

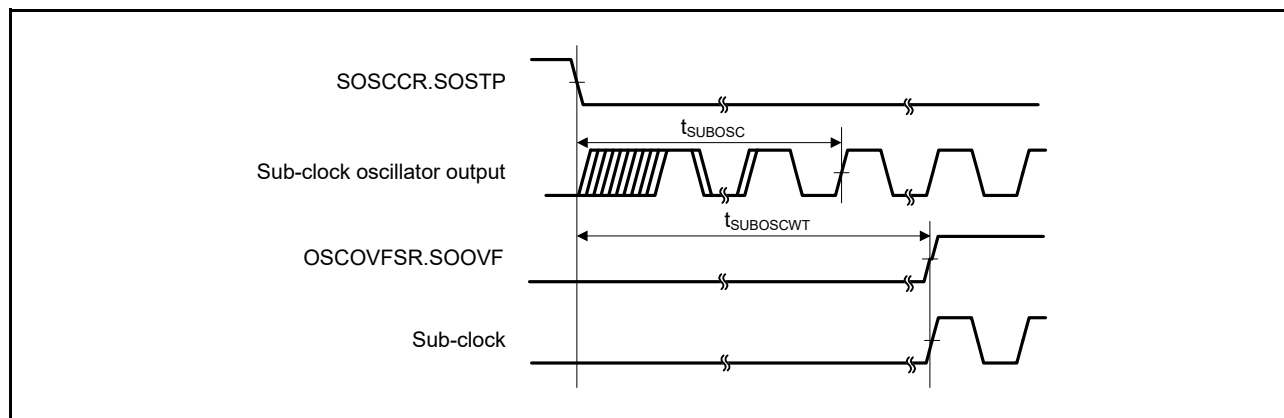
Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $V_{BATT} = 2.0$ to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 5.11
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the $SOSCWTCCR.SSTS[7:0]$ bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.

$$t_{SUBOSCWT} = [(SSTS[7:0] \text{ bits} \times 16384) + 10] / f_{Loco}$$

**Figure 5.11 Sub-Clock Oscillation Start Timing**

5.3.4 Control Signal Timing

Table 5.23 Control Signal Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.14
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 5.14
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.15
		$t_{PBcyc} \times 2$	—	—	ns	$t_{PBcyc} \times 2 > 200$ ns, Figure 5.15

Note 1. t_{PBcyc} : PCLKB cycle

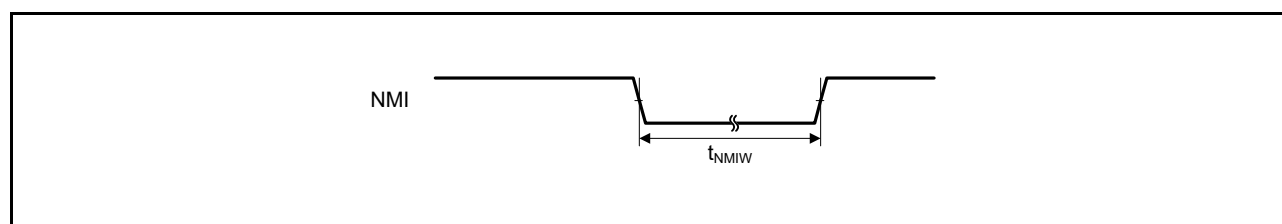
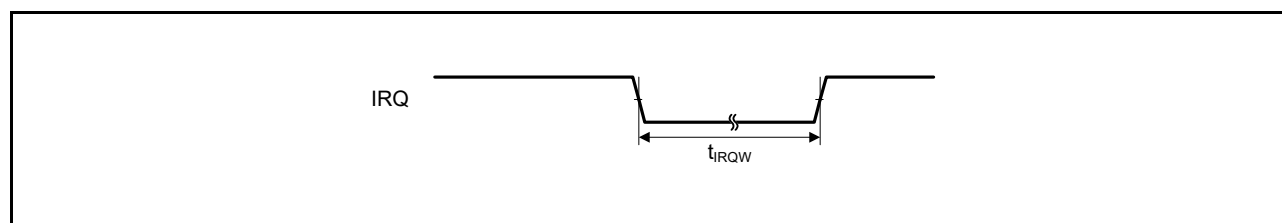
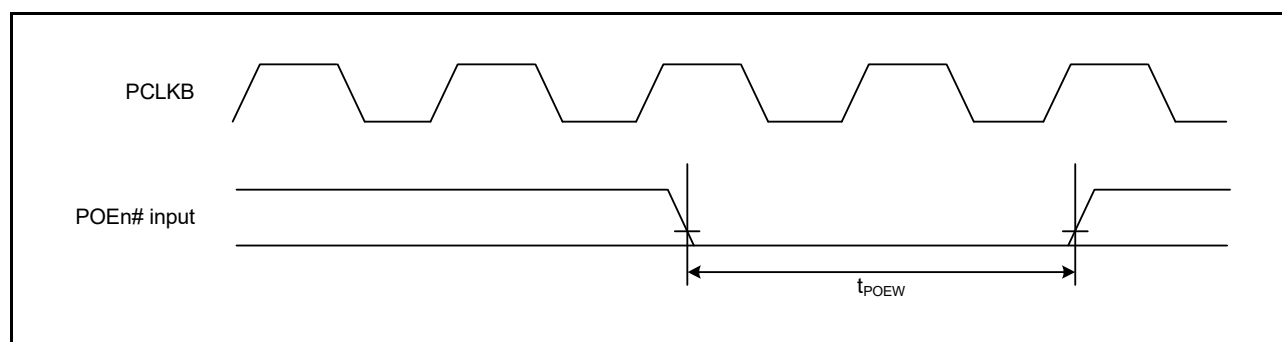
**Figure 5.14 NMI Interrupt Input Timing****Figure 5.15 IRQ Interrupt Input Timing**

Table 5.31 POE3 Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
POE	POE# input pulse width	t_{POEW}	1.5	—	t_{PBcyc}	Figure 5.40

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.40 POE# Input Timing**

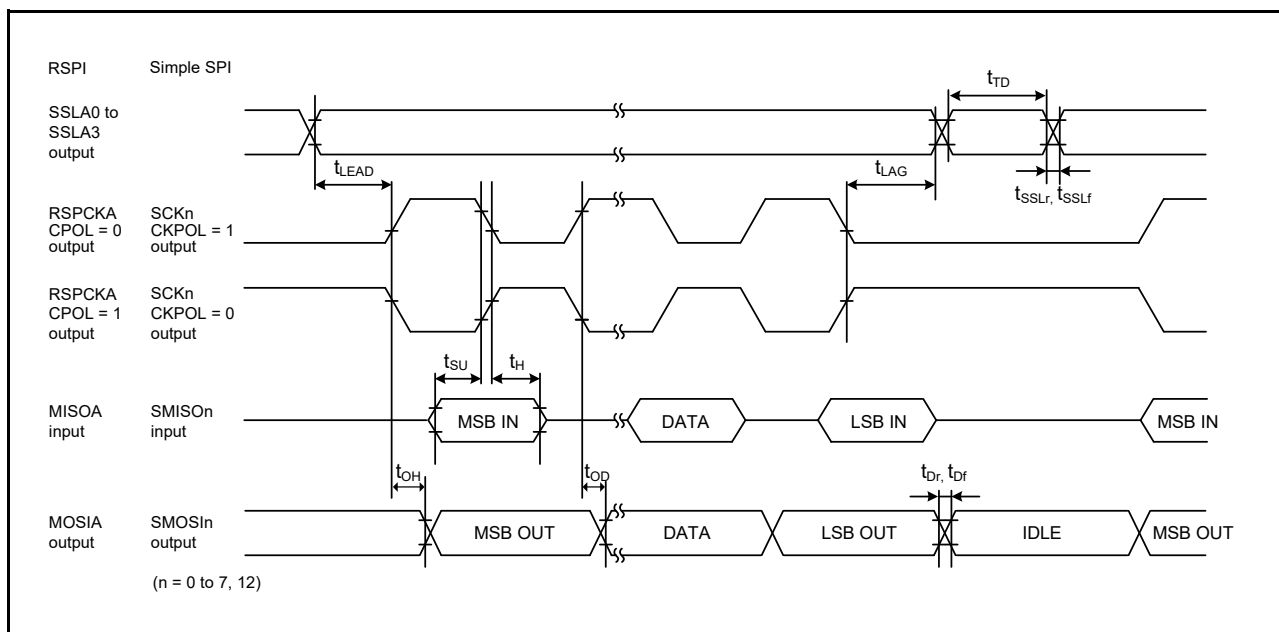


Figure 5.47 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

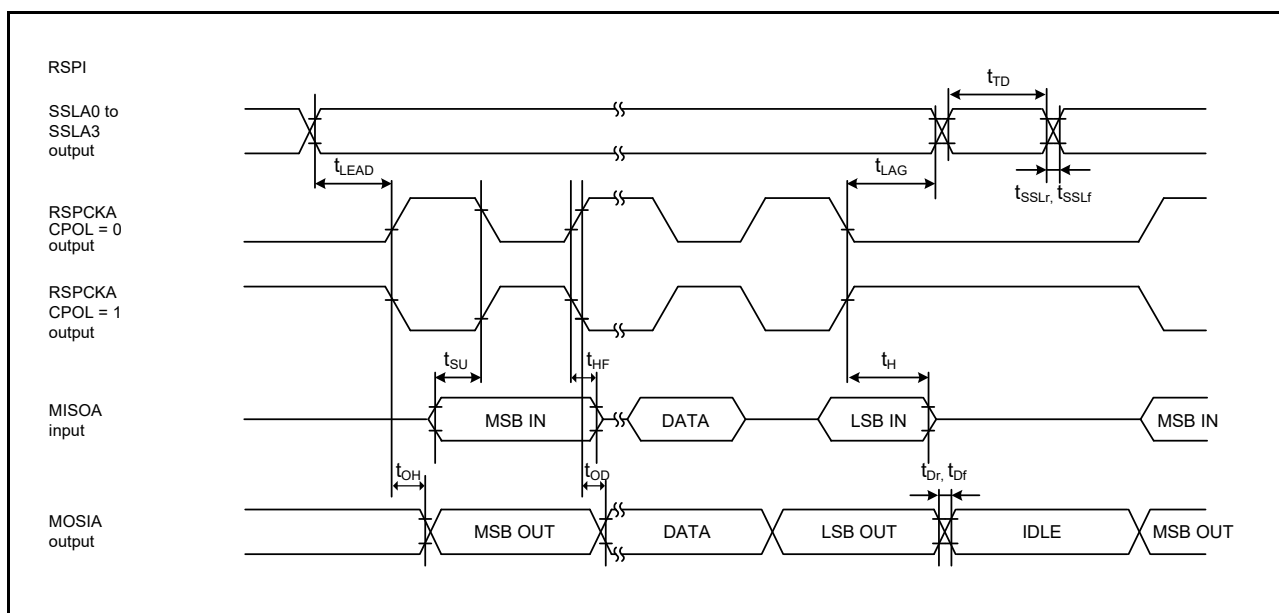


Figure 5.48 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

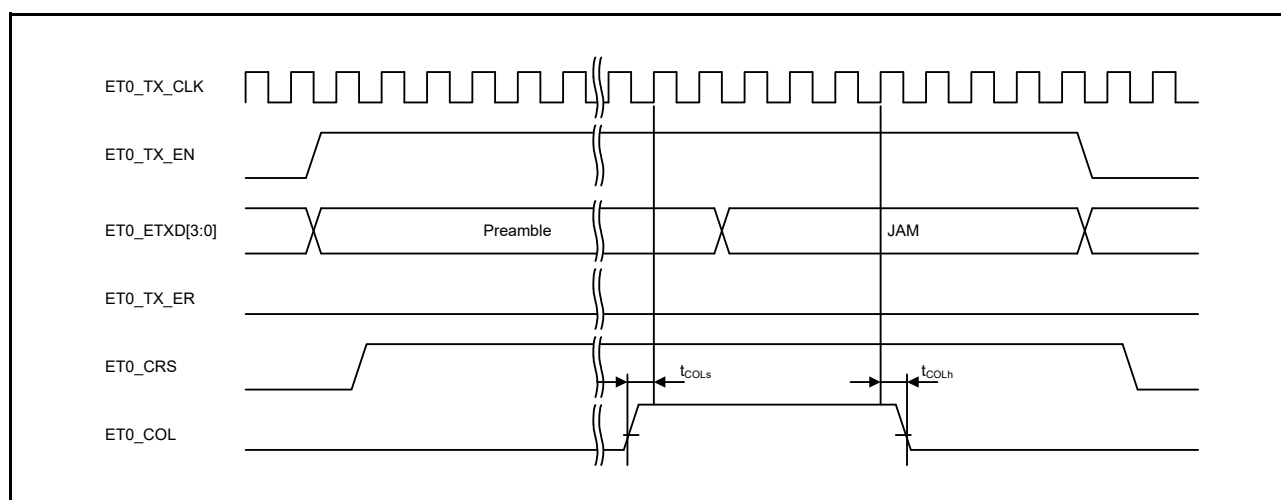


Figure 5.62 MII Transmission Timing (Conflict Occurrence)

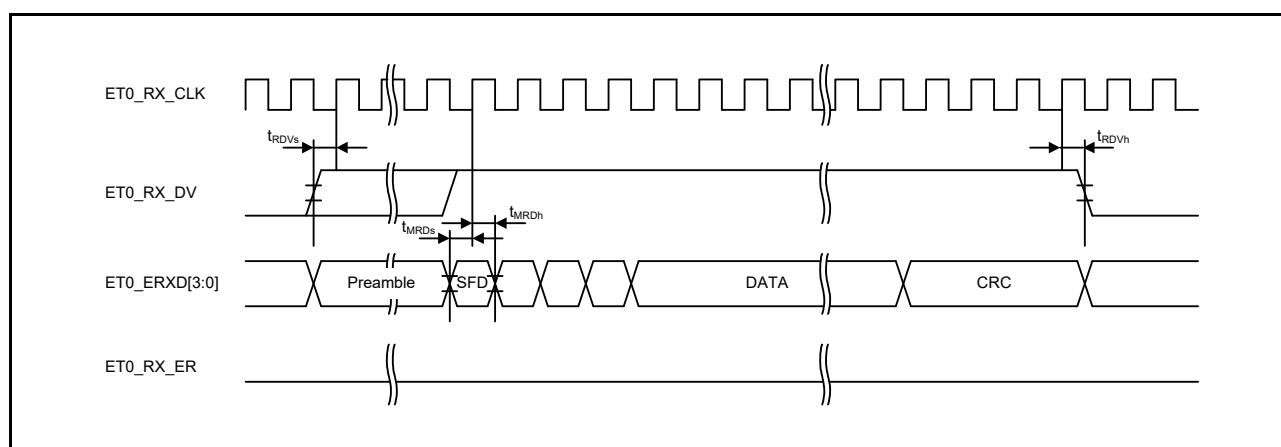


Figure 5.63 MII Reception Timing (Normal Operation)

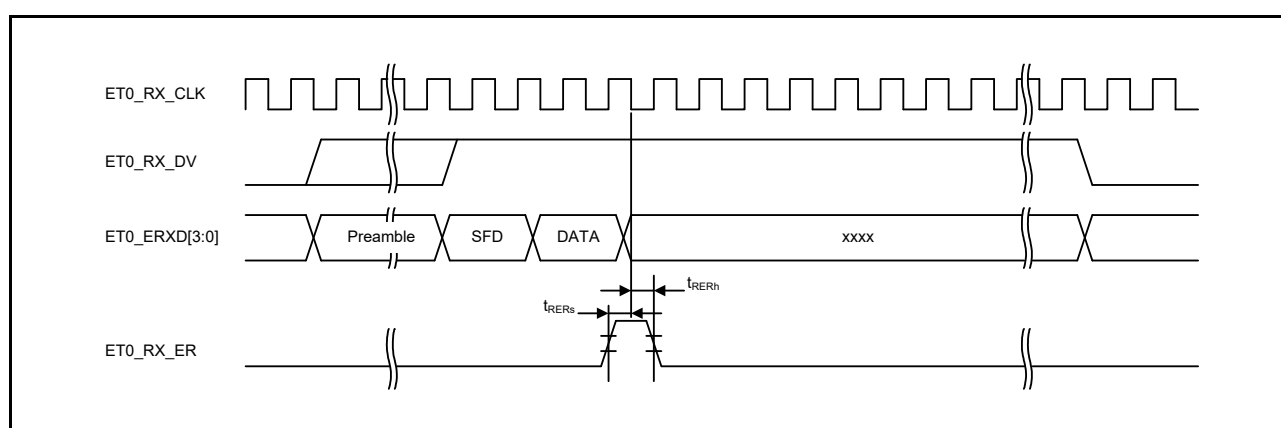


Figure 5.64 MII Reception Timing (Error Occurrence)

5.11 Flash Memory Characteristics

Table 5.54 Code Flash Memory Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N _{PEC} ≤ 100 times	128 bytes	t _{P128}	—	0.75	13.2	—	0.38	6.6	—	0.34	6	ms
	8 Kbytes	t _{P8K}	—	49	176	—	25	88	—	22	80	ms
	32 Kbytes	t _{P32K}	—	194	704	—	97	352	—	88	320	ms
Programming time N _{PEC} > 100 times	128 bytes	t _{P128}	—	0.91	15.8	—	0.46	8	—	0.41	7.2	ms
	8 Kbytes	t _{P8K}	—	60	212	—	30	106	—	27	96	ms
	32 Kbytes	t _{P32K}	—	234	848	—	117	424	—	106	384	ms
Erasure time N _{PEC} ≤ 100 times	8 Kbytes	t _{E8K}	—	78	216	—	48	132	—	43	120	ms
	32 Kbytes	t _{E32K}	—	283	864	—	173	528	—	157	480	ms
Erasure time N _{PEC} > 100 times	8 Kbytes	t _{E8K}	—	94	260	—	58	158	—	52	144	ms
	32 Kbytes	t _{E32K}	—	341	1040	—	208	632	—	189	576	ms
Reprogramming/erasure cycle*1		N _{PEC}	10000 *2	—	—	10000 *2	—	—	10000 *2	—	—	Times
Suspend delay time during programming		t _{SPD}	—	—	264	—	—	132	—	—	120	μs
First suspend delay time during erasing (in suspend priority mode)		t _{SESD1}	—	—	216	—	—	132	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t _{SESD2}	—	—	1.7	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t _{SEED}	—	—	1.7	—	—	1.7	—	—	1.7	ms
Forced stop command		t _{FD}	—	—	32	—	—	22	—	—	20	μs
Data hold time*3		t _{DRP}	10	—	—	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

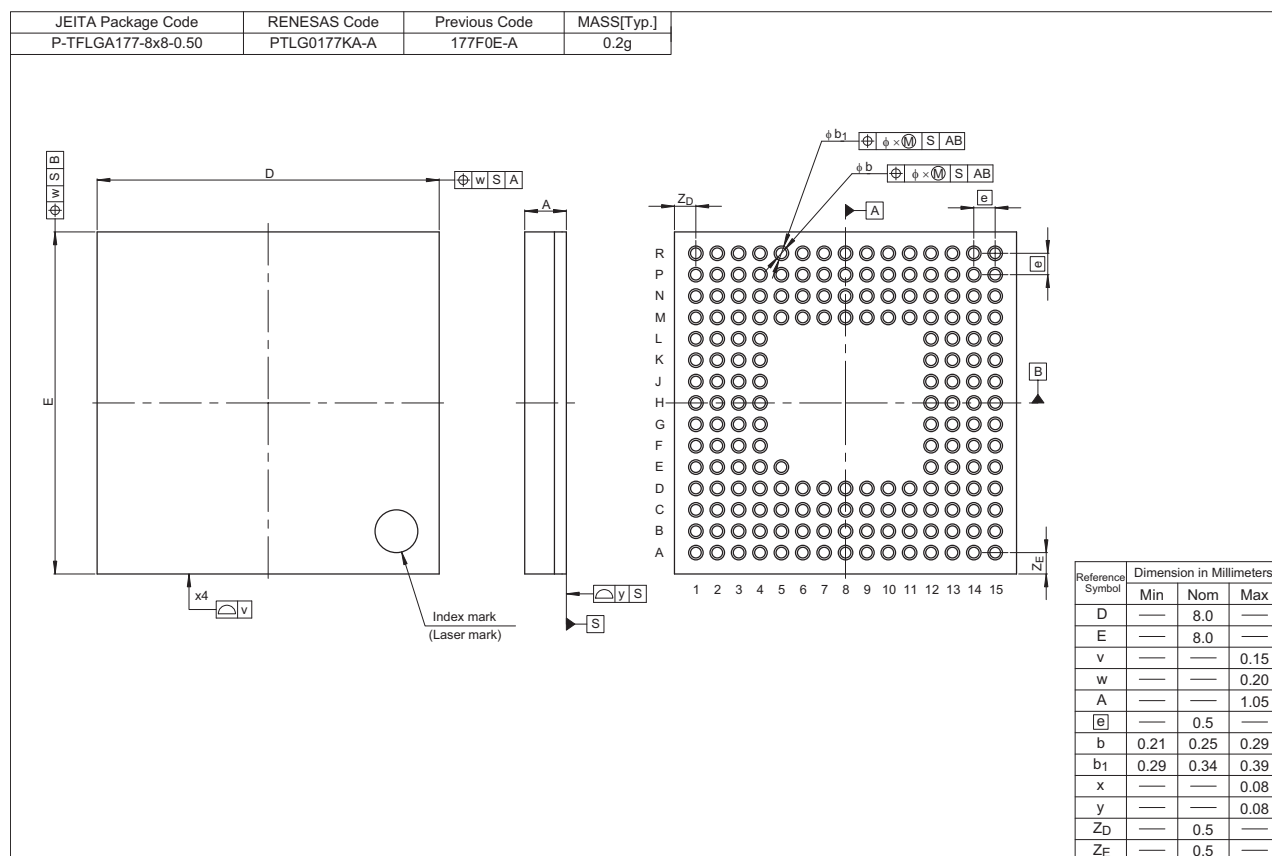


Figure A 177-Pin TFLGA (PTLG0177KA-A)