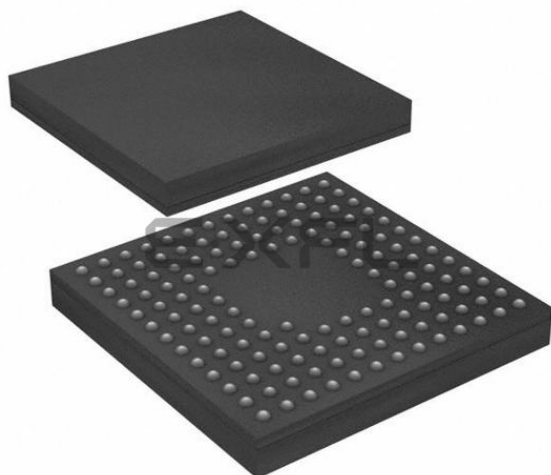




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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n9adlk-20

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
	UB	Input	USB boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC TRSYNC1	Output	This pin indicates that output from the TRDATA0 to TRDATA7 pins is valid.
	TRDATA0 TRDATA1 TRDATA2 TRDATA3 TRDATA4 TRDATA5 TRDATA6 TRDATA7	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock
	SSDA12	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RDX12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	RXD10 and RXD11	Input	Input pin for received data
	TXD10 and TXD11	Output	Output pin for transmitted data
	CTS10# and CTS11#	Input	Input pin for controlling the start of transmission and reception
	RTS10# and RTS11#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL10 and SSCL11	I/O	Input/output pin for the I ² C clock
	SSDA10 and SSDA11	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	SMISO10 and SMISO11	I/O	Input/output pin for slave transmission of data
	SMOSI10 and SMOSI11	I/O	Input/output pin for master transmission of data
	SS10# and SS11#	Input	Chip-select input pin
I ² C bus interface	SCL0[FM+], SCL1, SCL2, SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1, SDA2, SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

Table 1.4 Pin Functions (8/8)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins (P35: input pin)
	P40 to P47	I/O	8-bit input/output pins
	P50 to P57	I/O	8-bit input/output pins
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P87	I/O	8-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF5	I/O	6-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PJ0 to PJ3, PJ5	I/O	5-bit input/output pins

Note: Note the following regarding pin names. For details, see section 1.5, Pin Assignments.

- We recommend using pins that have a letter ("-A", "-B", etc.) to indicate group membership appended to their names as groups.

For the RSPI, QSPI, SDHI, SDSDI, MMC, and GLCDC interfaces, the AC portion of the electrical characteristics is measured for each group.

- Pins that have "-DS" appended to their names can be used as triggers for release from deep software standby.
- RIIC pin functions that have [FM+] appended to their names support fast-mode plus.

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
H13		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DA TA5-B	IRQ6-DS	
H14		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DA TA6-B		
H15	TRDATA3	PG7	D31						
J1	EXTAL	P36							
J2	VCC								
J3		P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
J4	TMS	PF3							
J12		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DA TA3-B		
J13	VSS								
J14		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DA TA1-B		
J15		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DA TA2-B		
K1		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0	PCKO		IRQ3-DS	
K2		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN	VSYN		IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1				
K4	TCK	PF1			SCK1				
K12		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2-B	LCD_TC ON2-B		
K13		P71	A18/CS1#		ET0_MDIO				
K14	VCC								
K15		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DA TA0-B	IRQ12	
L1		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
L2		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1				

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (5/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
87		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DA TA0-B*1	IRQ12	
88		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DA TA1-B*1		
89		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DA TA2-B*1		
90		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DA TA3-B*1		
91	VCC								
92		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DA TA4-B*1	IRQ5-DS	
93	VSS								
94		PA3	A3	MTIOC0D/ MTCLKD/ TIOC0D/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DA TA5-B*1	IRQ6-DS	
95		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DA TA6-B*1		
96		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DA TA7-B*1	IRQ11	
97		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DA TA8-B*1		
98		P67	DQM1/CS7#	MTIOC7C				IRQ15	
99		P66	DQM0/CS6#	MTIOC7D					
100		P65	CKE/CS5#						
101		PE7	D15[A15/ D15]/D7[A7/ D7]*1	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DA TA9-B*1	IRQ7	AN105
102		PE6	D14[A14/ D14]/D6[A6/ D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DA TA10-B*1	IRQ6	AN104
103	VCC								
104		P70	SDCLK						
105	VSS								
106		PE5	D13[A13/ D13]/D5[A5/ D5]*1	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DA TA11-B*1	IRQ5	AN103
107		PE4	D12[A12/ D12]/D4[A4/ D4]*1	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DA TA12-B*1		AN102
108		PE3	D11[A11/ D11]/D3[A3/ D3]*1	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#/SS12#	MMC_D7-B	LCD_DA TA13-B*1		AN101
109		PE2	D10[A10/ D10]/D2[A2/ D2]*1	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3- B	MMC_D6-B	LCD_DA TA14-B*1	IRQ7-DS	AN100

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
45	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A			IRQ14	
46		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A			IRQ13	
47		PC5	D3[A3/D3]*1/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	ET0_ETXD2/ SCK8/SCK10/ RSPCKA-A				
48		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	ET0_TX_CLK/ SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A				
49		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5				
50		PC2	A18	MTIOC4B/ TCLKA/PO21	ET0_RX_DV/ RXD5/SMISO5/ SSCL5/SSLA3-A				
51		PC1	A17	MTIOC3A/ TCLKD/PO18	ET0_ERXD2/ SCK5/SSLA2-A			IRQ12	
52		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
53		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
54		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
55		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CL K-B*1		
56		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TC ON0-B*1		
57		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK6	SDSI_D3-B	LCD_TC ON1-B*1		
58		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS6#/RTS6#/ SS6#	SDSI_D2-B	LCD_TC ON2-B*1		
59		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD6/SMOSI6/ SSDA6		LCD_TC ON3-B*1	IRQ4-DS	

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
79		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DA TA17-B*1	IRQ7	AN107
80		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DA TA18-B*1	IRQ6	AN106
81		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DA TA19-B*1	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DA TA20-B*1	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3- B/MMC_D3-B	LCD_DA TA21-B*1	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2- B/MMC_D2-B	LCD_DA TA22-B*1	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DA TA23-B*1	IRQ1	AN109
86		PD0	D0[A0/D0]	POE4#			LCD_EX TCLK-B *1	IRQ0	AN108
87		P47						IRQ15- DS	AN007
88		P46						IRQ14- DS	AN006
89		P45						IRQ13- DS	AN005
90		P44						IRQ12- DS	AN004
91		P43						IRQ11- DS	AN003
92		P42						IRQ10- DS	AN002
93		P41						IRQ9-DS	AN001
94	VREFL0								
95		P40						IRQ8-DS	AN000
96	VREFH0								
97	AVCC0								
98		P07						IRQ15	ADTRG0 #
99	AVSS0								
100		P05						IRQ13	DA1

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (5 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK		DTCb
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK		DTCb
0008 2410h	DTC	DTC Index Table Base Register	DTCIBR	32	32	2 ICLK		DTCb
0008 2414h	DTC	DTC Operation Register	DTCOR	8	8	2 ICLK		DTCb
0008 2416h	DTC	DTC Sequence Transfer Enable Register	DTCSEQE	16	16	2 ICLK		DTCb
0008 2418h	DTC	DTC Address Displacement Register	DTCDISP	32	32	2 ICLK		DTCb
0008 2800h	EXDMA C0	EXDMA Source Address Register	EDMSAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2804h	EXDMA C0	EXDMA Destination Address Register	EDMDAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2808h	EXDMA C0	EXDMA Transfer Count Register	EDMCRA	32	32	1, 2 BCLK		EXDMA Ca
0008 280Ch	EXDMA C0	EXDMA Block Transfer Count Register	EDMCRB	16	16	1, 2 BCLK		EXDMA Ca
0008 2810h	EXDMA C0	EXDMA Transfer Mode Register	EDMTMD	16	16	1, 2 BCLK		EXDMA Ca
0008 2812h	EXDMA C0	EXDMA Output Setting Register	EDMOMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2813h	EXDMA C0	EXDMA Interrupt Setting Register	EDMINT	8	8	1, 2 BCLK		EXDMA Ca
0008 2814h	EXDMA C0	EXDMA Address Mode Register	EDMAMD	32	32	1, 2 BCLK		EXDMA Ca
0008 2818h	EXDMA C0	EXDMA Offset Register	EDMOFR	32	32	1, 2 BCLK		EXDMA Ca
0008 281Ch	EXDMA C0	EXDMA Transfer Enable Register	EDMCNT	8	8	1, 2 BCLK		EXDMA Ca
0008 281Dh	EXDMA C0	EXDMA Software Start Register	EDMREQ	8	8	1, 2 BCLK		EXDMA Ca
0008 281Eh	EXDMA C0	EXDMA Status Register	EDMSTS	8	8	1, 2 BCLK		EXDMA Ca
0008 2820h	EXDMA C0	EXDMA External Request Sense Mode Register	EDMRMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2821h	EXDMA C0	EXDMA External Request Flag Register	EDMERF	8	8	1, 2 BCLK		EXDMA Ca
0008 2822h	EXDMA C0	EXDMA Peripheral Request Flag Register	EDMPRF	8	8	1, 2 BCLK		EXDMA Ca
0008 2840h	EXDMA C1	EXDMA Source Address Register	EDMSAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2844h	EXDMA C1	EXDMA Destination Address Register	EDMDAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2848h	EXDMA C1	EXDMA Transfer Count Register	EDMCRA	32	32	1, 2 BCLK		EXDMA Ca
0008 284Ch	EXDMA C1	EXDMA Block Transfer Count Register	EDMCRB	16	16	1, 2 BCLK		EXDMA Ca
0008 2850h	EXDMA C1	EXDMA Transfer Mode Register	EDMTMD	16	16	1, 2 BCLK		EXDMA Ca
0008 2852h	EXDMA C1	EXDMA Output Setting Register	EDMOMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2853h	EXDMA C1	EXDMA Interrupt Setting Register	EDMINT	8	8	1, 2 BCLK		EXDMA Ca
0008 2854h	EXDMA C1	EXDMA Address Mode Register	EDMAMD	32	32	1, 2 BCLK		EXDMA Ca
0008 285Ch	EXDMA C1	EXDMA Transfer Enable Register	EDMCNT	8	8	1, 2 BCLK		EXDMA Ca
0008 285Dh	EXDMA C1	EXDMA Software Start Register	EDMREQ	8	8	1, 2 BCLK		EXDMA Ca
0008 285Eh	EXDMA C1	EXDMA Status Register	EDMSTS	8	8	1, 2 BCLK		EXDMA Ca
0008 2860h	EXDMA C1	EXDMA External Request Sense Mode Register	EDMRMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2861h	EXDMA C1	EXDMA External Request Flag Register	EDMERF	8	8	1, 2 BCLK		EXDMA Ca

Table 4.1 List of I/O Registers (Address Order) (10 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 779Dh	ICU	Software Configurable Interrupt B Source Select Register 157	SLIBR157	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Eh	ICU	Software Configurable Interrupt B Source Select Register 158	SLIBR158	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 779Fh	ICU	Software Configurable Interrupt B Source Select Register 159	SLIBR159	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A0h	ICU	Software Configurable Interrupt B Source Select Register 160	SLIBR160	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A1h	ICU	Software Configurable Interrupt B Source Select Register 161	SLIBR161	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A2h	ICU	Software Configurable Interrupt B Source Select Register 162	SLIBR162	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A3h	ICU	Software Configurable Interrupt B Source Select Register 163	SLIBR163	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A4h	ICU	Software Configurable Interrupt B Source Select Register 164	SLIBR164	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A5h	ICU	Software Configurable Interrupt B Source Select Register 165	SLIBR165	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A6h	ICU	Software Configurable Interrupt B Source Select Register 166	SLIBR166	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A7h	ICU	Software Configurable Interrupt B Source Select Register 167	SLIBR167	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A8h	ICU	Software Configurable Interrupt B Source Select Register 168	SLIBR168	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77A9h	ICU	Software Configurable Interrupt B Source Select Register 169	SLIBR169	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AAh	ICU	Software Configurable Interrupt B Source Select Register 170	SLIBR170	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ABh	ICU	Software Configurable Interrupt B Source Select Register 171	SLIBR171	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ACh	ICU	Software Configurable Interrupt B Source Select Register 172	SLIBR172	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77ADh	ICU	Software Configurable Interrupt B Source Select Register 173	SLIBR173	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AEh	ICU	Software Configurable Interrupt B Source Select Register 174	SLIBR174	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77AFh	ICU	Software Configurable Interrupt B Source Select Register 175	SLIBR175	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B0h	ICU	Software Configurable Interrupt B Source Select Register 176	SLIBR176	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B1h	ICU	Software Configurable Interrupt B Source Select Register 177	SLIBR177	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B2h	ICU	Software Configurable Interrupt B Source Select Register 178	SLIBR178	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B3h	ICU	Software Configurable Interrupt B Source Select Register 179	SLIBR179	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B4h	ICU	Software Configurable Interrupt B Source Select Register 180	SLIBR180	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B5h	ICU	Software Configurable Interrupt B Source Select Register 181	SLIBR181	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B6h	ICU	Software Configurable Interrupt B Source Select Register 182	SLIBR182	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B7h	ICU	Software Configurable Interrupt B Source Select Register 183	SLIBR183	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B8h	ICU	Software Configurable Interrupt B Source Select Register 184	SLIBR184	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77B9h	ICU	Software Configurable Interrupt B Source Select Register 185	SLIBR185	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BAh	ICU	Software Configurable Interrupt B Source Select Register 186	SLIBR186	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BBh	ICU	Software Configurable Interrupt B Source Select Register 187	SLIBR187	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (12 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 79D2h	ICU	Software Configurable Interrupt A Source Select Register 210	SLIAR210	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D3h	ICU	Software Configurable Interrupt A Source Select Register 211	SLIAR211	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D4h	ICU	Software Configurable Interrupt A Source Select Register 212	SLIAR212	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D5h	ICU	Software Configurable Interrupt A Source Select Register 213	SLIAR213	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D6h	ICU	Software Configurable Interrupt A Source Select Register 214	SLIAR214	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D7h	ICU	Software Configurable Interrupt A Source Select Register 215	SLIAR215	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D8h	ICU	Software Configurable Interrupt A Source Select Register 216	SLIAR216	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D9h	ICU	Software Configurable Interrupt A Source Select Register 217	SLIAR217	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DAh	ICU	Software Configurable Interrupt A Source Select Register 218	SLIAR218	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DBh	ICU	Software Configurable Interrupt A Source Select Register 219	SLIAR219	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DCh	ICU	Software Configurable Interrupt A Source Select Register 220	SLIAR220	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DDh	ICU	Software Configurable Interrupt A Source Select Register 221	SLIAR221	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DEh	ICU	Software Configurable Interrupt A Source Select Register 222	SLIAR222	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DFh	ICU	Software Configurable Interrupt A Source Select Register 223	SLIAR223	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E0h	ICU	Software Configurable Interrupt A Source Select Register 224	SLIAR224	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E1h	ICU	Software Configurable Interrupt A Source Select Register 225	SLIAR225	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E2h	ICU	Software Configurable Interrupt A Source Select Register 226	SLIAR226	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E3h	ICU	Software Configurable Interrupt A Source Select Register 227	SLIAR227	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E4h	ICU	Software Configurable Interrupt A Source Select Register 228	SLIAR228	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E5h	ICU	Software Configurable Interrupt A Source Select Register 229	SLIAR229	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E6h	ICU	Software Configurable Interrupt A Source Select Register 230	SLIAR230	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E7h	ICU	Software Configurable Interrupt A Source Select Register 231	SLIAR231	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E8h	ICU	Software Configurable Interrupt A Source Select Register 232	SLIAR232	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E9h	ICU	Software Configurable Interrupt A Source Select Register 233	SLIAR233	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EAh	ICU	Software Configurable Interrupt A Source Select Register 234	SLIAR234	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EBh	ICU	Software Configurable Interrupt A Source Select Register 235	SLIAR235	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79ECh	ICU	Software Configurable Interrupt A Source Select Register 236	SLIAR236	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EDh	ICU	Software Configurable Interrupt A Source Select Register 237	SLIAR237	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EEh	ICU	Software Configurable Interrupt A Source Select Register 238	SLIAR238	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EFh	ICU	Software Configurable Interrupt A Source Select Register 239	SLIAR239	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F0h	ICU	Software Configurable Interrupt A Source Select Register 240	SLIAR240	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (33 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B131h	ELC	Event Link Setting Register 33	ELSR33	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B133h	ELC	Event Link Setting Register 35	ELSR35	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B134h	ELC	Event Link Setting Register 36	ELSR36	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B135h	ELC	Event Link Setting Register 37	ELSR37	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B136h	ELC	Event Link Setting Register 38	ELSR38	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Dh	ELC	Event Link Setting Register 45	ELSR45	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Fh	ELC	Event Link Option Setting Register F	ELOPF	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B141h	ELC	Event Link Option Setting Register H	ELOPH	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIh

Table 4.1 List of I/O Registers (Address Order) (57 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 011Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0120h	RSPI0	RSPI Data Control Register 2	SPDCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0140h	RSPI1	RSPI Control Register	SPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0141h	RSPI1	RSPI Slave Select Polarity Register	SSLP	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0142h	RSPI1	RSPI Pin Control Register	SPPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0143h	RSPI1	RSPI Status Register	SPSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0144h	RSPI1	RSPI Data Register	SPDR	32	8, 16, 32	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0148h	RSPI1	RSPI Sequence Control Register	SPSCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0149h	RSPI1	RSPI Sequence Status Register	SPSSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Ah	RSPI1	RSPI Bit Rate Register	SPBR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Bh	RSPI1	RSPI Data Control Register	SPDCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Ch	RSPI1	RSPI Clock Delay Register	SPCKD	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Dh	RSPI1	RSPI Slave Select Negation Delay Register	SSLND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Eh	RSPI1	RSPI Next-Access Delay Register	SPND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Fh	RSPI1	RSPI Control Register 2	SPCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0150h	RSPI1	RSPI Command Register 0	SPCMD0	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0152h	RSPI1	RSPI Command Register 1	SPCMD1	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0154h	RSPI1	RSPI Command Register 2	SPCMD2	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0156h	RSPI1	RSPI Command Register 3	SPCMD3	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0158h	RSPI1	RSPI Command Register 4	SPCMD4	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 015Ah	RSPI1	RSPI Command Register 5	SPCMD5	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 015Ch	RSPI1	RSPI Command Register 6	SPCMD6	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 015Eh	RSPI1	RSPI Command Register 7	SPCMD7	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0160h	RSPI1	RSPI Data Control Register 2	SPDCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0300h	RSPI2	RSPI Control Register	SPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0301h	RSPI2	RSPI Slave Select Polarity Register	SSLP	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0302h	RSPI2	RSPI Pin Control Register	SPPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0303h	RSPI2	RSPI Status Register	SPSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0304h	RSPI2	RSPI Data Register	SPDR	32	8, 16, 32	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0308h	RSPI2	RSPI Sequence Control Register	SPSCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0309h	RSPI2	RSPI Sequence Status Register	SPSSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Ah	RSPI2	RSPI Bit Rate Register	SPBR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Bh	RSPI2	RSPI Data Control Register	SPDCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Ch	RSPI2	RSPI Clock Delay Register	SPCKD	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Dh	RSPI2	RSPI Slave Select Negation Delay Register	SSLND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Eh	RSPI2	RSPI Next-Access Delay Register	SPND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Fh	RSPI2	RSPI Control Register 2	SPCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0310h	RSPI2	RSPI Command Register 0	SPCMD0	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0312h	RSPI2	RSPI Command Register 1	SPCMD1	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0314h	RSPI2	RSPI Command Register 2	SPCMD2	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0316h	RSPI2	RSPI Command Register 3	SPCMD3	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0318h	RSPI2	RSPI Command Register 4	SPCMD4	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 031Ah	RSPI2	RSPI Command Register 5	SPCMD5	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 031Ch	RSPI2	RSPI Command Register 6	SPCMD6	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 031Eh	RSPI2	RSPI Command Register 7	SPCMD7	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0320h	RSPI2	RSPI Data Control Register 2	SPDCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000E 0000h to 000E 03FCh	GLCDC	Graphic 1 Color Look-up Table 0[0 to 255]	GR1CLUT0[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC

Table 4.1 List of I/O Registers (Address Order) (59 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000E 1300h	GLCDC	Gamma Correction G Block Register Update Control Register	GAMGVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1304h	GLCDC	Gamma Correction Block Function Switch Register	GAMSW	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1308h	GLCDC	Gamma Correction G Table Setting Register 1	GAMGLUT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 130Ch	GLCDC	Gamma Correction G Table Setting Register 2	GAMGLUT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1310h	GLCDC	Gamma Correction G Table Setting Register 3	GAMGLUT3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1314h	GLCDC	Gamma Correction G Table Setting Register 4	GAMGLUT4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1318h	GLCDC	Gamma Correction G Table Setting Register 5	GAMGLUT5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 131Ch	GLCDC	Gamma Correction G Table Setting Register 6	GAMGLUT6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1320h	GLCDC	Gamma Correction G Table Setting Register 7	GAMGLUT7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1324h	GLCDC	Gamma Correction G Table Setting Register 8	GAMGLUT8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1328h	GLCDC	Gamma Correction G Area Setting Register 1	GAMGAREA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 132Ch	GLCDC	Gamma Correction G Area Setting Register 2	GAMGAREA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1330h	GLCDC	Gamma Correction G Area Setting Register 3	GAMGAREA3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1334h	GLCDC	Gamma Correction G Area Setting Register 4	GAMGAREA4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1338h	GLCDC	Gamma Correction G Area Setting Register 5	GAMGAREA5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1340h	GLCDC	Gamma Correction B Block Register Update Control Register	GAMBVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1348h	GLCDC	Gamma Correction B Table Setting Register 1	GAMBLUT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 134Ch	GLCDC	Gamma Correction B Table Setting Register 2	GAMBLUT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1350h	GLCDC	Gamma Correction B Table Setting Register 3	GAMBLUT3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1354h	GLCDC	Gamma Correction B Table Setting Register 4	GAMBLUT4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1358h	GLCDC	Gamma Correction B Table Setting Register 5	GAMBLUT5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 135Ch	GLCDC	Gamma Correction B Table Setting Register 6	GAMBLUT6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1360h	GLCDC	Gamma Correction B Table Setting Register 7	GAMBLUT7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1364h	GLCDC	Gamma Correction B Table Setting Register 8	GAMBLUT8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1368h	GLCDC	Gamma Correction B Area Setting Register 1	GAMBAREA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 136Ch	GLCDC	Gamma Correction B Area Setting Register 2	GAMBAREA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1370h	GLCDC	Gamma Correction B Area Setting Register 3	GAMBAREA3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1374h	GLCDC	Gamma Correction B Area Setting Register 4	GAMBAREA4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1378h	GLCDC	Gamma Correction B Area Setting Register 5	GAMBAREA5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1380h	GLCDC	Gamma Correction R Block Register Update Control Register	GAMRVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1388h	GLCDC	Gamma Correction R Table Setting Register 1	GAMRLUT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 138Ch	GLCDC	Gamma Correction R Table Setting Register 2	GAMRLUT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1390h	GLCDC	Gamma Correction R Table Setting Register 3	GAMRLUT3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1394h	GLCDC	Gamma Correction R Table Setting Register 4	GAMRLUT4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 1398h	GLCDC	Gamma Correction R Table Setting Register 5	GAMRLUT5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 139Ch	GLCDC	Gamma Correction R Table Setting Register 6	GAMRLUT6	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13A0h	GLCDC	Gamma Correction R Table Setting Register 7	GAMRLUT7	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13A4h	GLCDC	Gamma Correction R Table Setting Register 8	GAMRLUT8	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13A8h	GLCDC	Gamma Correction R Area Setting Register 1	GAMRAREA1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13ACh	GLCDC	Gamma Correction R Area Setting Register 2	GAMRAREA2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13B0h	GLCDC	Gamma Correction R Area Setting Register 3	GAMRAREA3	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13B4h	GLCDC	Gamma Correction R Area Setting Register 4	GAMRAREA4	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13B8h	GLCDC	Gamma Correction R Area Setting Register 5	GAMRAREA5	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13C0h	GLCDC	Output Control Block Register Update Control Register	OUTVEN	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13C4h	GLCDC	Output Interface Register	OUTSET	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13C8h	GLCDC	Brightness Adjustment Register 1	BRIGHT1	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC
000E 13CCh	GLCDC	Brightness Adjustment Register 2	BRIGHT2	32	32	2, 3 PCLKA	1, 2 ICLK	GLCDC

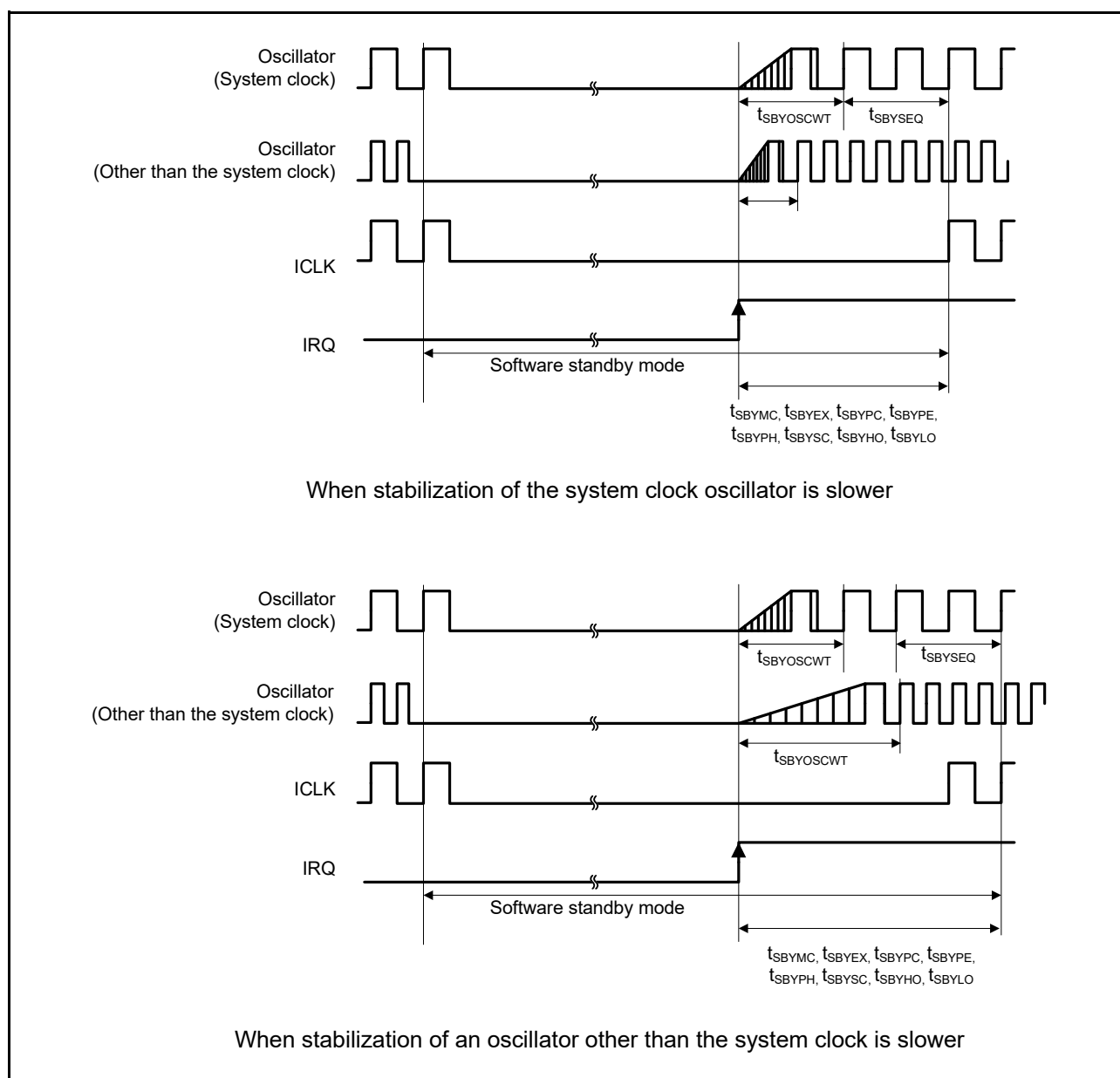
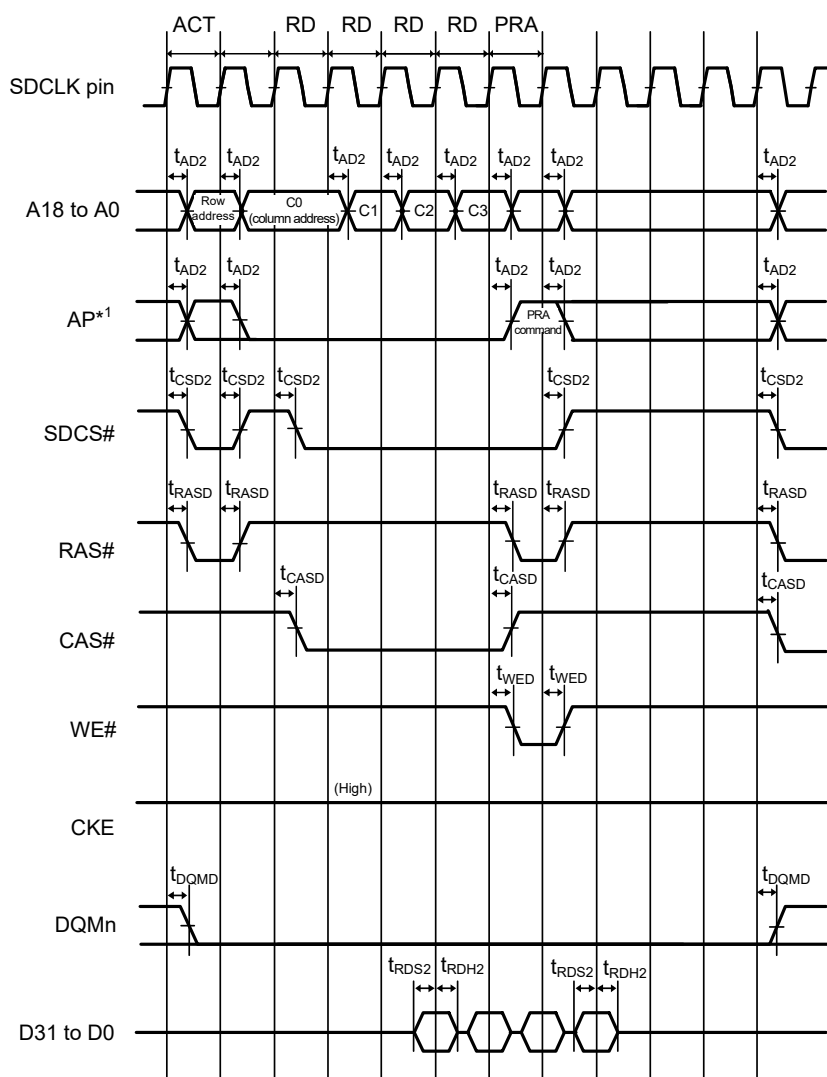


Figure 5.12 Software Standby Mode Cancellation Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.25 SDRAM Space Multiple Read Bus Timing

Table 5.41 ETHERC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.56 to Figure 5.58
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII0_xxx*2 setup time	T_{su}	3	—	ns	
	RMII0_xxx*2 hold time	T_{hd}	1	—	ns	
	RMII0_xxx*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.60
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET0_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.61
	ET0_ETXD0 to ET0_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET0_CRS setup time	t_{CRSs}	10	—	ns	
	ET0_CRS hold time	t_{CRSh}	10	—	ns	
	ET0_COL setup time	t_{COLs}	10	—	ns	Figure 5.62
	ET0_COL hold time	t_{COLh}	10	—	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET0_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 5.63
	ET0_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET0_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.64
	ET0_RX_ER hold time	t_{RERh}	10	—	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.65

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0

Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

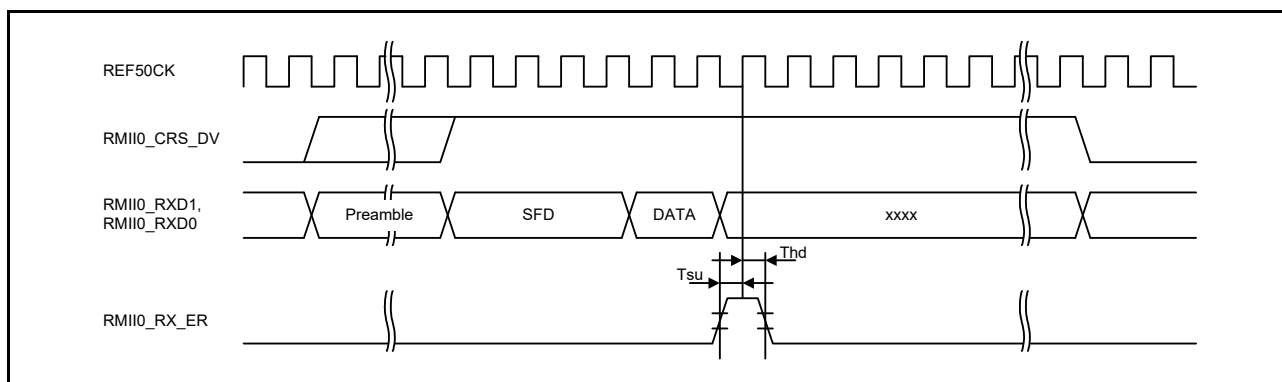


Figure 5.59 RMII Reception Timing (Error Occurrence)

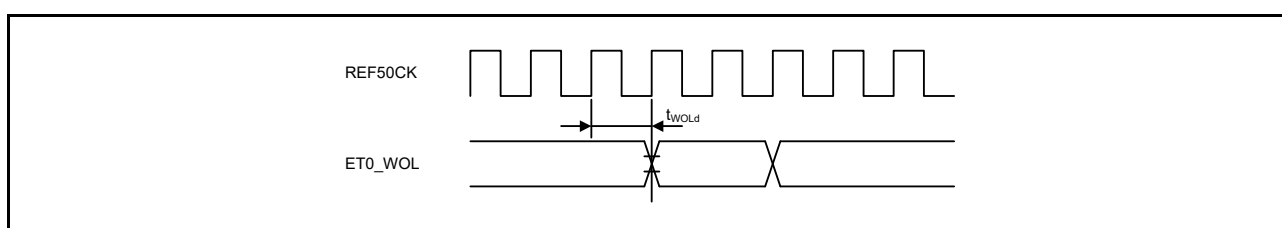


Figure 5.60 WOL Output Timing (RMII)

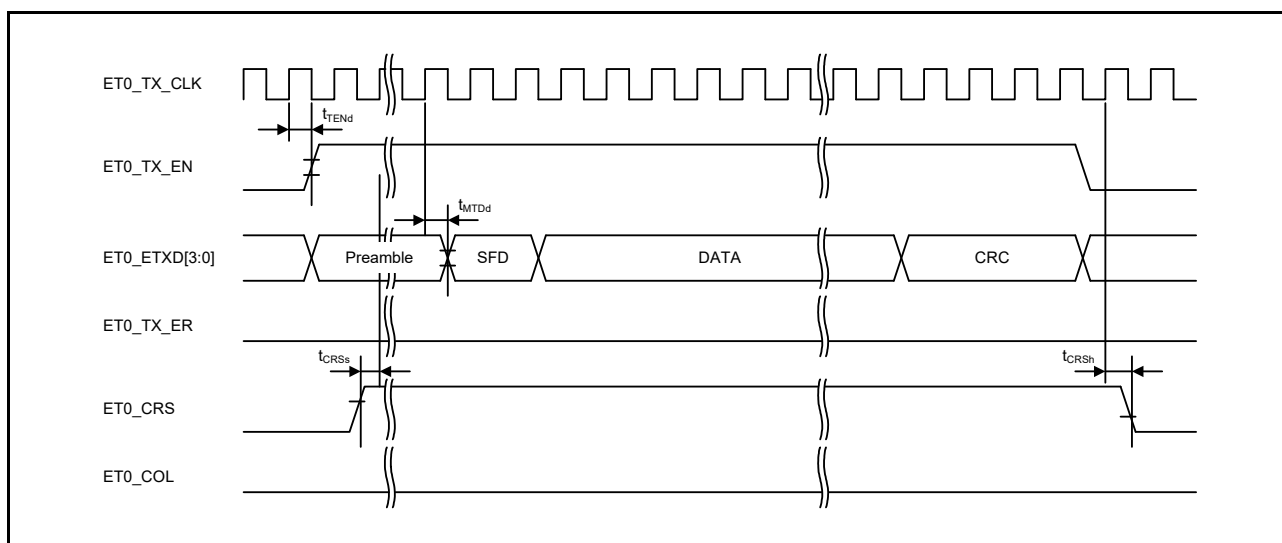
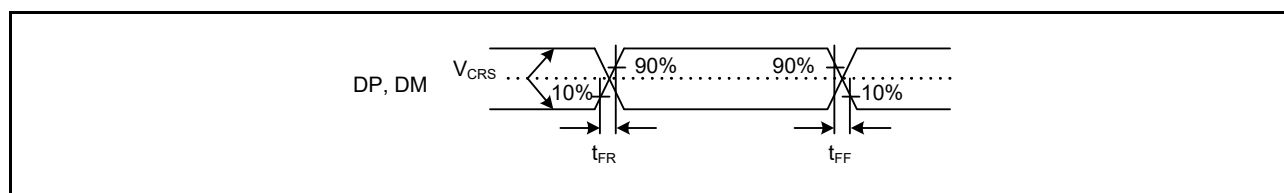
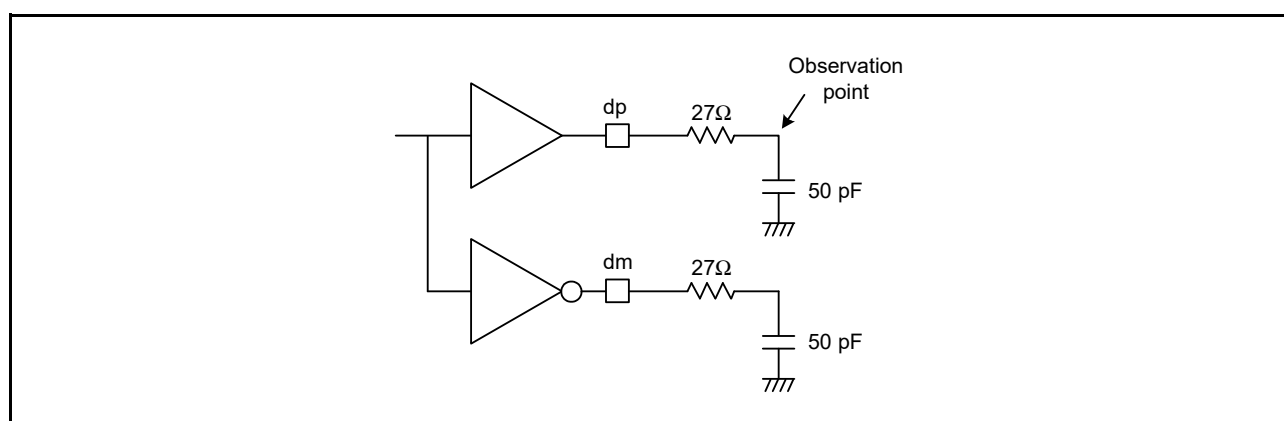


Figure 5.61 MII Transmission Timing (Normal Operation)

Table 5.45 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $3.0 \leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $U_{CLK} = 48$ MHz,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V
	Input low level voltage	V_{IL}	—	—	0.8	V
	Differential input sensitivity	V_{DI}	0.2	—	—	V
	Differential common mode range	V_{CM}	0.8	—	2.5	V
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V
	Output low level voltage	V_{OL}	0.0	—	0.3	V
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V
	Rise time	t_{FR}	4	—	20	ns
	Fall time	t_{FF}	4	—	20	ns
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	%
	Output resistance	Z_{DRV}	28	—	44	Ω
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	k Ω
			1.425	—	3.090	k Ω
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	k Ω

**Figure 5.74 DP and DM Output Timing (Full-Speed)****Figure 5.75 Test Circuit (Full-Speed)**

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.