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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565n9bdlj-20

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.

Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, see Table 1.2, Code Flash Memory Capacity and Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 120 MHz 32-bit RX CPU (RXv2) - Minimum instruction execution time: One instruction per state (cycle of the system clock) - Address space: 4-Gbyte linear - Register set of the CPU - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers - Basic instructions: 75 - Floating-point instructions: 11 - DSP instructions: 23 - Addressing modes: 11 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: $32 \times 32 \rightarrow 64$ bits - On-chip divider: $32 / 32 \rightarrow 32$ bits - Barrel shifter: 32 bits
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	- Capacity: 512 Kbytes/768 Kbytes/1 Mbyte/1.5 Mbytes/2 Mbytes $50 \text{ MHz} \leq$ No-wait cycle access $100 \text{ MHz} \leq$ 1-wait cycle access $100 \text{ MHz} \geq$ 2-wait cycle access - Instructions hitting the ROM cache or operand = 120 MHz: No-wait access - On-board programming: Four types - Off-board programming (parallel programmer mode) - Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. - A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	- Capacity: 32 Kbytes - Programming/erasing: 100,000 times
	RAM	- Capacity: 256 Kbytes (Products with 1 Mbyte of code flash memory or less) - RAM: 256 Kbytes - Capacity: 640 Kbytes (Products with at least 1.5 Mbytes of code flash memory) - RAM: 256 Kbytes - Expansion RAM: 384 Kbytes 120 MHz, no-wait access
	Standby RAM	- Capacity: 8 Kbytes - Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access

Table 1.3 List of Products (2/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N7ADFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NEDDLK	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLK	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDLK	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLK	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NEDDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (6/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
M14		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CL K-B		
M15		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TC ON0-B		
N1	VCC								
N2		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C/PIXD7			
N3		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C/PIXD6			
N4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMC12/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	
N5		P12	WR3#/BC3#	MTIC5U/ TMC11	RXD2/SMISO2/ SSCL2/ SCL0[FM+]		LCD_TC ON1-A	IRQ2	
N6		PJ0		MTIOC6B	SCK8/SSLC1-B		LCD_DA TA0-A		
N7		P84		MTIOC6D			LCD_DA TA2-A		
N8		P54	D1[A1/D1]/ EDACK0	MTIOC4B/ TMC11	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1		LCD_DA TA6-A		
N9		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
N10	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A	MMC_D7-A	LCD_DA TA9-A	IRQ14	
N11		P82	EDREQ1	MTIOC4A/ PO28	ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/TXD10	MMC_D4-A	LCD_DA TA12-A		
N12		PC3	A19	MTIOC4D/ TCLKB/PO24	ET0_TX_ER/ TXD5/SMOSI5/ SSDA5	QMO-A/QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A	LCD_DA TA16-A		
N13		PC0	A16	MTIOC3C/ TCLKC/PO17	ET0_ERXD3/ CTS5#/RTS5#/ SS5#/SSLA1-A			IRQ14	
N14		P73	CS3#	PO16	ET0_WOL		LCD_EX TCLK-A		
N15	VSS								
P1	VSS								
P2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C/PIXD3		IRQ7	ADTRG1 #

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (1/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
1	AVSS0								
2		P05						IRQ13	DA1
3	AVCC1								
4		P03						IRQ11	DA0
5	AVSS1								
6		P02		TMC11	SCK6			IRQ10	AN120
7		P01		TMC10	RXD6/SMISO6/SSCL6			IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/SSDA6			IRQ8	AN118
9		PF5						IRQ4	
10	EMLE								
11		PJ5		POE8#	CTS2#/RTS2#/SS2#				
12	VSS								
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#				
14	VCL								
15	VBATT								
16	NC								
17	TRST#	PF4							
18	MD/FINED								
19	XCIN								
20	XCOUT								
21	RES#								
22	XTAL	P37							
23	VSS								
24	EXTAL	P36							
25	VCC								
26	UPSEL	P35						NMI	
27		P34		MTIOC0A/TMC13/PO12/POE10#	ET0_LINKSTA/SCK6/SCK0			IRQ4	
28		P33	EDREQ1	MTIOC0D/TIOC0D/TMRI3/PO11/POE4#/POE11#	RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0	PCKO		IRQ3-DS	
29		P32		MTIOC0C/TIOC0C/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#	TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN	VSYN		IRQ2-DS	
30	TMS	PF3							
31	TDI	PF2			RXD1/SMISO1/SSCL1				

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (2/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
32		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
33		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
34	TCK	PF1			SCK1				
35	TDO	PF0			TXD1/SMOSI1/ SSDA1				
36		P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB- A				
37		P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
38		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0 #
39	VCC								
40		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
41	VSS								
42		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C/PIXD7			
43		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C/PIXD6			
44		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN	SDHI_CLK-C/ PIXD5		IRQ9	
45		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID	SDHI_CMD-C/ PIXD4		IRQ8	
46		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C/PIXD3		IRQ7	ADTRG1 #
47		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C/PIXD2			
48		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
49		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
50		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
H1	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
H2		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3				ADTRG0 #
H3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOU	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
H4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMC12/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS			IRQ5	
H5		P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ CRX1			IRQ10	
H6		P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMC11	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
H7	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A			IRQ14	
H8		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMC12/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A			IRQ13	
H9		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
H10		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMISO9/ SSDA9/ SMISO11/ SSDA11/TXD11	SDSI_D1-B			
J1		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN				
J2		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN			IRQ9	
J3		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS			IRQ7	ADTRG1 #
J4		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1 #
J5	VSS_USB								

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
79		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DA TA17-B*1	IRQ7	AN107
80		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DA TA18-B*1	IRQ6	AN106
81		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DA TA19-B*1	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DA TA20-B*1	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3- B/MMC_D3-B	LCD_DA TA21-B*1	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2- B/MMC_D2-B	LCD_DA TA22-B*1	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DA TA23-B*1	IRQ1	AN109
86		PD0	D0[A0/D0]	POE4#			LCD_EX TCLK-B *1	IRQ0	AN108
87		P47						IRQ15- DS	AN007
88		P46						IRQ14- DS	AN006
89		P45						IRQ13- DS	AN005
90		P44						IRQ12- DS	AN004
91		P43						IRQ11- DS	AN003
92		P42						IRQ10- DS	AN002
93		P41						IRQ9-DS	AN001
94	VREFL0								
95		P40						IRQ8-DS	AN000
96	VREFH0								
97	AVCC0								
98		P07						IRQ15	ADTRG0 #
99	AVSS0								
100		P05						IRQ13	DA1

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM areas (SDCS) in on-chip ROM disabled extended mode.

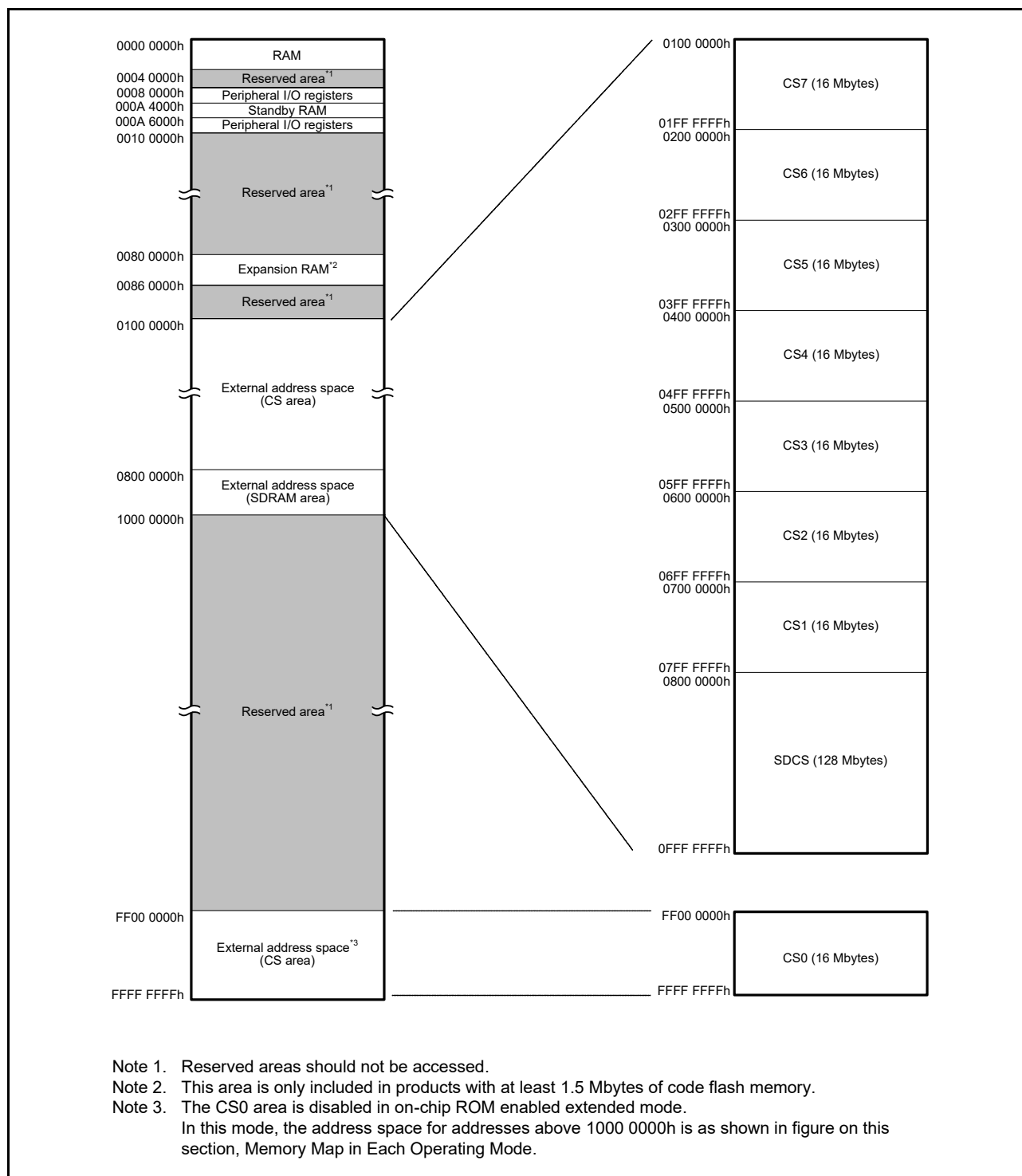


Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).

The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
 Number of divided clock synchronization cycles +
 Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

(5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

Table 4.1 List of I/O Registers (Address Order) (11 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 77BCh	ICU	Software Configurable Interrupt B Source Select Register 188	SLIBR188	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BDh	ICU	Software Configurable Interrupt B Source Select Register 189	SLIBR189	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BEh	ICU	Software Configurable Interrupt B Source Select Register 190	SLIBR190	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77BFh	ICU	Software Configurable Interrupt B Source Select Register 191	SLIBR191	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C0h	ICU	Software Configurable Interrupt B Source Select Register 192	SLIBR192	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C1h	ICU	Software Configurable Interrupt B Source Select Register 193	SLIBR193	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C2h	ICU	Software Configurable Interrupt B Source Select Register 194	SLIBR194	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C3h	ICU	Software Configurable Interrupt B Source Select Register 195	SLIBR195	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C4h	ICU	Software Configurable Interrupt B Source Select Register 196	SLIBR196	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C5h	ICU	Software Configurable Interrupt B Source Select Register 197	SLIBR197	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C6h	ICU	Software Configurable Interrupt B Source Select Register 198	SLIBR198	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C7h	ICU	Software Configurable Interrupt B Source Select Register 199	SLIBR199	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C8h	ICU	Software Configurable Interrupt B Source Select Register 200	SLIBR200	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77C9h	ICU	Software Configurable Interrupt B Source Select Register 201	SLIBR201	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CAh	ICU	Software Configurable Interrupt B Source Select Register 202	SLIBR202	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CBh	ICU	Software Configurable Interrupt B Source Select Register 203	SLIBR203	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CCh	ICU	Software Configurable Interrupt B Source Select Register 204	SLIBR204	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CDh	ICU	Software Configurable Interrupt B Source Select Register 205	SLIBR205	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CEh	ICU	Software Configurable Interrupt B Source Select Register 206	SLIBR206	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 77CFh	ICU	Software Configurable Interrupt B Source Select Register 207	SLIBR207	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUB
0008 7830h	ICU	Group AL0 Interrupt Request Register	GRPAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7834h	ICU	Group AL1 Interrupt Request Register	GRPAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7870h	ICU	Group AL0 Interrupt Request Enable Register	GENAL0	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7874h	ICU	Group AL1 Interrupt Request Enable Register	GENAL1	32	32	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7900h	ICU	Software Configurable Interrupt A Request Register 0	PIAR0	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7901h	ICU	Software Configurable Interrupt A Request Register 1	PIAR1	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7902h	ICU	Software Configurable Interrupt A Request Register 2	PIAR2	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7903h	ICU	Software Configurable Interrupt A Request Register 3	PIAR3	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7904h	ICU	Software Configurable Interrupt A Request Register 4	PIAR4	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7905h	ICU	Software Configurable Interrupt A Request Register 5	PIAR5	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 790Bh	ICU	Software Configurable Interrupt A Request Register B	PIARB	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D0h	ICU	Software Configurable Interrupt A Source Select Register 208	SLIAR208	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D1h	ICU	Software Configurable Interrupt A Source Select Register 209	SLIAR209	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (22 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 91E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E4h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E5h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E6h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E7h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E8h	S12AD1	A/D Sampling State Register 8	ADSSTR8	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E9h	S12AD1	A/D Sampling State Register 9	ADSSTR9	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EAh	S12AD1	A/D Sampling State Register 10	ADSSTR10	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EBh	S12AD1	A/D Sampling State Register 11	ADSSTR11	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91ECh	S12AD1	A/D Sampling State Register 12	ADSSTR12	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EDh	S12AD1	A/D Sampling State Register 13	ADSSTR13	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EEh	S12AD1	A/D Sampling State Register 14	ADSSTR14	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EFh	S12AD1	A/D Sampling State Register 15	ADSSTR15	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Set Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E24h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 2	SPBMUL2	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E28h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 3	SPBMUL3	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 A000h	SCIO	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, SCli
0008 A001h	SCIO	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (25 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A046h	SMCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A049h	SCI2	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Ah	SCI2	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Bh	SCI2	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Ch	SCI2	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Eh	SCI2	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Fh	SCI2	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A04Eh	SCI2	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A050h	SCI2	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A051h	SCI2	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A050h	SCI2	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A052h	SCI2	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A066h	SMCI3	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, Scli

Table 4.1 List of I/O Registers (Address Order) (28 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (29 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E0h	SCI7	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E1h	SCI7	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E2h	SCI7	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E3h	SCI7	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E4h	SCI7	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E5h	SCI7	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E6h	SMCI7	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E7h	SCI7	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E8h	SCI7	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0E9h	SCI7	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0EAh	SCI7	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0EBh	SCI7	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0ECh	SCI7	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0EDh	SCI7	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0EEh	SCI7	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0EFh	SCI7	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i

Table 4.1 List of I/O Registers (Address Order) (37 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C086h	PORT3	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C087h	PORT3	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C088h	PORT4	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C089h	PORT4	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C08Ah	PORT5	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C08Bh	PORT5	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C08Ch	PORT6	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C08Dh	PORT6	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C08Eh	PORT7	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C08Fh	PORT7	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C090h	PORT8	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C091h	PORT8	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C092h	PORT9	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C093h	PORT9	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C094h	PORTA	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C095h	PORTA	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C096h	PORTB	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C097h	PORTB	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C098h	PORTC	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C099h	PORTC	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Ah	PORTD	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Bh	PORTD	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Ch	PORTE	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Dh	PORTE	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Eh	PORTF	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Fh	PORTF	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A0h	PORTG	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A1h	PORTG	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A4h	PORTJ	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A5h	PORTJ	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C0h	PORT0	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports

Table 5.22 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: $V_{CC} = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq VREFH0 \leq AVCC0$,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 5.13
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	23	—	24	t_{Lcyc}	

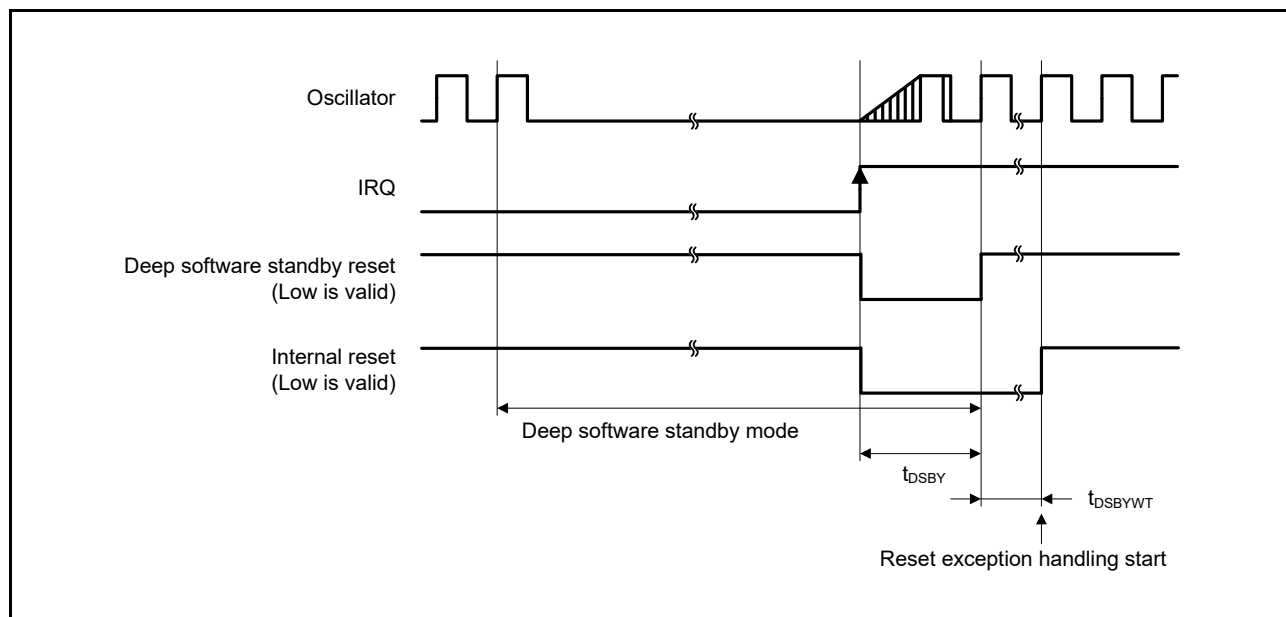
**Figure 5.13 Deep Software Standby Mode Cancellation Timing**

Table 5.41 ETHERC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.56 to Figure 5.58
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII0_xxx*2 setup time	T_{su}	3	—	ns	
	RMII0_xxx*2 hold time	T_{hd}	1	—	ns	
	RMII0_xxx*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.60
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET0_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.61
	ET0_ETXD0 to ET0_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET0_CRS setup time	t_{CRSs}	10	—	ns	
	ET0_CRS hold time	t_{CRSh}	10	—	ns	
	ET0_COL setup time	t_{COLs}	10	—	ns	Figure 5.62
	ET0_COL hold time	t_{COLh}	10	—	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET0_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 5.63
	ET0_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET0_ERXD0 to ET0_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET0_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.64
	ET0_RX_ER hold time	t_{RERh}	10	—	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.65

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0

Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

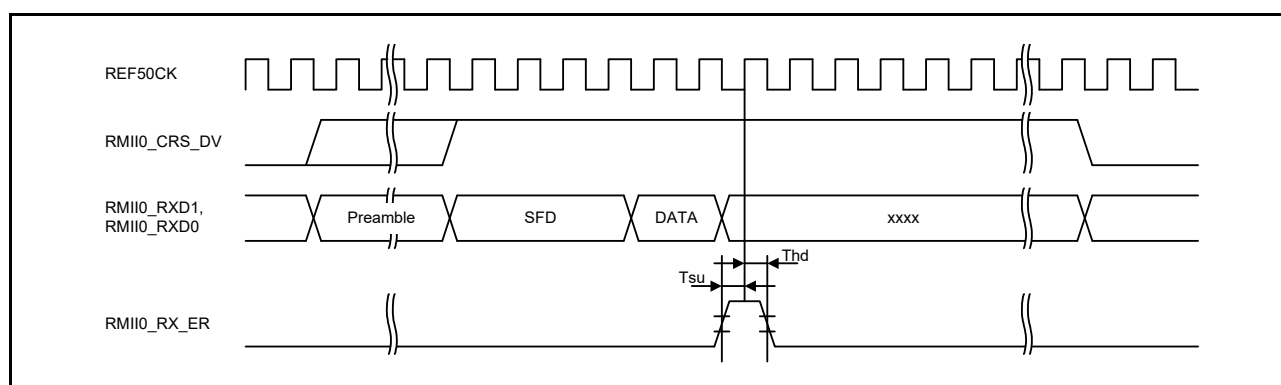


Figure 5.59 RMII Reception Timing (Error Occurrence)

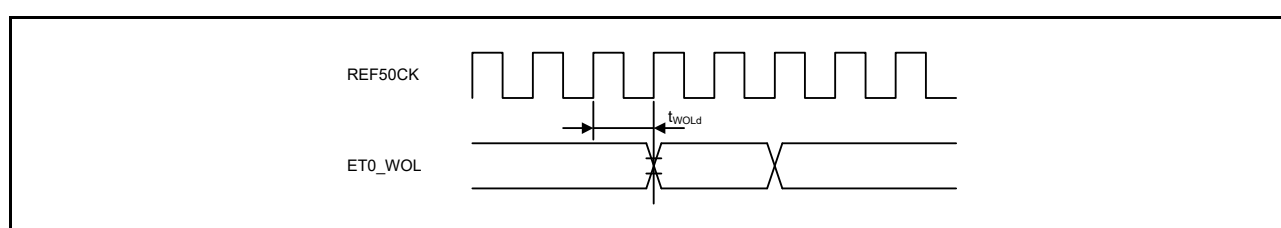


Figure 5.60 WOL Output Timing (RMII)

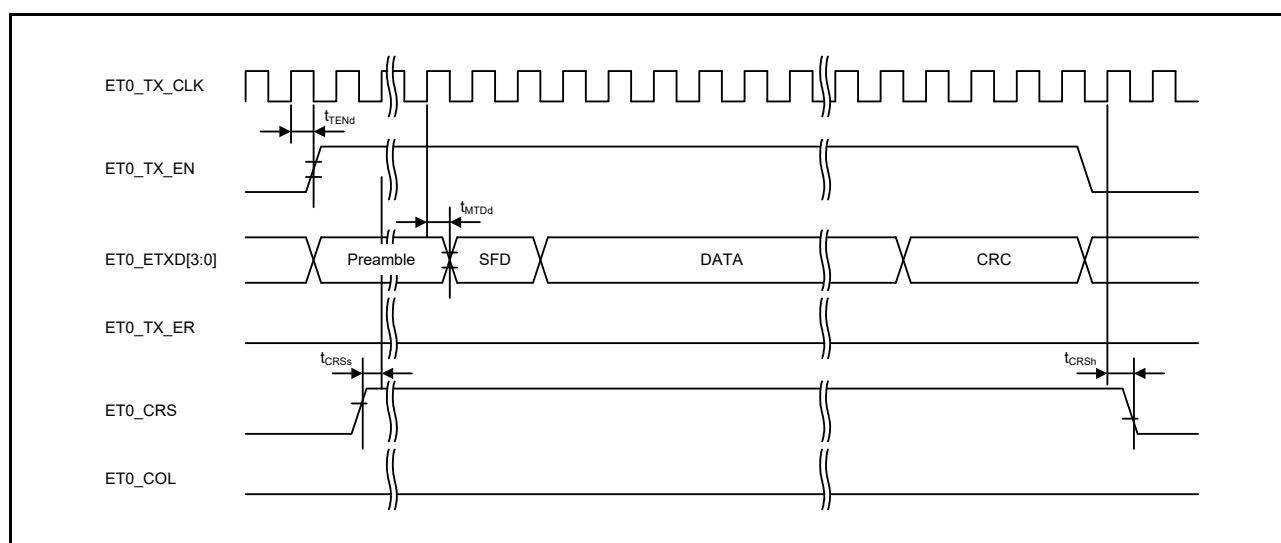


Figure 5.61 MII Transmission Timing (Normal Operation)

5.6 D/A Conversion Characteristics

Table 5.49 D/A Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	12	12	12	Bit	
Unbuffered output	Absolute accuracy	—	—	—	± 6.0	LSB	2-M Ω resistive load 10-bit conversion
	Differential nonlinearity error	DNL	—	± 1.0	± 2.0	LSB	2-M Ω resistive load
	Output resistance	R_O	—	8.6	—	k Ω	
	Setting time	t_s	—	—	3	μ s	20-pF capacitive load
Buffered output	Load resistance	R_L	5	—	—	k Ω	
	Load capacitance	C_L	—	—	50	pF	
	Output voltage	V_O	0.2	—	$AVCC1 - 0.2$	V	
	Differential nonlinearity error	DNL	—	± 1.0	± 2.0	LSB	
	Integral nonlinearity error	INL	—	± 2.0	± 4.0	LSB	
	Setting time	t_s	—	—	4	μ s	

5.7 Temperature Sensor Characteristics

Table 5.50 Temperature Sensor Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	± 1	—	$^{\circ}$ C	
Temperature slope	—	4	—	mV/ $^{\circ}$ C	
Output voltage (at 25 $^{\circ}$ C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	μ s	
Sampling time*1	4.15	—	—	μ s	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

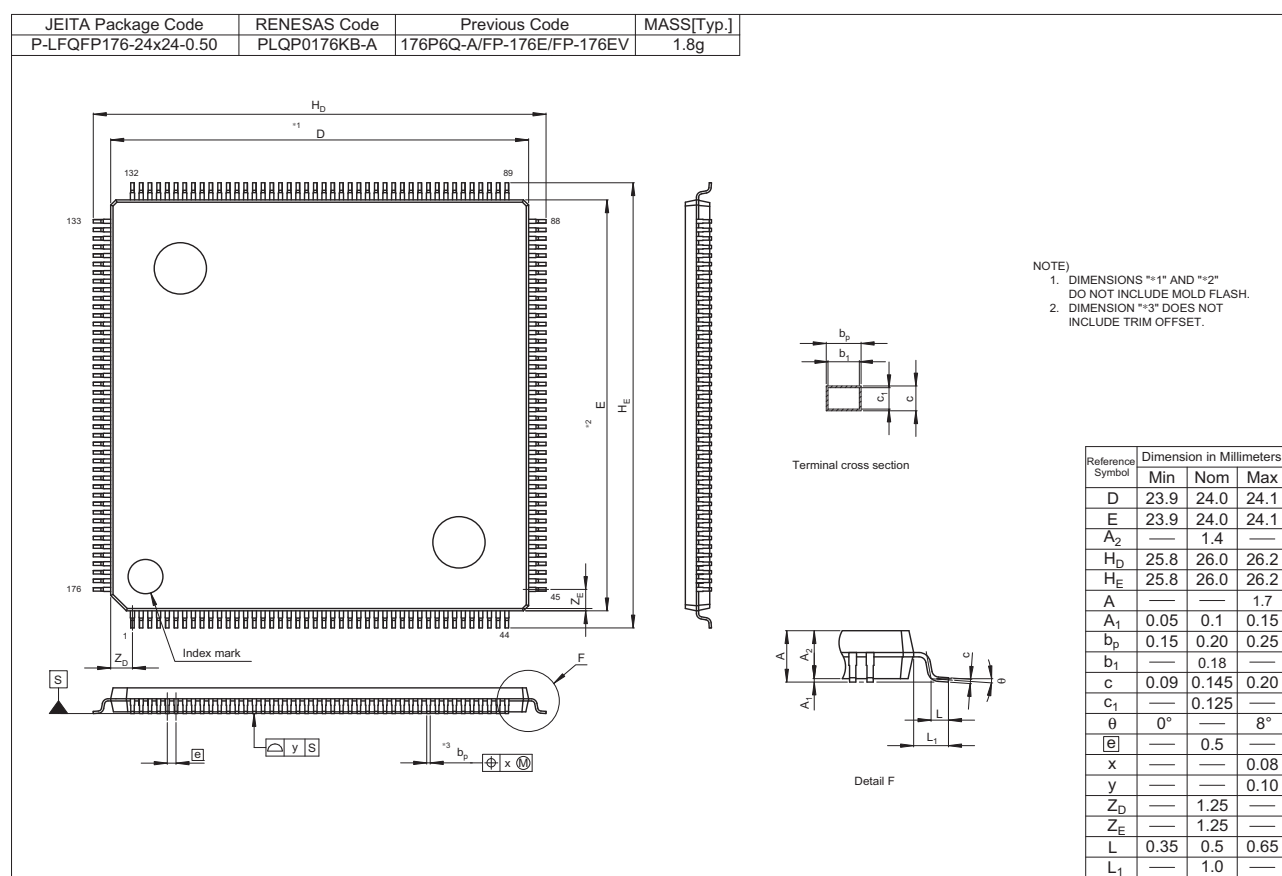


Figure C 176-Pin LFQFP (PLQP0176KB-A)