Renesas Electronics America Inc - R5F565NCDDFP#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565ncddfp-30

Table 1.1 Outline of Specifications (8/9)

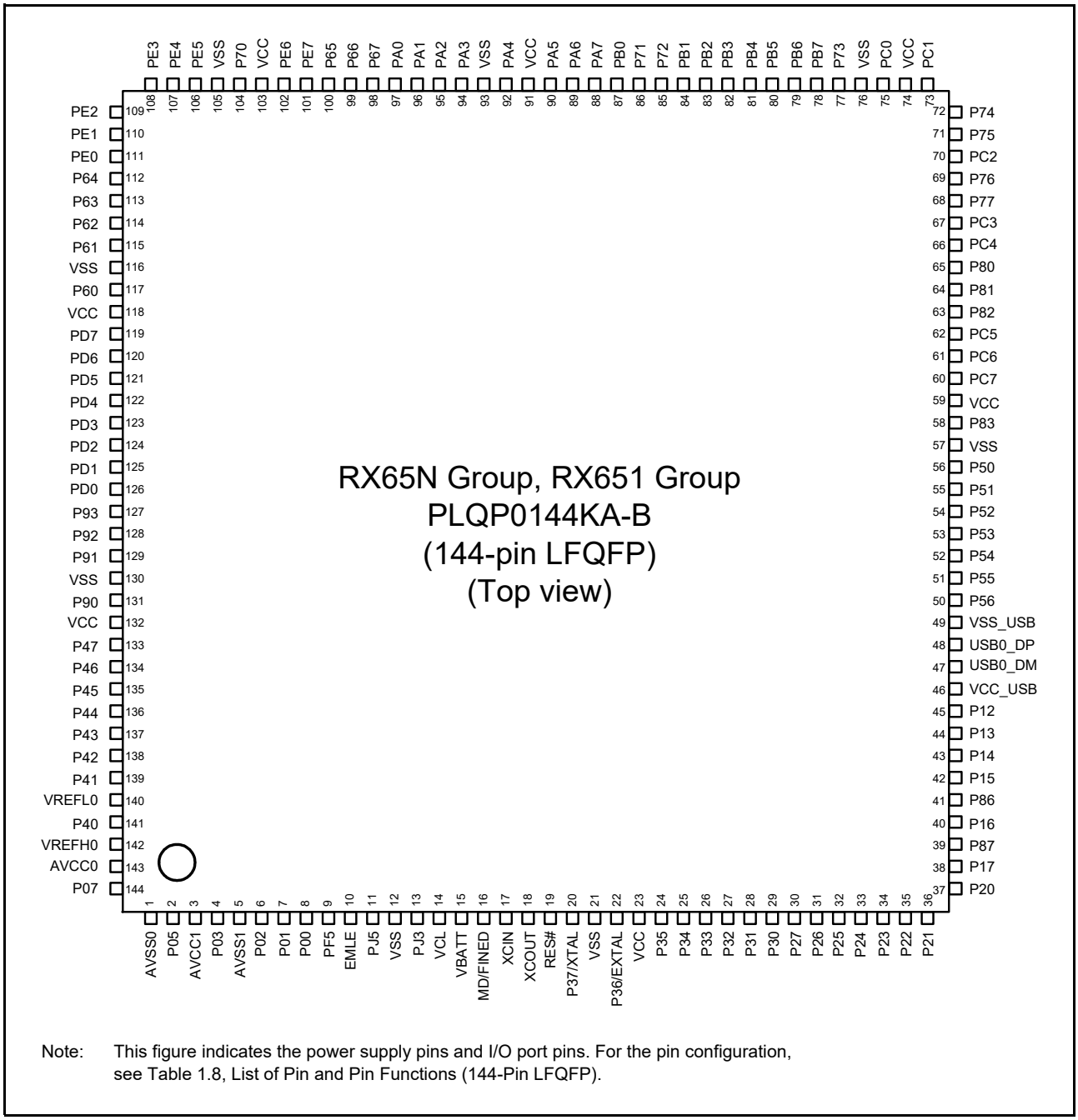
Classification	Module/Function	Description
12-bit A/D converter (S12ADFa)		• 12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels) • 12-bit resolution (switchable between 8, 10, and 12 bits) • Conversion time 0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control (only for 3 group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU3, TMR, TPU) trigger, external trigger • Event linking by the ELC
12-bit D/A converter (R12DA)		• 2 channels • 12-bit resolution • Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output) • Buffered output or unbuffered output can be selected. • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ± 1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available

Table 1.3 List of Products (6/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F56517EDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56517FDFP	PLQP0100KB-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56514ADFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56514BDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56514EDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56514FDFP	PLQP0100KB-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F5651EDDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDBG	PLBG0176GA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDBG	PLBG0176GA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651EDDLC	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDLC	PTLG0177KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDLC	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDLC	PTLG0177KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651EDDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651EHDLK	PTLG0145KA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F5651CDDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F5651CHDLK	PTLG0145KA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F56519ADLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56519BDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56519EDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56519FDLK	PTLG0145KA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56517ADLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56517BDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56517EDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56517FDLK	PTLG0145KA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F56514ADLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F56514BDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F56514EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F56514FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strove signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU in the high impedance state



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.7 Pin Assignment (144-Pin LFQFP)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
A1	AVSS0								
A2	AVCC0								
A3	VREFL0								
A4		P42						IRQ10-DS	AN002
A5		P46						IRQ14-DS	AN006
A6	VCC								
A7	VSS								
A8		P94	D20/A20						
A9	VCC								
A10	TRSYNC1	P97	D23/A23						
A11		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106
A12		P60	CS0#						
A13		P63	CAS#/ D2[A2/D2]/ CS3#						
A14		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B		ANEX1
A15		PE2	D10[A10/ D10]/D2[A2/ D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100
B1		P05						IRQ13	DA1
B2		P07						IRQ15	ADTRG0#
B3		P40						IRQ8-DS	AN000
B4		P41						IRQ9-DS	AN001
B5		P47						IRQ15-DS	AN007
B6		P91	D17/A17		SCK7				AN115
B7		P92	D18/A18	POE4#	RXD7/SMISO7/ SSCL7				AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DATA23-B	IRQ1	AN109
B9	TRDATA5	P96	D22/A22						
B10		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
B11	TRDATA7	PG1	D25						
B12	VSS								
B13		P64	WE#/D3[A3/ D3]/CS4#						
B14		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B		ANEX0

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
D14		PE7	D15[A15/D15]/D7[A7/D7]	MTIOC6A/TOC1	MISOB-B	SDHI_WP/MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105
D15		P65	CKE/CS5#						
E1		PJ5		POE8#	CTS2#/RTS2#/SS2#				
E2	EMLE								
E3		PF5						IRQ4	
E4	VSS								
E5 *1	NC								
E12		PE6	D14[A14/D14]/D6[A6/D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/MMC_CD-B	LCD_DATA10-B	IRQ6	AN104
E13	TRDATA0	PG2	D26						
E14	TRDATA1	PG3	D27						
E15		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	VBATT								
F2	VCL								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#				
F4	BSCANP								
F12		P66	DQM0/CS6#	MTIOC7D					
F13	TRSYNC	PG4	D28						
F14		PA0	DQM2/BC0#/A0	MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF	ET0_TX_EN/RMII0_TXD_EN/SSLA1-B		LCD_DATA8-B		
F15	VSS								
G1	XCIN								
G2	XCOUT								
G3	MD/FINED								
G4	TRST#	PF4							
G12	TRCLK	PG5	D29						
G13	TRDATA2	PG6	D30						
G14		PA1	DQM3/A1	MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17	ET0_WOL/SCK5/SSLA2-B		LCD_DATA7-B	IRQ11	
G15	VCC								
H1	XTAL	P37							
H2	VSS								
H3	RES#								
H4	UPSEL	P35						NMI	
H12		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B		LCD_DATA4-B	IRQ5-DS	

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (2/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
32		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
33		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
34	TCK	PF1			SCK1				
35	TDO	PF0			TXD1/SMOSI1/ SSDA1				
36		P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A				
37		P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
38		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0#
39	VCC								
40		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
41	VSS								
42		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C/PIXD7			
43		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB	SDHI_D0-C/PIXD6			
44		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN	SDHI_CLK-C/ PIXD5		IRQ9	
45		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID	SDHI_CMD-C/ PIXD4		IRQ8	
46		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C/PIXD3		IRQ7	ADTRG1#
47		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C/PIXD2			
48		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB			IRQ6	ADTRG0#
49		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
50		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (5/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
92	VSS								
93		P73	CS3#	PO16	ET0_WOL		LCD_EXTCLK-A		
94		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
95		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
96		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CLK-B		
97		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B		
98		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6	SDSI_D3-B	LCD_TCON1-B		
99		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2-B	LCD_TCON2-B		
100		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		LCD_TCON3-B	IRQ4-DS	
101		P72	A19/CS2#		ET0_MDC		LCD_DATA23-A		
102		P71	A18/CS1#		ET0_MDIO				
103	VCC								
104		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DATA0-B	IRQ12	
105	VSS								
106		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B		
107		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B		
108		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B		

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
E4	EMLE								
E5		P44						IRQ12-DS	AN004
E10		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DATA8-B*1		
E11		P66	DQM0/CS6#	MTIOC7D					
E12		P65	CKE/CS5#						
E13		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	XCIN								
F2	XCOUT								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
F4	VBATT								
F10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DATA5-B*1	IRQ6-DS	
F11	VSS								
F12		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DATA7-B*1	IRQ11	
F13		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DATA6-B*1		
G1	XTAL	P37							
G2	RES#								
G3	MD/FINED								
G4	BSCANP								
G10		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B*1		
G11		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B*1		
G12	VCC								
G13		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DATA4-B*1	IRQ5-DS	
H1	EXTAL	P36							
H2	VCC								
H3	VSS								
H4	UPSEL	P35						NMI	
H10		P72	A19/CS2#		ET0_MDC				
H11		P71	A18/CS1#		ET0_MDIO				

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (7/7)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
136		P44						IRQ12-DS	AN004
137		P43						IRQ11-DS	AN003
138		P42						IRQ10-DS	AN002
139		P41						IRQ9-DS	AN001
140	VREFL0								
141		P40						IRQ8-DS	AN000
142	VREFH0								
143	AVCC0								
144		P07						IRQ15	ADTRG0#

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.
Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (2/5)

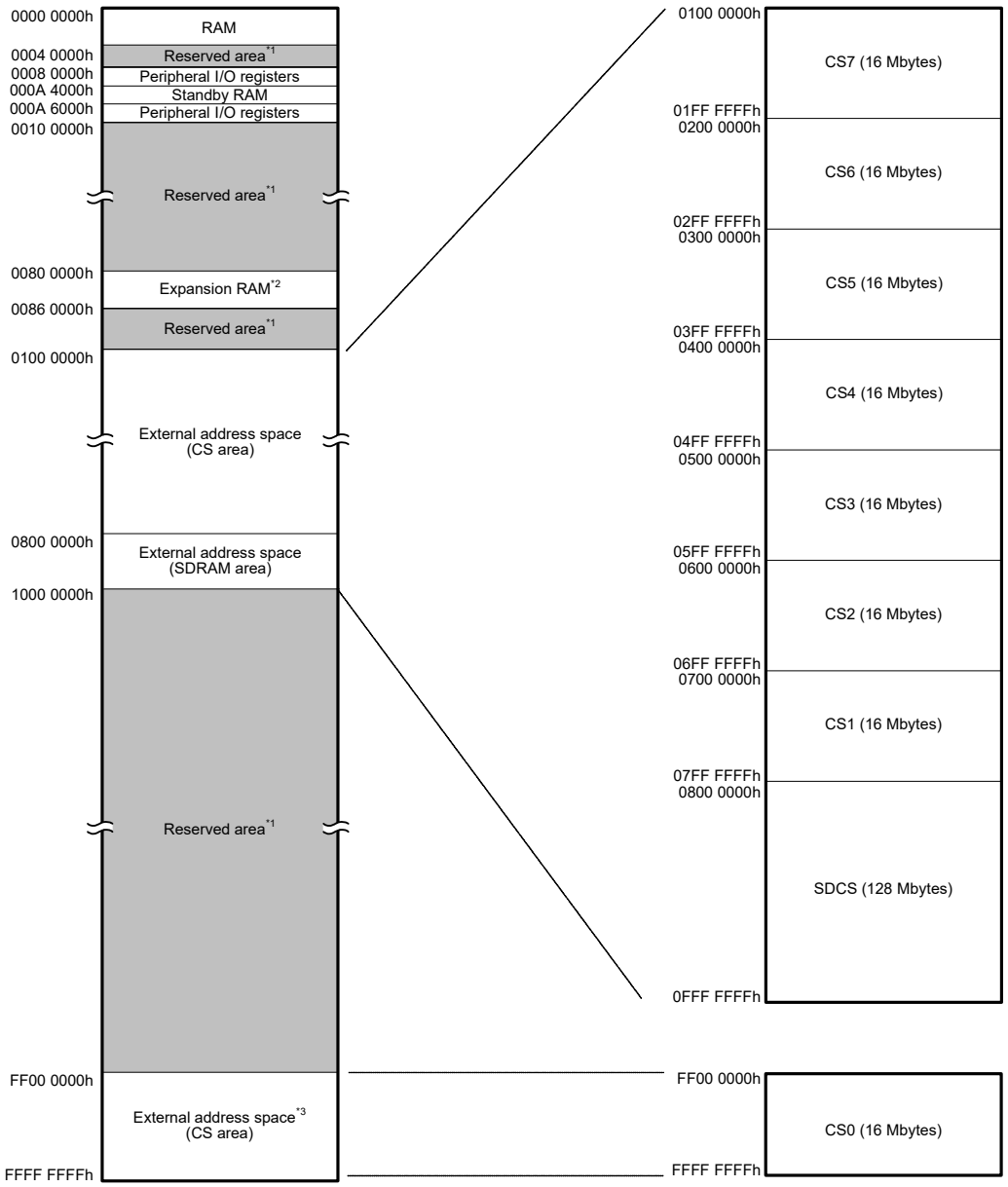
Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
26		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B				
27		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN			IRQ9	
28		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1*1/ USB0_ID			IRQ8	
29		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS			IRQ7	ADTRG1 #
30		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
31		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS			IRQ5	
32		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A			IRQ4	
33		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1 #
34		P12		TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]			IRQ2	
35	VCC_USB								
36					USB0_DM				
37					USB0_DP				
38	VSS_USB								
39		P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ CRX1			IRQ10	
40		P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
41		P53*2	BCLK						
42		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
43		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (4/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
60	VCC								
61		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD6/SMISO6/ SSCL6		LCD_DATA0-B*1	IRQ12	
62	VSS								
63		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B*1		
64		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B*1		
65		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B*1		
66		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DATA4-B*1	IRQ5-DS	
67		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DATA5-B*1	IRQ6-DS	
68		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DATA6-B*1		
69		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DATA7-B*1	IRQ11	
70		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DATA8-B*1		
71		PE7	D15[A15/ D15]/D7[A7/ D7]*1	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DATA9-B*1	IRQ7	AN105
72		PE6	D14[A14/ D14]/D6[A6/ D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DATA10-B*1	IRQ6	AN104
73		PE5	D13[A13/ D13]/D5[A5/ D5]*1	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DATA11-B*1	IRQ5	AN103
74		PE4	D12[A12/ D12]/D4[A4/ D4]*1	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DATA12-B*1		AN102
75		PE3	D11[A11/ D11]/D3[A3/ D3]*1	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#/SS12#	MMC_D7-B	LCD_DATA13-B*1		AN101
76		PE2	D10[A10/ D10]/D2[A2/ D2]*1	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B*1	IRQ7-DS	AN100
77		PE1	D9[A9/D9]/ D1[A1/D1]*1	MTIOC4C/ MTIOC3B/ PO18	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/SSLB2-B	MMC_D5-B	LCD_DATA15-B*1		ANEX1
78		PE0	D8[A8/D8]/ D0[A0/D0]*1	MTIOC3D	SCK12/SSLB1-B	MMC_D4-B	LCD_DATA16-B*1		ANEX0

3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.
Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM areas (SDCS) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. This area is only included in products with at least 1.5 Mbytes of code flash memory.
Note 3. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (26 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A068h	SCI3	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A069h	SCI3	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A06Ah	SCI3	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A06Bh	SCI3	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A06Ch	SCI3	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A06Dh	SCI3	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A06Eh	SCI3	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A06Fh	SCI3	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A06Eh	SCI3	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A070h	SCI3	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A071h	SCI3	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A070h	SCI3	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A072h	SCI3	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A080h	SCI4	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A081h	SCI4	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A082h	SCI4	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A083h	SCI4	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A084h	SCI4	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A085h	SCI4	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A086h	SMCI4	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A087h	SCI4	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A088h	SCI4	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A089h	SCI4	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

5.3 AC Characteristics

Table 5.10 Operating Frequency (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	120	MHz
	Peripheral module clock (PCLKA)			—	—	120	
	Peripheral module clock (PCLKB)			—	—	60	
	Peripheral module clock (PCLKC)			—	—	60	
	Peripheral module clock (PCLKD)			—	—	60	
	Flash-IF clock (FCLK)			—*1	—	60	
	External bus clock (BCLK)	Other than 100-pin package		—	—	120	
		100-pin package		—	—	60	
	BCLK pin output	Other than 100-pin package		—	—	60	
		100-pin package		—	—	30	
	SDRAM clock (SDCLK)	Other than 100-pin package		—	—	60	
	SDCLK pin output	Other than 100-pin package		—	—	60	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 5.11 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	1	MHz
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	Peripheral module clock (PCLKC)*1			—	—	1	
	Peripheral module clock (PCLKD)*1			—	—	1	
	Flash-IF clock (FCLK)			—	—	1	
	External bus clock (BCLK)	Other than 100-pin package		—	—	1	
		100-pin package		—	—	1	
	BCLK pin output	Other than 100-pin package		—	—	1	
		100-pin package		—	—	1	
	SDRAM clock (SDCLK)	Other than 100-pin package		—	—	1	
	SDCLK pin output	Other than 100-pin package		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

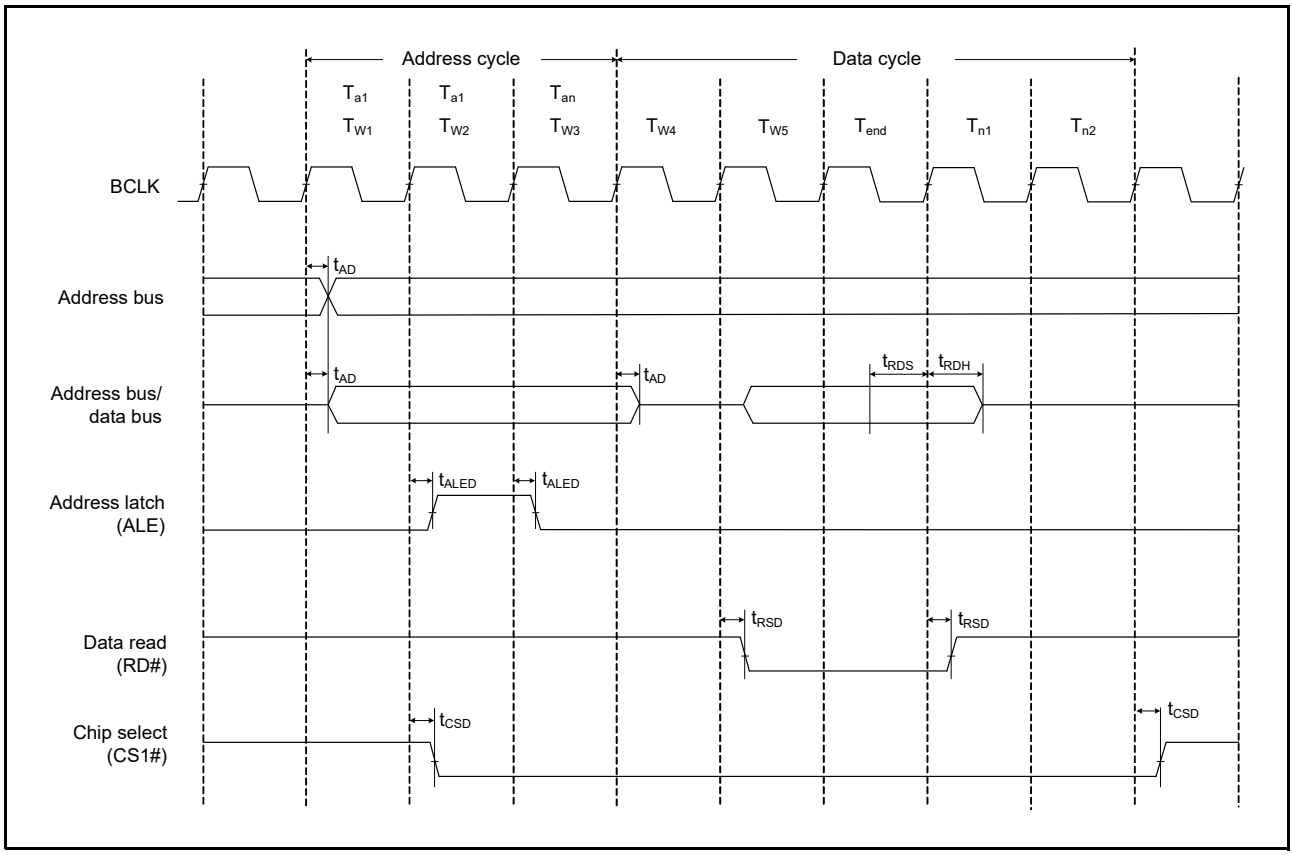


Figure 5.16 Address/Data Multiplexed Bus Read Access Timing

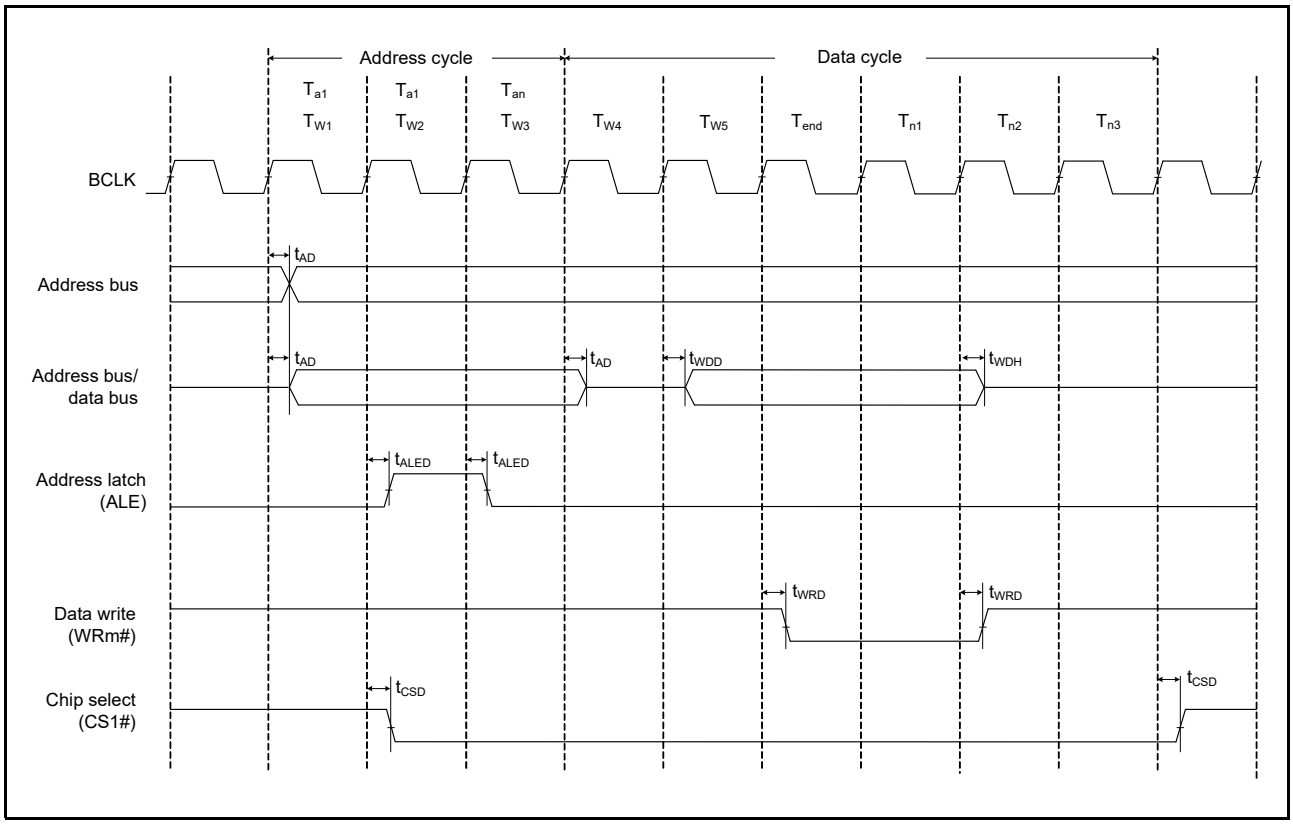


Figure 5.17 Address/Data Multiplexed Bus Write Access Timing

Table 5.28 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 5.36
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

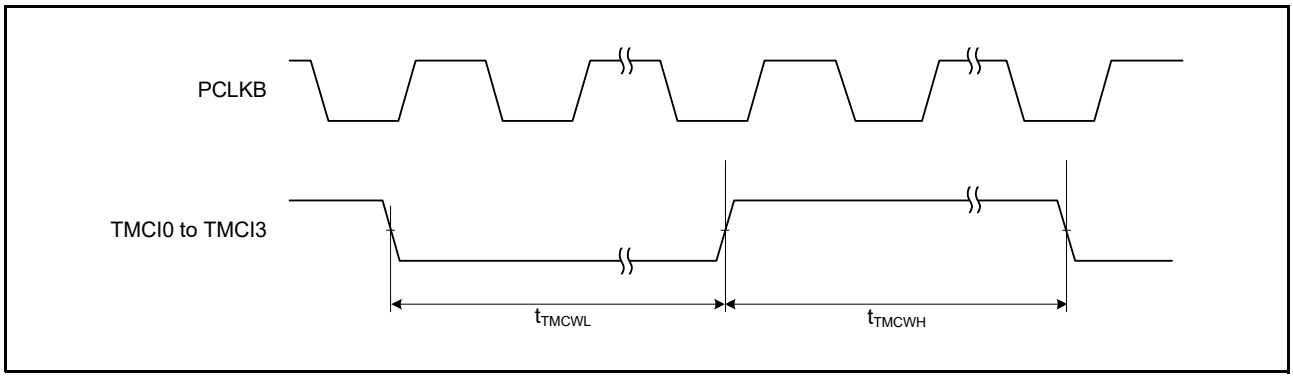


Figure 5.36 TMR Clock Input Timing

Table 5.29 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 5.37
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

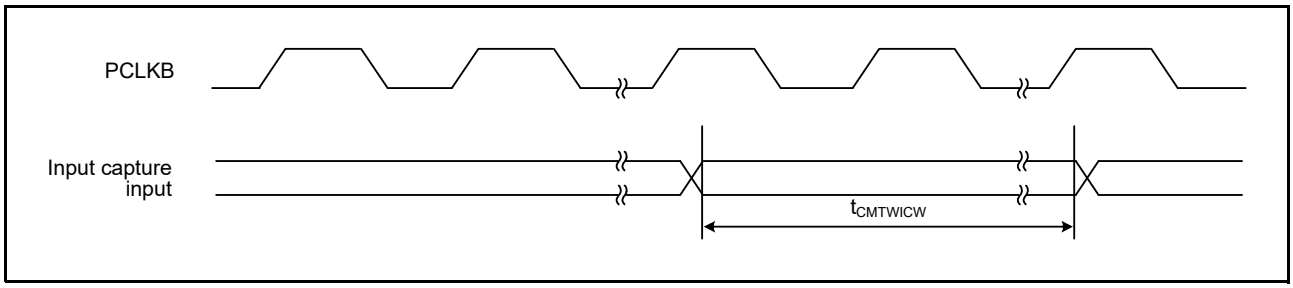


Figure 5.37 CMTW Input Capture Input Timing

Table 5.37 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions*2
QSPI	QSPCLK clock cycle	t_{QScyc}	2	4080	t_{PBcyc}	Figure 5.51
	Data input setup time*3	t_{Su}	6.5	—	ns	Figure 5.52, Figure 5.53
	Data input hold time	t_{IH}	5	—	ns	
	SS setup time	t_{LEAD}	1.5	8.5	t_{QScyc}	
	SS hold time	t_{LAG}	1	8	t_{QScyc}	
	Data output delay time	t_{OD}	—	10.0	ns	
	Data output hold time	t_{OH}	–5	—	ns	
	Successive transmission delay time	t_{TD}	1	8	t_{QScyc}	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the QSPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. For version G products (+85 < Ta ≤ +105°C), the high-drive ability control register of the QSPCLK pin measures this data input setup time with the high-speed interface high-drive output selected.

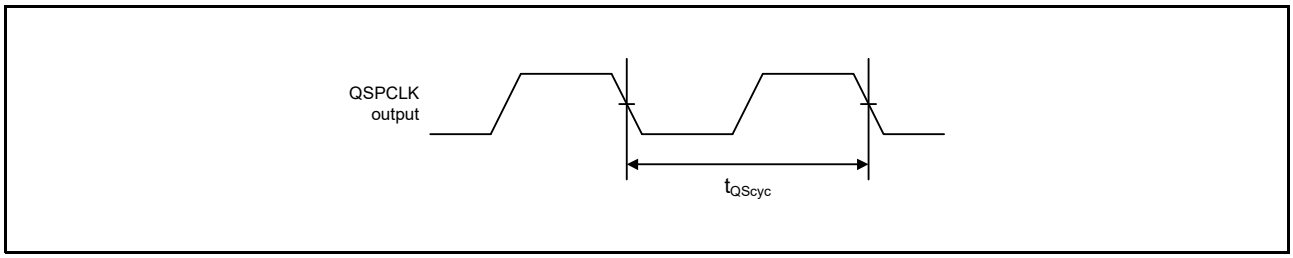


Figure 5.51 QSPI Clock Timing

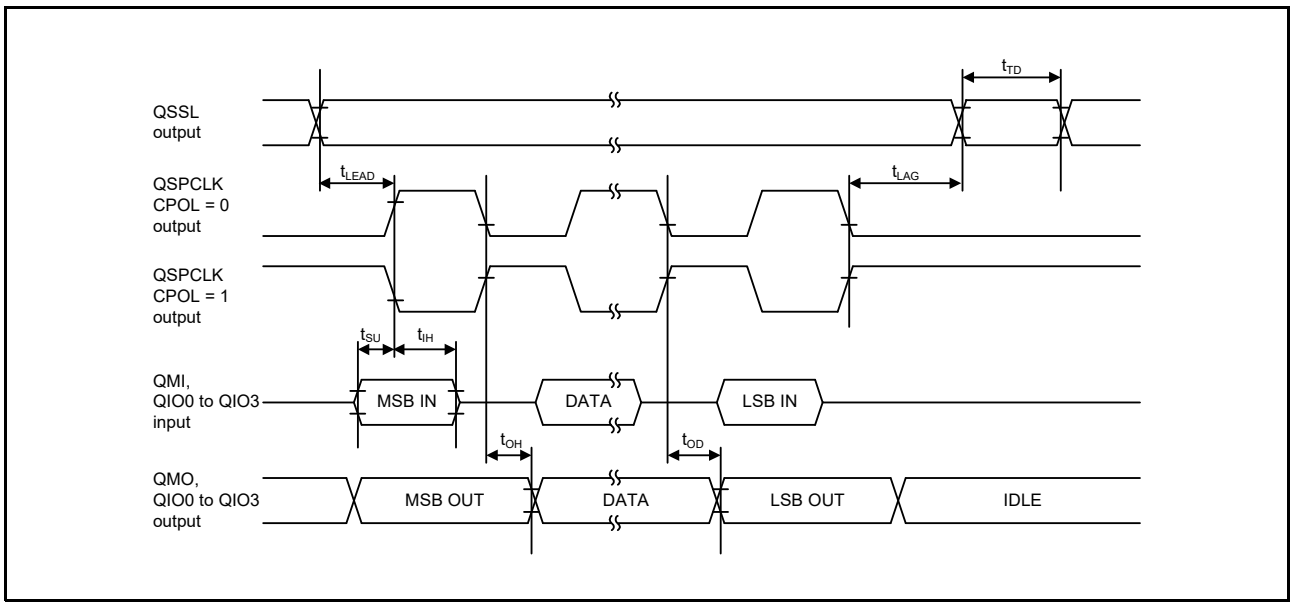


Figure 5.52 Transmit/Receive Timing (CPHA = 0)

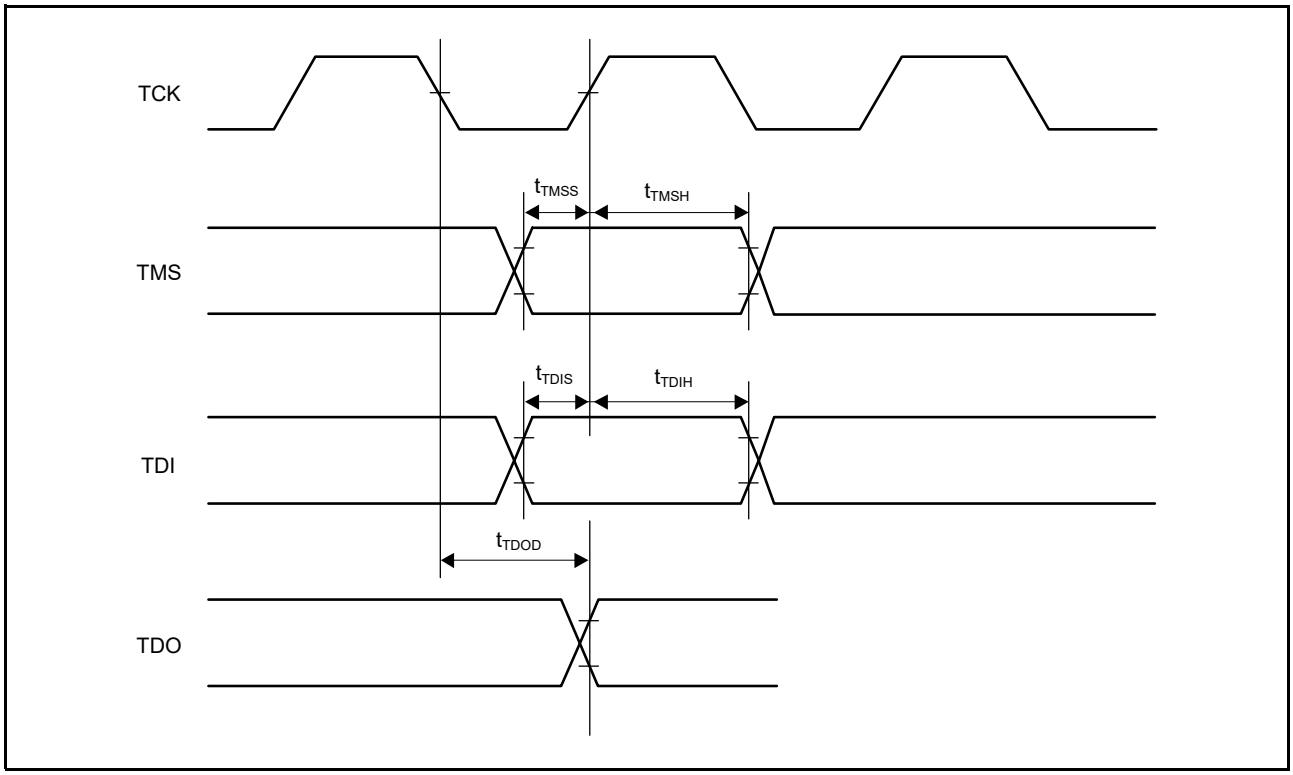
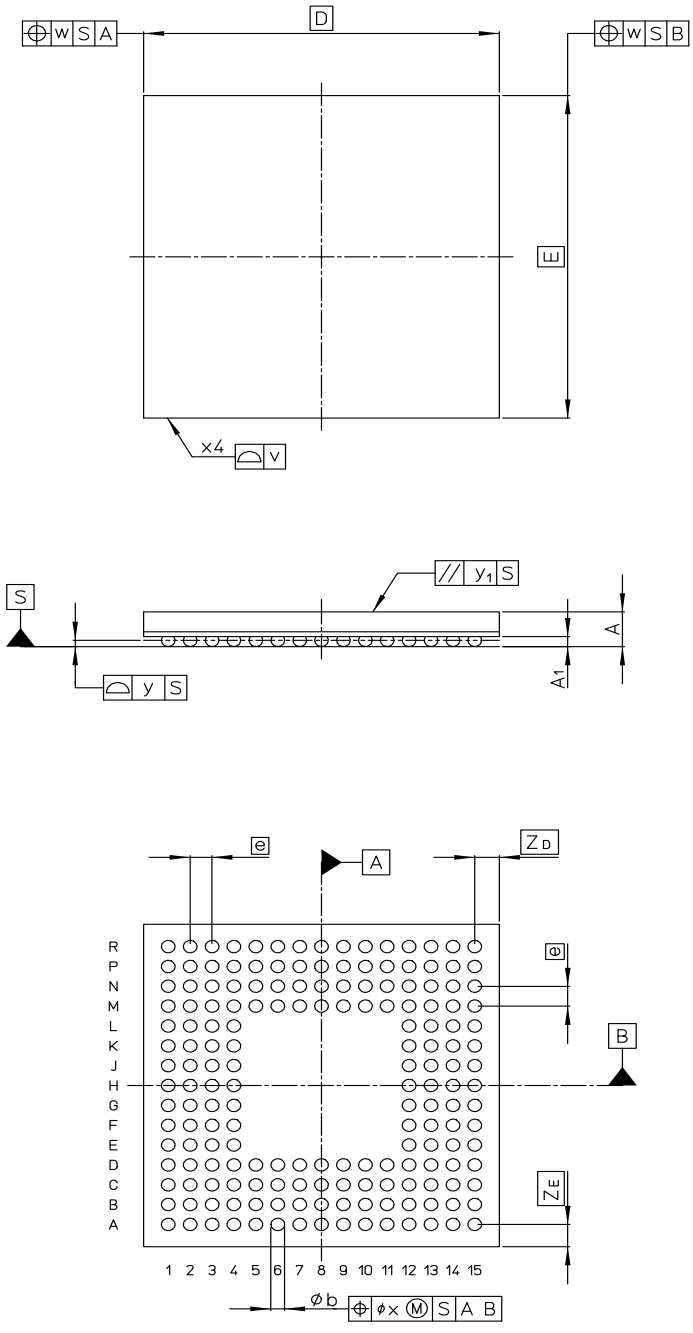


Figure 5.85 Boundary Scan Input/Output Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.2
SD	—	—	—
SE	—	—	—
ZD	—	0.90	—
ZE	—	0.90	—

Figure B 176-Pin LFBGA (PLBG0176GA-A)